Features

- E^2 Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1 bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays
- Simple Interface to SRAM FPGAs Requires Only One User I/O Pin
- Compatible With AT6000 FPGAs, ATT3000 FPGA, EPF8000 FPGAs, ORCA FPGAs, XC2000, XC3000, XC4000, XC5000 FPGAs
- Cascadable To Support Additional Configurations or Future Higher-density Arrays (17C128 and 17C256 only)
- Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available In the Space-efficient Plastic DIP or Surface-mount PLCC and SOIC Packages
- In-system Programmable Via 2-Wire Bus
- Emulation of 24CXX Serial E^2PROMs

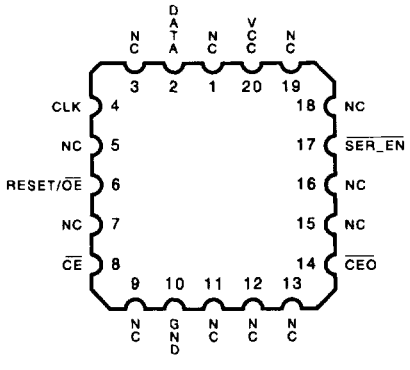
Description

The AT17C65/128/256 (AT17CXXX family) FPGA Configuration E^2PROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Both the AT17C65 and the AT17C128 are packaged in the 8-pin DIP and the popular 20-pin Plastic Leaded Chip Carrier, and SOIC. The AT17C256 is available in 14-pin SOIC or 20-pin PLCC or SOIC packages. The AT17CXXX family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17CXXX organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17CXXX, the user can select the polarity of the reset function by programming a special E^2PROM bit.

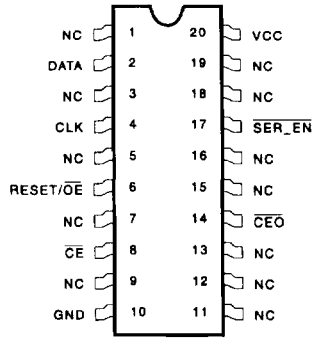
The AT17C65/128/256 can be programmed with the standard programmers from other manufacturers.

Pin Configurations

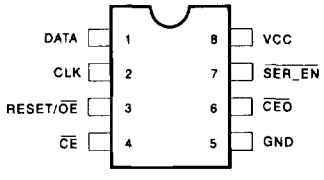
20-Pin PLCC



20-Pin SOIC



8-Pin DIP



FPGA Configuration E^2PROM

65K, 128K, and 256K

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Controlling The AT17C65/128/256 Serial E²PROMs

Most connections between the FPGA device and the Serial E²PROM are simple and self-explanatory:

- The DATA output of the AT17C65/128/256 drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17C65/128/256.
- The $\overline{CEO}$ output of any AT17C128/256 drives the $\overline{CE}$ input of the next AT17C128/256 in a cascade chain of PROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC}.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics Waveform.

Condition 1

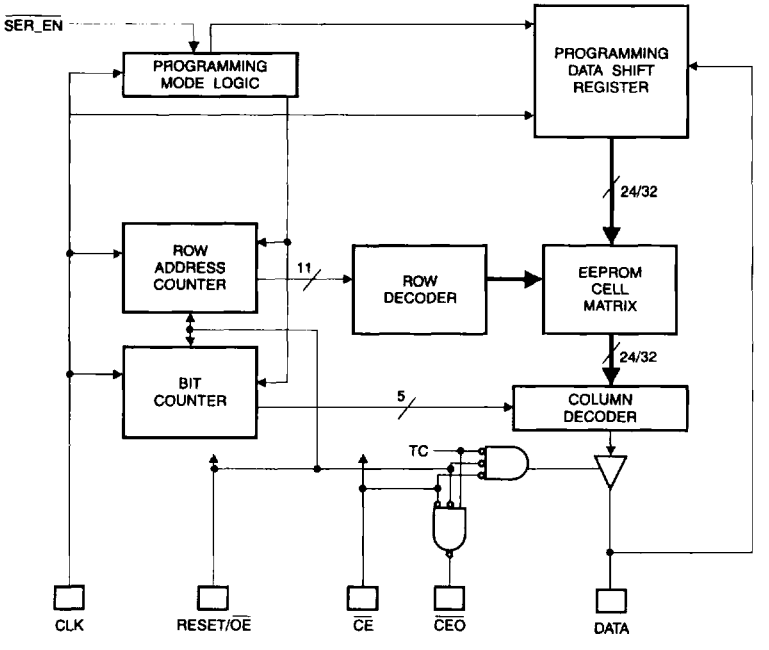
The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel. Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle.

If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17C65/128/256 does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the CE input of the AT17C65/128/256, while its $\overline{OE}$ input is driven by the inversion of the FPGA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A high level on the RESET/$\overline{OE}$ input to the AT17CXXX during FPGA reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The AT17C65/ 128/256 does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

PLCC/SOIC	DIP			
Pin	**Pin**	**Name**	**I/O**	**Description**
2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$	I	RESET/Output Enable input. A Low level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or RESET/$\overline{OE}$. This document describes the pin as RESET/$\overline{OE}$.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.
10	5	GND		Ground pin.
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
17	7	$\overline{SER\_EN}$	I	Serial enable is normally high during FPGA loading operations. Bringing $\overline{SER\_EN}$ low, enables the two wire serial interface mode for programming.
20	8	V_{CC}		+5V power supply input.

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FPGA Master Serial Mode Summary

The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration E^2PROM has been designed for compatibility with the Master Serial Mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Cascading Serial Configuration E²PROMs (AT17C128 and AT17C256)

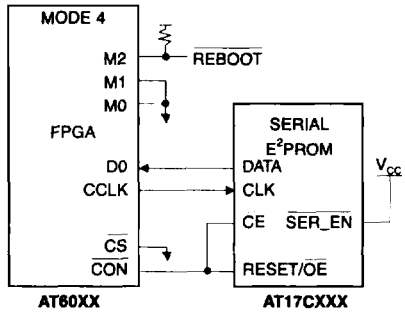
For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory (17C128 and 17C256 only).

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if $\overline{RESET}$ goes Low forcing the RESET/$\overline{OE}$ on each Configurator to go High.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground.

Mode 4 Configuration



Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ low. In this mode the chip can be programmed by a 2-wire interface. The programming is done at V_{CC} supply only. Programming (High) voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information.

AT17CXXX Reset Polarity

The AT17CXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE.

Standby Mode

The AT17CXXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 1.0 mA of current. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

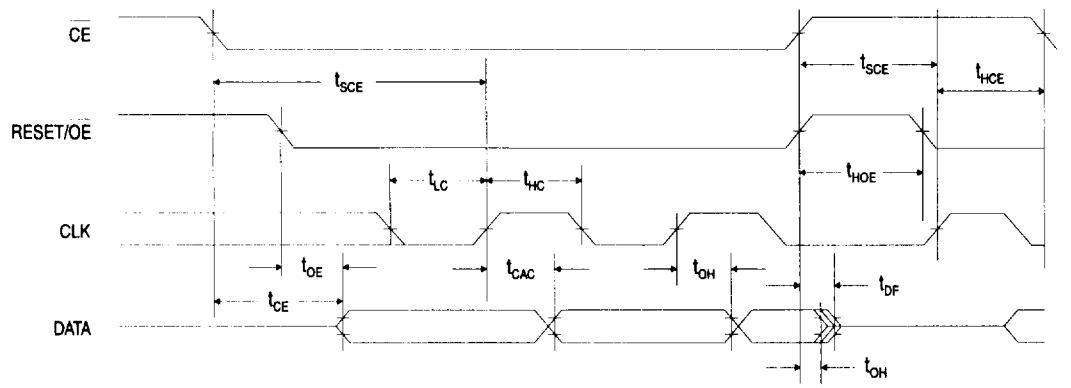
Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	V

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		1	mA
		Industrial/Military		2	mA

AC Characteristics Over Operating Conditions

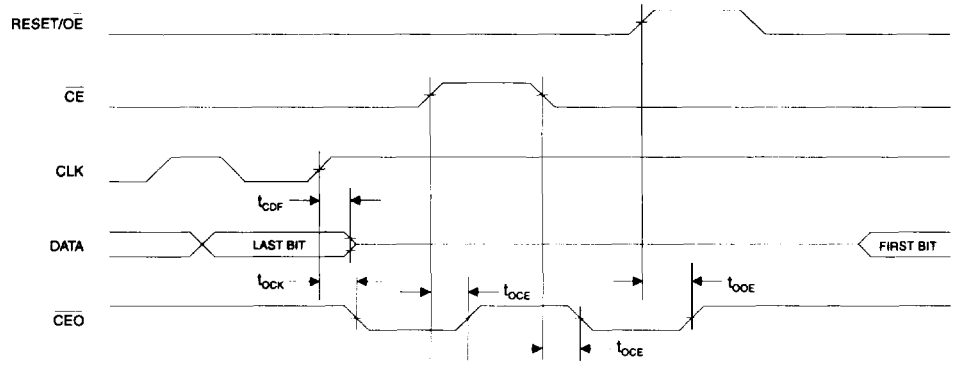


AC Characteristics Over Operating Conditions

Symbol	Description	Commercial		Industrial/Military		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to Data Delay		110		150	ns
T_{CE}	$\overline{CE}$ to Data Delay		50		50	ns
T_{CAC}	CLK to Data Delay		50		55	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	30		35		ns
T_{HC}	CLK High Time	30		35		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	45		50		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		5		ns
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Is Reset)	50		60		ns
F_{MAX}	MAX Input Clock Frequency		10		10	MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±500 mV from steady state active levels.

AC Characteristics Over Operating Conditions When Cascading



AC Characteristics Over Operating Conditions When Cascading

Symbol		Description	Commercial		Industrial/Military		Units
			Min	Max	Min	Max	
1	T_{CDF}	CLK to Data Float Delay		50		50	ns
2	T_{OCK}	CLK to $\overline{CEO}$ Delay		65		75	ns
3	T_{OCE}	CE to $\overline{CEO}$ Delay		55		60	ns
4	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		55		55	ns

Ordering Information

Memory Size (K)	Ordering Code	Package	Operation Range
64K	AT17C65-10PC AT17C65-10JC AT17C65-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17C65-10PI AT17C65-10JI AT17C65-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
128K	AT17C128-10PC AT17C128-10JC AT17C128-10SC	8P3 20J 20S	Commercial (0°C to 70°C)
	AT17C128-10PI AT17C128-10JI AT17C128-10SI	8P3 20J 20S	Industrial (-40°C to 85°C)
256K	AT17C256-10JC AT17C256-10SC	20J 20S	Commercial (0°C to 70°C)
	AT17C256-10JI AT17C256-10SI	20J 20S	Industrial (-40°C to 85°C)

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Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)