CY7C1358A/ GVT7164T18

64K x 18 Synchronous Cache Tag RAM Pipelined Output

Features

- **Fast match times: 4.5, 5.0, 6.0, and 7.0 ns**
- **Fast clock speed: 133, 100, 83, and 75 MHz**
- **Fast OE access times: 4.5 ns and 5.0 ns**
- **Pipelined data comparator**
- **Data input register load control by $\overline{DEN}$**
- **3.3V –5% and +10% power supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SS} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Two chip enables for depth expansion**
- **Address, data, and control registers**
- **Internally self-timed Write cycle**
- **Automatic power-down for portable applications**
- **Low profile 100-pin TQFP package**

Functional Description

The Cypress Synchronous SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT7164T18 SRAM integrates 65,536 x 18 SRAM cells with advanced synchronous peripheral circuitry and a 18-bit comparator for tag compare operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion Chip Enables ($\overline{CE}$ and CE1), Write Enable ($\overline{WE}$), and Data Input Enable ($\overline{DEN}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$) and the Match Output Enable ($\overline{MOE}$). The Data Outputs (Q) and Match Output (MATCH), enabled by $\overline{OE}$ and $\overline{MOE}$ respectively, are also asynchronous.

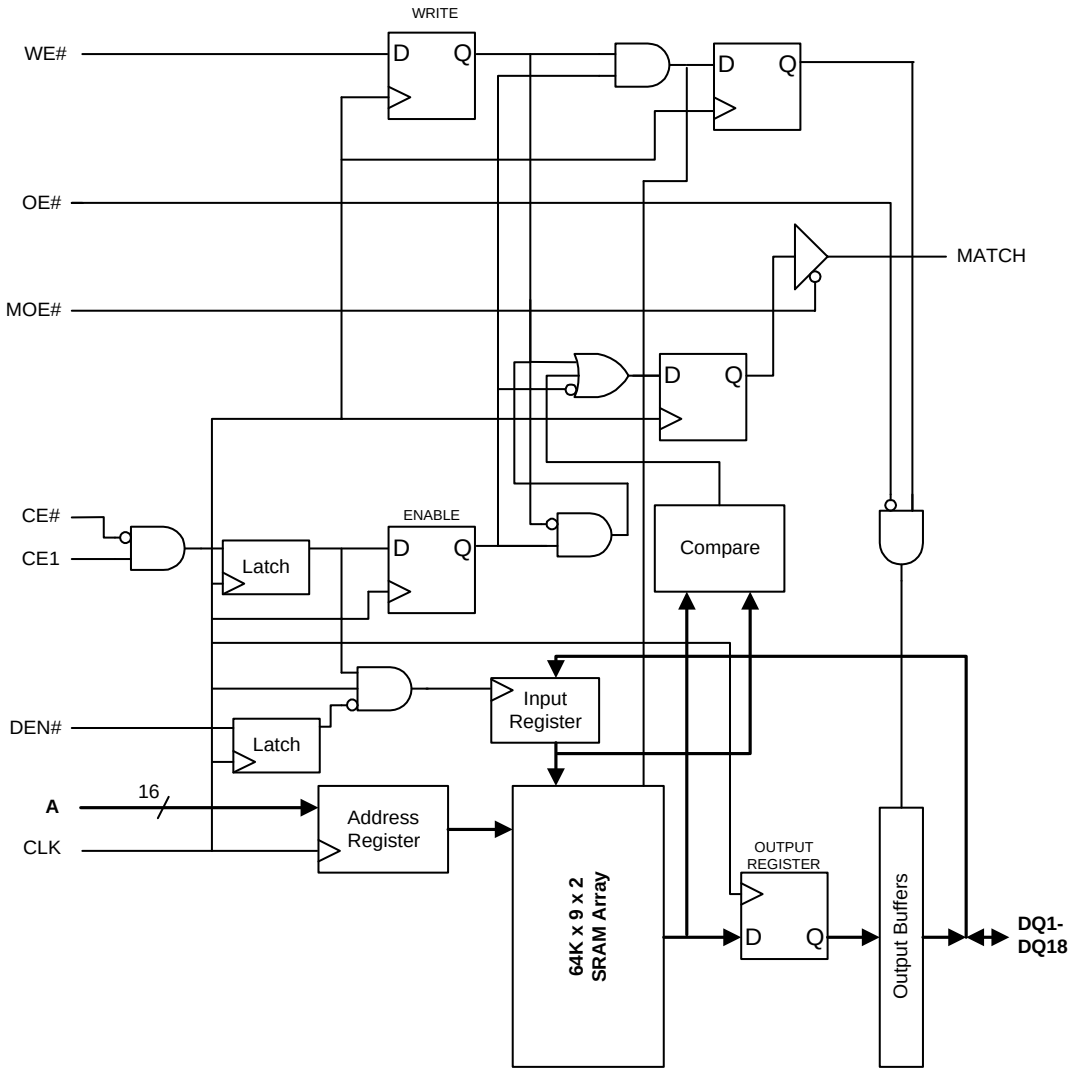
Data inputs are registered with Data Input Enable ($\overline{DEN}$) and Chip Enable pins ($\overline{CE}$, CE1). The outputs of the data input registers are compared with data in the memory array and a match signal is generated. The match output is gated into a pipeline register and released to the match output pin at the next rising edge of Clock (CLK).

The GVT7164T18 operates from a +3.3V power supply. All inputs and outputs are LVTTL compatible. The device is ideally suited for address tag RAM for up to 2 MB secondary cache.

Selection Guide

	7C1358A-133 7164T18-4	**7C1358A-100 7164T18-5**	**7C1358A-83 7164T18-6**	**7C1358A-75 7164T18-7**
Maximum Access Time (ns)	4.5	5.0	6.0	7.0
Maximum Operating Current (mA)	300	240	220	200
Maximum CMOS Standby Current (mA)	20	20	20	20

Functional Block Diagram—64Kx18[1]

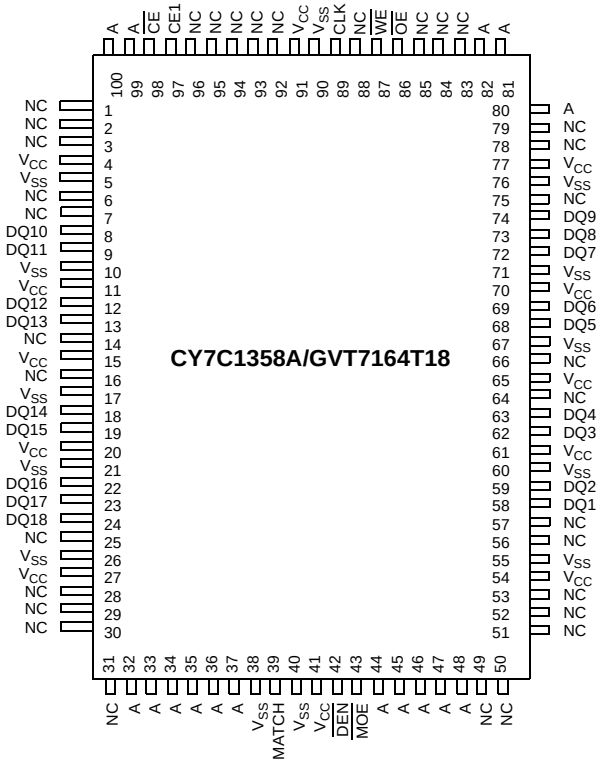


Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP
Top View



119-Lead BGA
Top View

	1	2	3	4	5	6	7
A	V_{CC}	A	A	NC	A	NC	V_{CC}
B	NC	CE1	NCA	NC	NC	$\overline{CE}$	NC
C	NC	NC	NC	V_{CC}	A	A	NC
D	DQ10	NC	V_{SS}	NC	V_{SS}	DQ9	NC
E	NC	DQ11	V_{SS}	NC	V_{SS}	NC	DQ8
F	V_{CC}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ7	V_{CC}
G	NC	DQ12	NC	NC	V_{SS}	NC	DQ6
H	DQ13	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ5	NC
J	V_{CC}	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CC}
K	NC	DQ14	V_{SS}	CLK	V_{SS}	NC	DQ4
L	DQ15	NC	V_{SS}	NC	NC	DQ3	NC
M	V_{CC}	DQ16	V_{SS}	NC	V_{SS}	NC	V_{CC}
N	DQ17	NC	V_{SS}	A	V_{SS}	DQ2	NC
P	NC	DQ18	V_{SS}	A	V_{SS}	NC	DQ1
R	NC	A	A	V_{CC}	A	A	NC
T	NC	A	A	MATCH	A	A	ZZ
U	V_{CC}	$\overline{DEN}$	NC	A	$\overline{MOE}$	NC	V_{CC}

Pin Descriptions

BGA Pins	TQFP Pins	Pin Name	Type	Description
2A, 3A, 5A, 5C, 6C, 4N, 4P, 2R, 3R, 5R, 6R, 2T, 3T, 5T, 6T, 4U	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK.
4H	87	$\overline{WE}$	Input-Synchronous	Write Enable: this write enable is LOW for a Write cycle and HIGH for a Read cycle. Data I/O are high impedance one cycle after $\overline{WE}$ = LOW is gated into register.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and data input enable control input on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
6B	98	$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE1	Input-Synchronous	Chip Enable: This active HIGH input is used to enable the device.
4F	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
2U	42	$\overline{DEN}$	Input-Synchronous	Data Input Enable: This active LOW input is used to control the update of data input registers.
4T	39	MATCH	Output	Match Output: MATCH will be HIGH if data in the data input registers match the data stored in the memory array, assuming $\overline{MOE}$ being LOW. MATCH will be LOW if data do not match.
5U	43	$\overline{MOE}$	Input	Match Output Enable: This active LOW asynchronous input enables the MATCH output drivers.
7P, 6N, 6L, 7K, 6H, 7G, 6F, 7E, 6D, 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	58, 59, 62, 63, 68, 69, 72, 73, 74, 8, 9, 12, 13, 18, 19, 22, 23, 24	DQ1–DQ18	Input/Output	Data Inputs/Outputs: Input data must meet set-up and hold times around the rising edge of CLK.
1A, 7A, 4C, 1F, 7F, 1J, 2J, 4J, 6J, 7J, 1M, 7M, 4R, 1U, 7U	4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: +3.3V –5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	5, 10, 17, 21, 26, 38, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Ground	Ground: GND
4A, 6A, 1B, 3B, 4B, 5B, 7B, 1C, 2C, 3C, 7C, 2D, 4D, 7D, 1E, 4E, 6E, 2F, 1G, 3G, 4G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 5L, 7L, 4M, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 7T, 3U, 6U	1-3, 6, 7, 14, 16, 25, 28-31, 49-53, 56, 57, 64, 66, 75, 78, 79, 83-85, 88, 92-96	NC	-	No Connect: These signals are not internally connected.

Truth Table[2, 3, 4, 5, 6]

Operation	$\overline{E}$	$\overline{WE}$	$\overline{DEN}$	$\overline{MOE}$	$\overline{OE}$	MATCH	DQ
READ Cycle	L	H	X	X	L	-	Q
WRITE Cycle	L	L	L	X	H	-	D
Fill WRITE Cycle	L	L	H	X	H	-	High-Z
COMPARE Cycle	L	H	L	L	H	Output	D
Deselected Cycle (MATCH Out)	H	X	X	L	X	H	High-Z
Deselected Cycle	H	X	X	H	X	High-Z	High-Z

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) .....–55°C to +150°C

Junction Temperature .....+150°C

Power Dissipation..... 1.0W

Short Circuit Output Current..... 50 mA

Operating Range

Range	Ambient Temperature[7]	V_{CC} [8]
Com'l	0°C to +70°C	3.3V –5%/+10%

Notes:

2. X means "Don't Care." H means logic HIGH. L means logic LOW.
3. E=L is defined as CE = LOW and CE1 = HIGH. E =H is defined as CE=HIGH or CE1 = LOW.
4. All inputs except OE and MOE must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. For a write operation following a read operation, OE must be HIGH before the input data required set-up time plus High-Z time for OE and staying HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. T_A is the case temperature.
8. Power supply ramp up should be monotonic.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[9, 10]	Data Inputs (DQxx)	2.0	V_{CC}+0.5	V
V_{IH}		All Other Inputs	2.0	4.6	V
V_{Il}	Input Low (Logic 0) Voltage[9, 10]		–0.5	0.8	V
IL_I	Input Leakage Current[11]	$0V \le V_{IN} \le V_{CC}$	–1	1	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–1	1	µA
V_{OH}	Output High Voltage[9, 12]	I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output Low Voltage[9, 12]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[9]		3.135	3.6	V

Parameter	Description	Conditions	Typ.	133 MHz/ -4	100 MHz/ -5	83 MHz/ -6	75 MHz/ -7	Unit
I_{CC}	Power Supply Current: Operating[13, 14, 15]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} = Max.; outputs open	150	300	240	220	200	mA
I_{SB2}	CMOS Standby[14, 15]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby[14, 15]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	10	20	20	20	20	mA
I_{SB4}	Clock Running[14, 15]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ min.	40	80	70	60	50	mA

Capacitance[16]

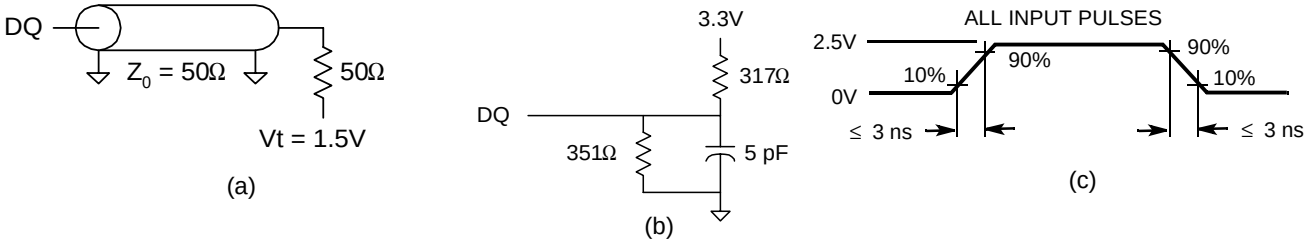
Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	4	5	pF
C_O	Input/Output Capacitance (DQ)		7	8	pF

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB	Θ_{JA}	25	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	9	°C/W

Notes:
9. All voltages referenced to V_{SS} (GND).
10. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot: $V_{IL} \le -2.0V$ for $t \le t_{KC}/2$.
11. Capacitance derating applies to capacitance different from the load capacitance shown in part (a) of AC Test Loads.
12. AC I/O curves are available upon request.
13. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
14. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
15. Typical values are measured at 3.3V, 25°C, and 8.5-ns cycle time.
16. This parameter is sampled.

AC Test Loads and Waveforms [17]



Switching Characteristics Over the Operating Range[18]

Parameter	Description	-4 133 MHz		-5 100 MHz		-6 83 MHz		-7 75 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	6.0		6.7		7.5		8.5		ns
t_{KH}	Clock HIGH Time	2.4		2.6		2.8		3.4		ns
t_{KL}	Clock LOW Time	2.4		2.6		2.8		3.4		ns
Output Times										
t_{KQ}	Clock to Output Valid		3.5		3.8		4.0		4.0	ns
t_{KM}	Clock to MATCH Valid									
t_{KQX}	Clock to Output Invalid	1.5		1.5		1.5		1.5		ns
t_{KMX}	Clock to MATCH Invalid									
t_{KQLZ}	Clock to Output in Low-Z[16, 19, 20]	0		0		0		0		ns
t_{KQHZ}	Clock to Output in High-Z[16, 19, 20]	1.5	6.0	1.5	6.7	1.5	7.5	1.5	8.5	ns
t_{OEQ}	OE to Output Valid[21]		3.5		3.5		3.8		3.8	ns
t_{MOEM}	MOE to MATCH Valid[21]									
t_{OELZ}	OE to Output in Low-Z[16, 19, 20]	0		0		0		0		ns
t_{MOELZ}	MOE to MATCH in Low-Z[16, 19, 20]									
t_{OEHZ}	OE to Output in High-Z[16, 19, 20]		3.5		3.5		3.8		3.8	ns
t_{MOEHZ}	MOE to MATCH in High-Z[16, 19, 20]									
Set-up Times										
t_S	Address, Controls, and Data In[22]	1.5		1.5		1.5		2.0		ns
Hold Times										
t_H	Address, Controls, and Data In[22]	0.5		0.5		0.5		0.5		ns

Notes:

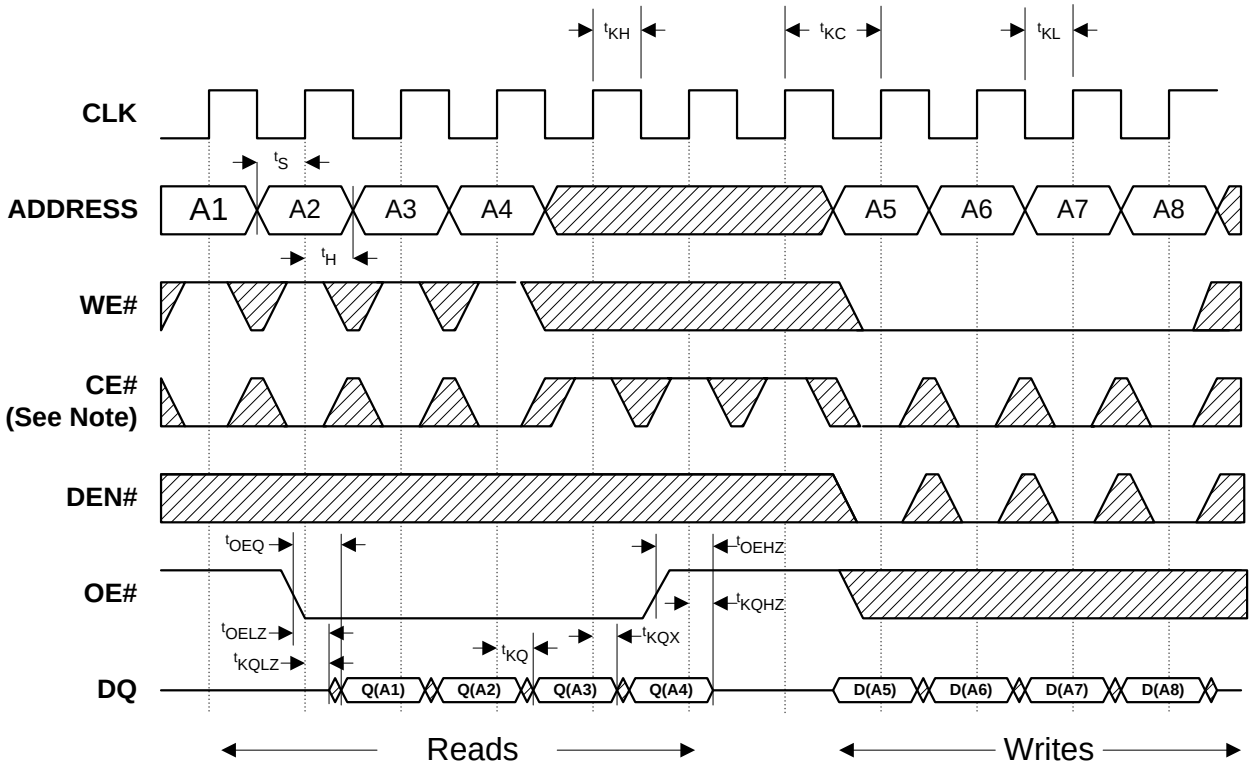
17. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.
18. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
19. Output loading is specified with C_L = 5 pF as in AC Test Loads.
20. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ}, t_{OEHZ} is less than t_{OELZ} and t_{MOEHZ} is less than t_{MOELZ}.
21. $\overline{OE}$ is a “Don’t Care” when a Write Enable ($\overline{WE}$) is sampled LOW.
22. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “Don’t Care” as defined in the truth table.

Typical Output Buffer Characteristics

Output High Voltage	Pull-Up Current			Output Low Voltage	Pull-Down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.		V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
–0.5	–38	–105		–0.5	0	0
0	–38	–105		0	0	0
0.8	–38	–105		0.4	10	20
1.25	–26	–83		0.8	20	40
1.5	–20	–70		1.25	31	63
2.3	0	–30		1.6	40	80
2.7	0	–10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

Switching Waveforms

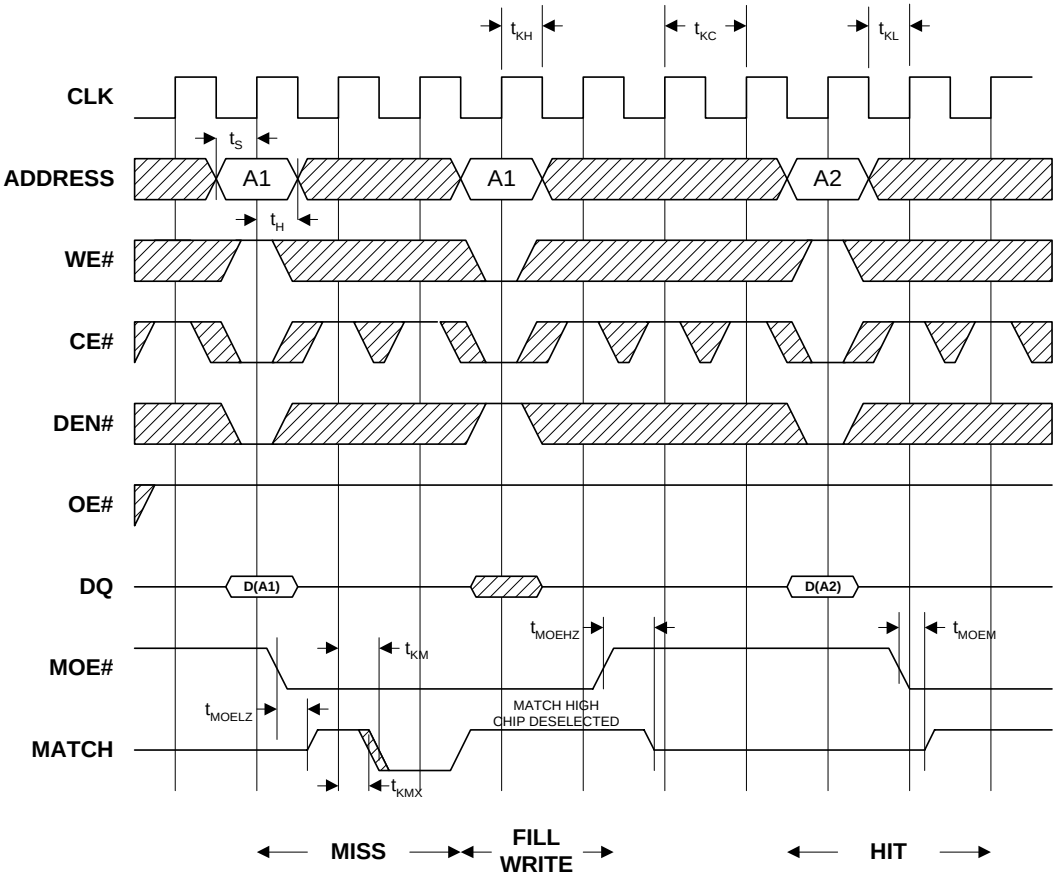
Read/Write Timing[23]



Notes:
23. $\overline{CE}$ active in this timing diagram means that all Chip Enables $\overline{CE}$ and CE1 are active.

Switching Waveforms (continued)

Compare/Fill Write Timing[23]

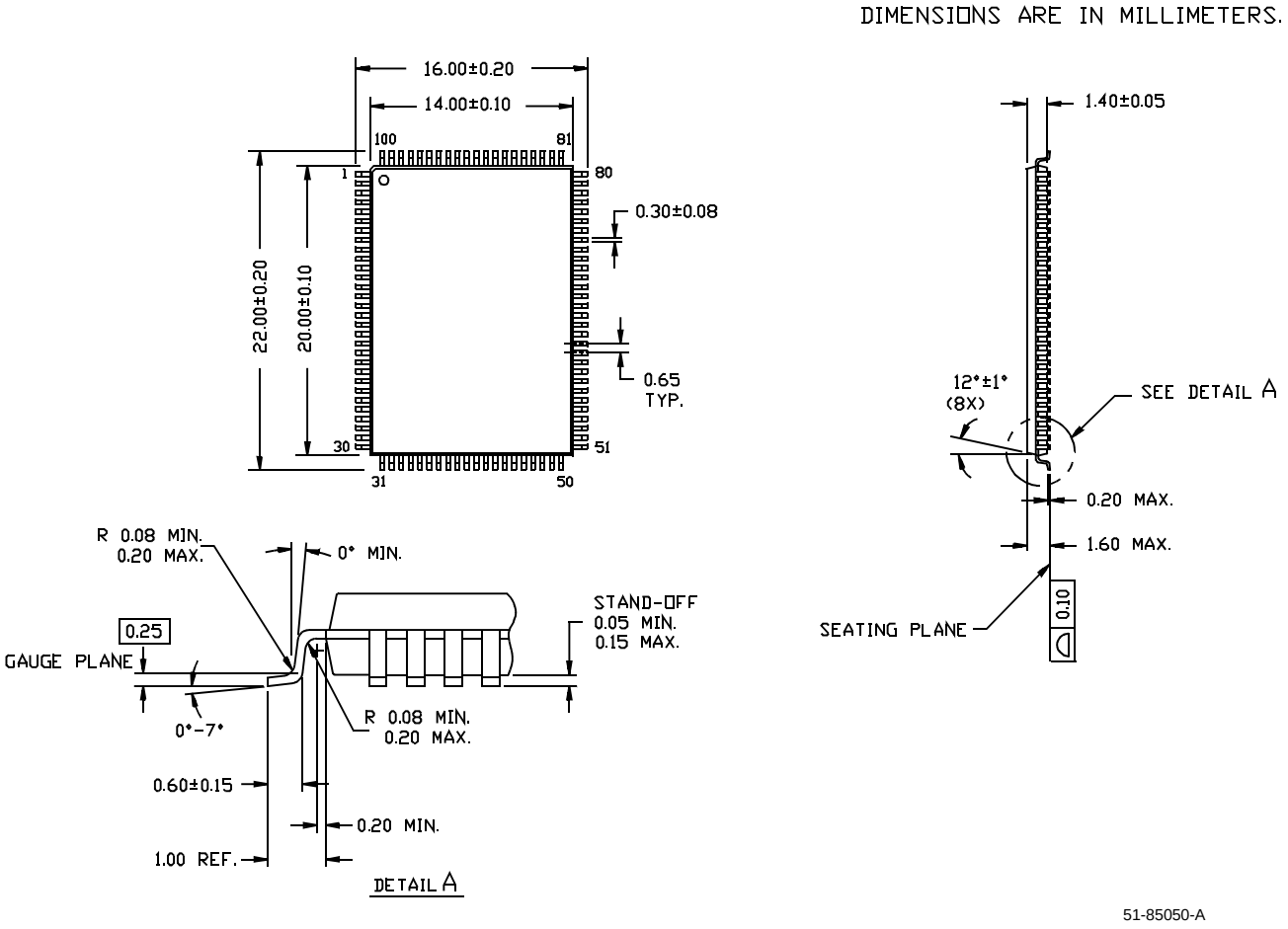


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1358A-133AC/ GVT7164T18T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
100	CY7C1358A-100AC/ GVT7164T18T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
83	CY7C1358A-83AC/ GVT7164T18T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
75	CY7C1358A-75AC/ GVT7164T18T-7	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-A

Revision History

Document Title: CY7C1358A/GVT7164T18 64K x 18 Synchronous Cache Tag RAM Pipelined Output Document Number: 38-05121				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	108312	09/25/01	BRI	New Cypress spec—converted from Galvantech format.
*A	123150	01/19/03	RBI	Updated power-up requirements in Operating Range and in AC Test Loads and Waveforms