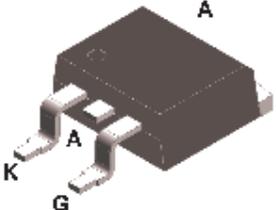
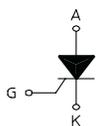


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<p>D²PAK</p>  	<table style="width: 100%; border: none;"> <tr> <td style="text-align: center;">On-State Current</td> <td style="text-align: center;">Gate Trigger Current</td> </tr> <tr> <td style="text-align: center;">12 Amp</td> <td style="text-align: center;">2 mA to 15 mA</td> </tr> <tr> <td colspan="2" style="text-align: center;">Off-State Voltage</td> </tr> <tr> <td colspan="2" style="text-align: center;">200 V ÷ 800 V</td> </tr> </table> <p>These series of Silicon Controlled Rectifier use a high performance PNP technology.</p> <p>These parts are intended for general purpose applications where high gate sensitivity is required.</p>	On-State Current	Gate Trigger Current	12 Amp	2 mA to 15 mA	Off-State Voltage		200 V ÷ 800 V	
On-State Current	Gate Trigger Current								
12 Amp	2 mA to 15 mA								
Off-State Voltage									
200 V ÷ 800 V									

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 110\text{ °C}$	12	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $\Theta = 180\text{ °}$, $T_c = 110\text{ °C}$	8	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	154	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	140	A
I^2t	Fusing Current	$t_p = 10\text{ms}$, Half Cycle	98	A ² s
I_{GM}	Peak Gate Current	20 μs max.	4	A
P_{GM}	Peak Gate Dissipation	20 μs max.	10	W
$P_{G(AV)}$	Gate Dissipation	20ms max.	1	W
T_j	Operating Temperature		(-40 to +125)	°C
T_{stg}	Storage Temperature		(-40 to +150)	°C
T_{sld}	Soldering Temperature	10s max.	260	°C
V_{RGM}	Reverse Gate Voltage		5	V

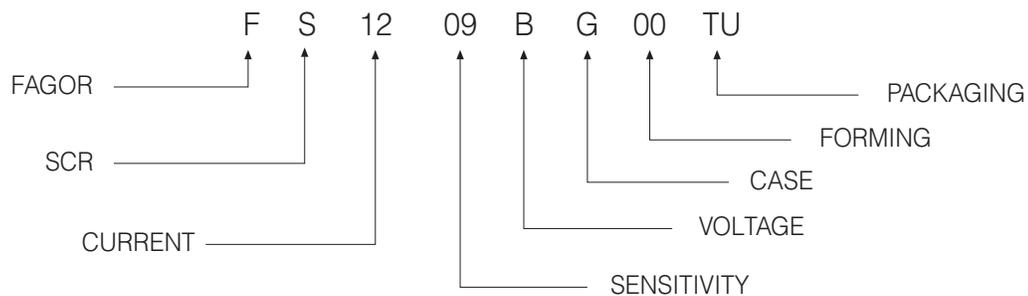
SYMBOL	PARAMETER	CONDITIONS	VOLTAGE					Unit
			B	D	M	S	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1\text{ k}\Omega$	200	400	600	700	800	V

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Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	SENSITIVITY		Uni
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MIN MAX	09 2 15	m A
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MAX	1.3	V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3k\Omega, R_{GK} = 220\Omega, T_j = 125^\circ C$	MIN	0.2	V
I_H	Holding Current	$I_T = 500 \text{ mA}$	MAX	20	mA
I_L	Latching Current	$I_G = 1.2 I_{GT}$	MAX	40	mA
dV / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open}, T_j = 125^\circ C$	MIN	200	V/ μ s
dI / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, tr \leq 100 \text{ ns}, f = 60 \text{ Hz}, T_j = 125^\circ C$	MIN	50	A/ μ s
V_{TM}	On-state Voltage	at $I_T = 24 \text{ Amp}, tp = 380 \mu\text{s}, T_j = 25^\circ C$	MAX	1.6	V
$V_{t(o)}$	Threshold Voltage	$T_j = 125^\circ C$	MAX	0.85	V
r_d	Dynamic resistance	$T_j = 125^\circ C$	MAX	32	$m\Omega$
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, R_{GK} = 1k\Omega, V_R = V_{RRM}, T_j = 125^\circ C, T_j = 25^\circ C$	MAX MAX	2 5	mA μ A
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC	for AC 360° conduction angle		1.3	$^\circ C/W$
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S = 1 \text{ cm}^2$		45	$^\circ C/W$

PART NUMBER INFORMATION



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Fig. 1: Maximum average power dissipation versus average on-state current.

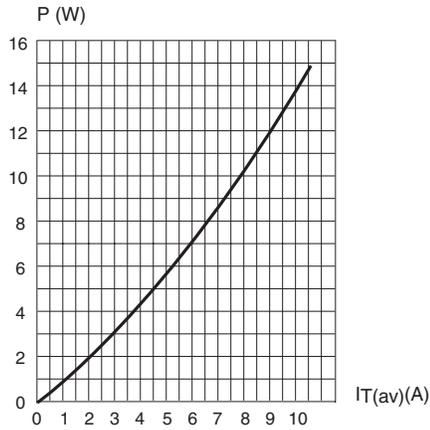


Fig. 2: Average and D.C. on-state current versus case temperature.

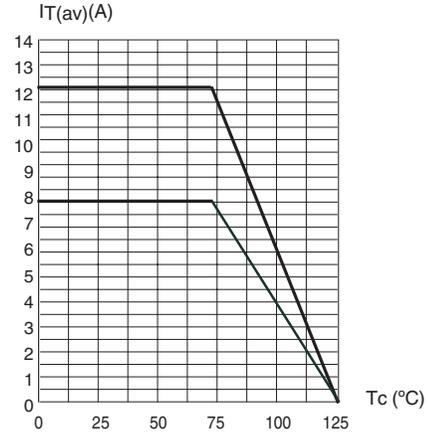


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

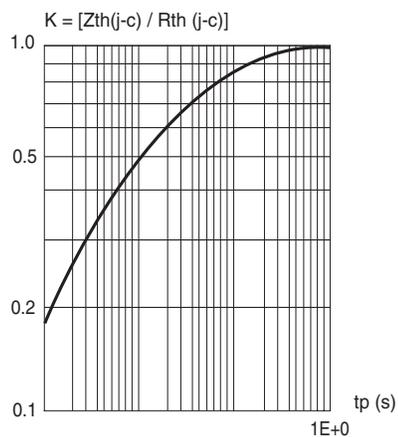


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

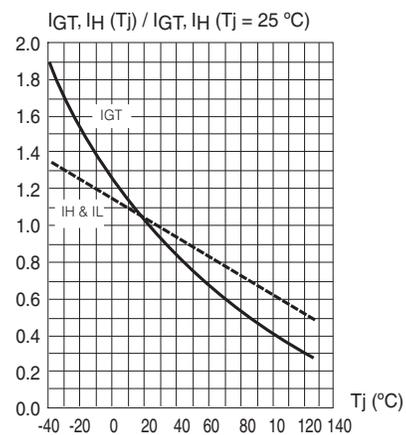


Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

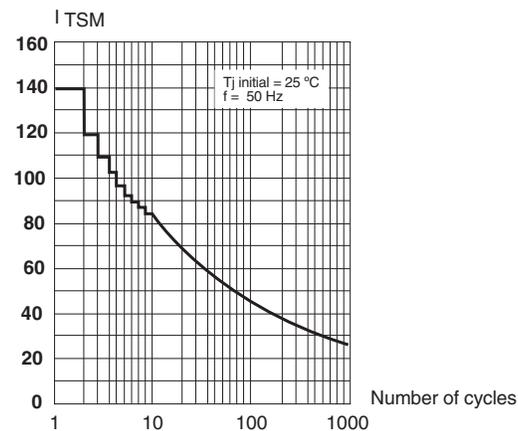
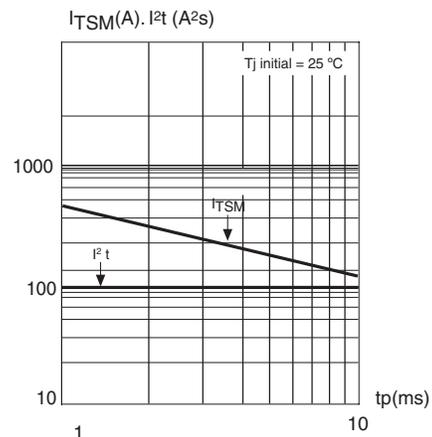


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10 \text{ ms}$, and corresponding value of I^2t .



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Fig. 7: On-state characteristics (maximum values).

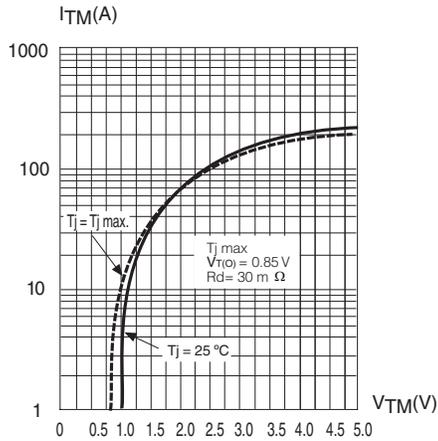


Fig. 8: D²PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm), full cycle.

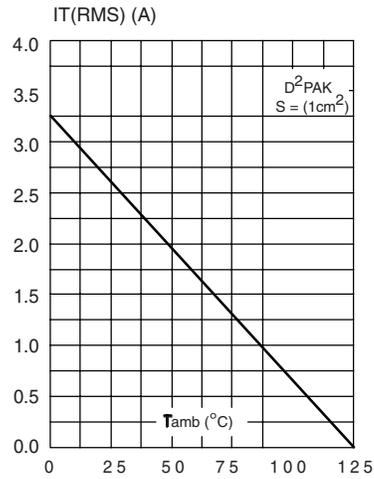
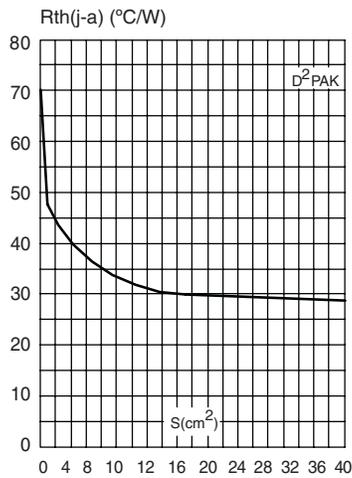
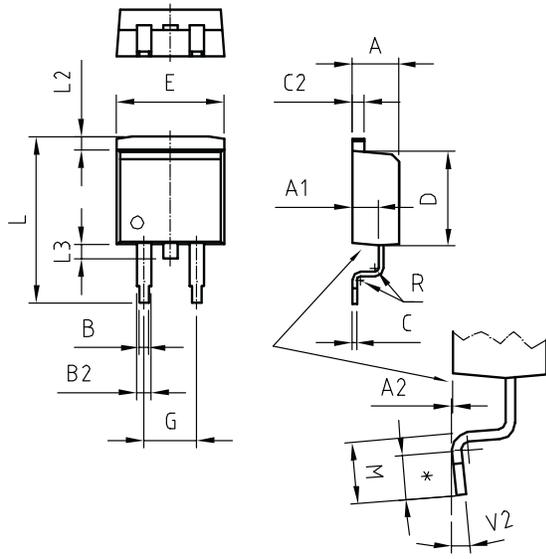


Fig. 9: D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FRA, copper thickness: 35µm).

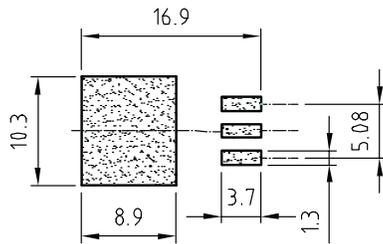


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PACKAGE MECHANICAL DATA D²PAK



* FLAT ZONE NO LESS THAN 2mm



REF.	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A	4.40	4.45	4.60
A1	2.49	2.50	2.69
A2	0.03	0.10	0.23
B	0.70	0.90	0.93
B2	1.14	1.03	1.70
C	0.45	0.45	0.60
C2	1.23	1.23	1.36
D	8.95	9.00	9.35
E	10.00	10.25	10.40
G	4.88	5.15	5.28
L	15.00	15.40	15.85
L2	1.27	1.27	1.40
L3	1.40	1.55	1.75
M	2.40	3.00	3.20
R	0.40 typ.		
V2	0°		8°

NOTE: LIMITING VALUES AND LIFE SUPPORT APPLICATIONS (SEE WEB PAGE).