HARRIS SEMICONDUCTOR

HMP8201

June 1997

Audio Link Processor

Features

- Performs ITU G.711, G.722, and G.728 Audio Compression for H.320 Video Conferencing
- Provides Sub-Band Acoustic Echo Cancellation to Support High Quality Video Teleconference Audio and Speaker Phone Interfaces
- PCI 2.1 Compliant Interface
- Glueless Interface to Industry Standard Audio Codec (CS4231A, AD1845)
- Glueless Interface to Harris Video Codec (HMP8364)
- I^2C Bus Master Port
- Plug and Play Support
- Complete H.320 Reference Design Available
- 3.3V Operation with 5V Tolerant Inputs
- 208 Lead PQFP Package

Applications

- ITU H.320 Video Conferencing
- Audio Processing for Speaker Phone Applications
- Multimedia PC Applications
- Related Products
  - H.261 Video Codec: HMP8364
  - NTSC/PAL Video Decoder: HMP8112
  - NTSC/PAL Video Encoder: HMP8156
  - H.320 Video Conferencing Reference Design

Description

The Harris Audio Link Processor (ALP) combines high performance audio processing with a PCI bus interface to support implementation of ITU H.320 Video Conferencing using the Harris Video Conferencing Chipset.

The ALP provides a complete solution for the audio layer of ITU H.320. The audio processing includes full duplex implementations of ITU G.711, G.722 and G.728 audio compression, with wideband and narrowband acoustic echo cancellation to enable the use of a “hands free” speaker phone type interface.

In addition to audio processing the ALP provides a PCI interface to manage data flows between the host and the Harris Video Conferencing chipset. The PCI interface supports control and data flows between the host system and the H.261 Video Codec, the audio codec, the video encoder/decoder, and the ISDN modem. As shown in the block diagram, these data flows are routed to the various ICs via an I^2C bus, an 8-bit general purpose I/O bus, a telecom interface supporting the MVIP or IOM2 standards, and buses for compressed and uncompressed video.

Additional information on register programming and software support may be obtained in the accompanying programming and technical reference manual for the HMP8201 and the Harris Reference Design.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HMP8201CN	0 to 70	208 Ld PQFP (Note)	Q208.28x28

NOTE: PQFP is also known as QFP and MQFP.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 4285.2

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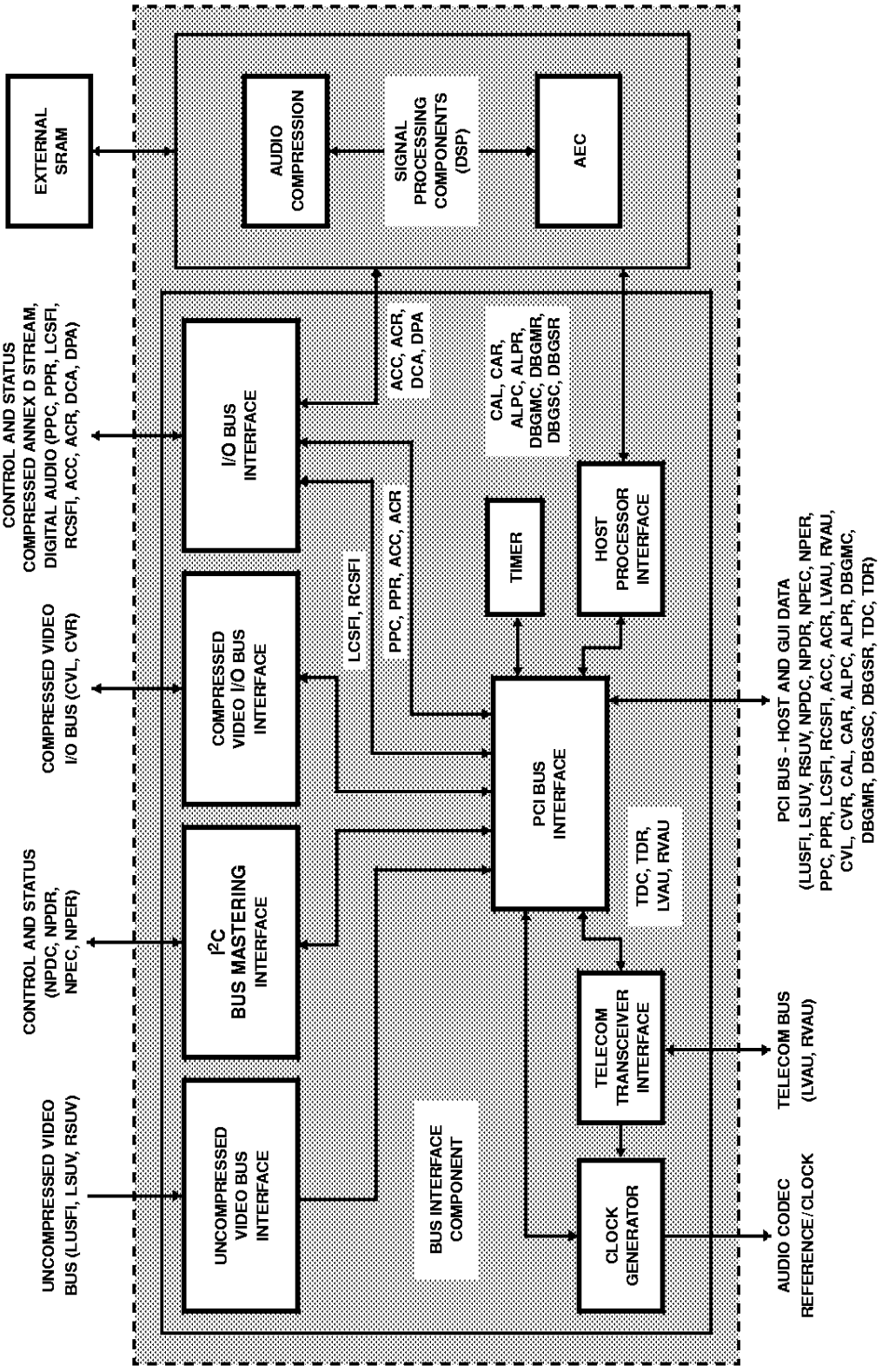
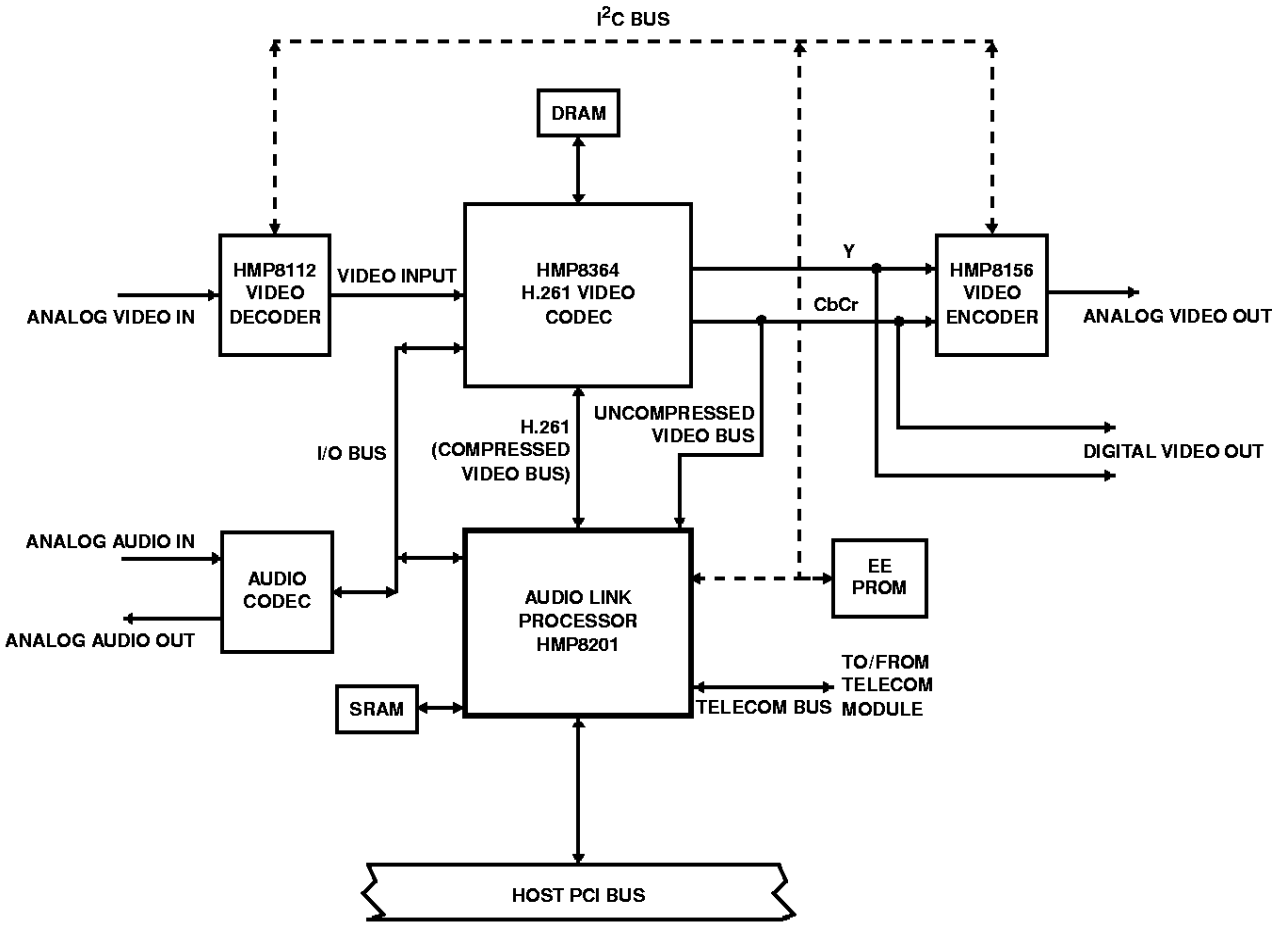
Functional Block Diagram



Target Application - PC Based H-320 Video Teleconferencing



Introduction

The Harris Audio Link Processor (ALP) combines flexible audio processing capabilities with sophisticated PCI bus interface functions to support implementation of the International Telecommunications Union (ITU) H.320 videoconferencing recommendation. The ALP provides a complete solution for the audio (ITU G.7xx) layers of ITU H.320. In addition, it includes an sub-band based acoustic echo cancellation (AEC) algorithm that greatly reduces annoying speech echo during full duplex audio communication.

The ALP utilizes digital signal processor (DSP) technology to execute the H.320 audio layer. The audio capabilities include: full duplex implementations of ITU G.711, G.722 and G.728 and acoustic echo cancellation with noise cancellation. The transport layer is an host implementation of ITU H.221, which requires interfaces to the H.261 video compression chip and the telecom communications channel. In addition, the DSP provides host processor communications via the PCI bus and hardware I/O control and data flow functions for external audio codecs.

The ALP also provides PCI bus interface functions to support ITU H.320 implementation. The ALP provides a "gateway" to the PCI bus for the devices used in implementing the video, audio and transport layers of the ITU H.320 standard.

To this end, the ALP supports these PCI bus interfaces: the 8-bit digital video input bus (uncompressed video data), a compressed video bus (H.261), an 8-bit general purpose bus (control and status, compressed H.yyy Annex D data streams, and digital audio), Telecom communication channel time-division multiplexed bus (MVIP or IOM2), the serial I^2C bus (control and status), and to the on-chip DSP core (host processor communications.

NOTE: This document describes the ALP hardware. In order to function, the hardware is designed to work with host software and downloadable DSP microcode. In some sections of this document, descriptions and statements will imply that the host software and downloadable DSP microcode are an integral part of the ALP subsystem.

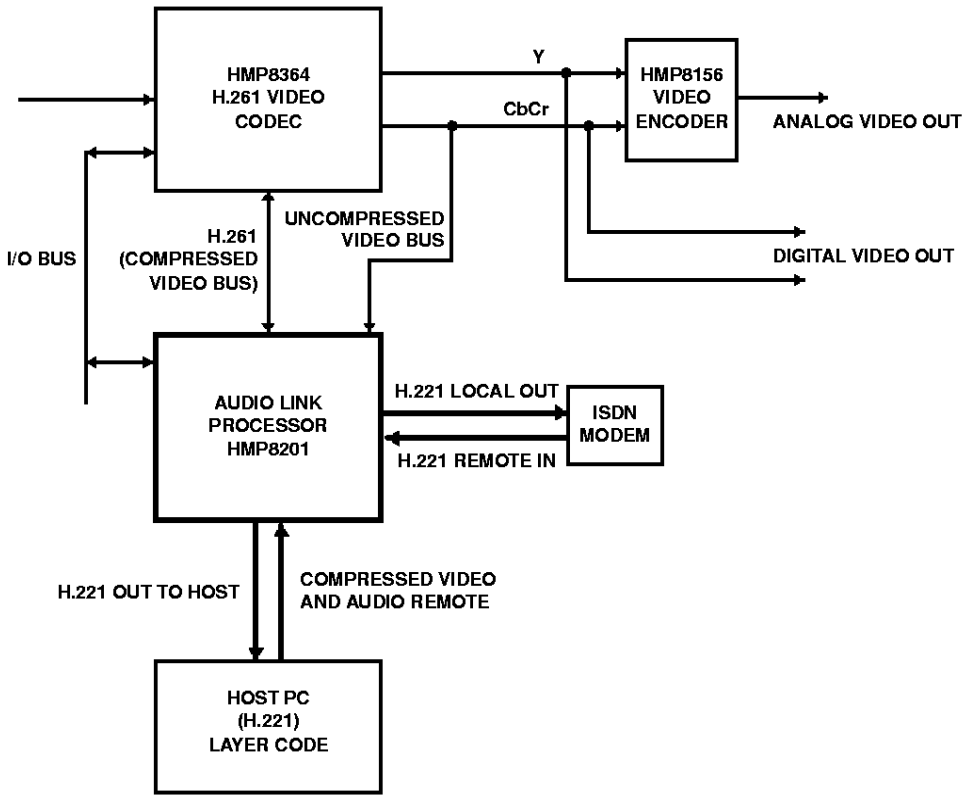


FIGURE 1.

Audio Compression

The full duplex implementations of ITU G.711, G.722, and G.728 audio compression run in the embedded Digital Signal Processors (DSPs) in the ALP. Linear audio samples from the audio codec are input through the I/O bus and then subsequently processed. G.711 implements A-Law or u-Law companding which provides a compression ratio of 1.6. G.711 performs a logarithmic quantization on signals with a 4kHz bandwidth falls into the waveform coding class of audio compression techniques. Waveform coders work equally well compressing music or speech. G.722, which is also a form of waveform coding, implements Sub-Band ADPCM which provides a higher compression ratio (3.5) and wider audio bandwidth (8kHz) then G.711. Finally, G.728 implements Low Delay Code Excited Linear Predictive coding (LD-CELP), which is a form of speech coding. Speech coders provide the highest amount of compression on signals that are primarily speech. G.728 provides a compression ratio of 6.5 and outputs a signal with a 4kHz bandwidth.

Acoustic Echo Cancellation

The ALP implements a proprietary, sub-band based AEC technique that was developed by PictureTel Corp. This technique is similar to PictureTel's Integrated Dynamic Echo Canceller II (IDEC II) technique which has been shown to be superior to other AEC techniques. The AEC algorithm runs on the DSP core in the ALP. The AEC function has two modes of operation, wide and narrow band. It may be selectively disabled by the user (for simplex communication or in excessively noisy environments). Additionally, noise suppression is included with this AEC algorithm.

PCI Interface

The PCI Interface provides a gateway through which video teleconferencing data and control are passed between a host computer and PCMS chip set. The ALP supports little endian transfers and conforms to the PCI 2.1 specification. The PCI Interface provides two sets of register address spaces which are visible on the PCI bus.

The first register set is used to configure the ALP for PCI operation and includes the registers required for plug-and-play compatibility. This conforms to the 256 byte Configuration Space specification as defined in the PCI 2.1 specification. The first 16 bytes of this configuration space represent a universal, read only header whose content is set by ROM on the ALP. User specific vendor information is loaded into the Subsystem registers from an external serial I^2C EEPROM. Access to this configuration space is generally restricted to the host operating system.

The second register set, which supports doubleword transfers only, is used to provide control, status, and data transfer information associated with the PCMS chip set operation. At boot up, the host allocates a 4096 byte block of PCI register space for this second register set.

In some cases, the host computer performs the data transfer and the ALP acts as a PCI bus target. In other cases, the

ALP acts as a PCI master to transfer the data; these are listed below:

As a bus target, the ALP responds to the following types of data transfers:

- I^2C Master Read data transfer
- I^2C Master Write data transfer
- I/O Bus Read and Write transfers
- Mailbox FIFO data transfers with the embedded DSP cores
- Timer Control

As a bus master, the ALP can initiate the following types of data transfer:

- Telecom H.221 transmit data transfer
- Telecom H.221 receive data transfer
- Uncompressed Video (UCV) receive
- Compressed Video Local (CVL) transfer
- Compressed Video Remote(CVR) transfer
- Compressed Audio Local (CAL) transfer
- Compressed Audio Remote (CAR) transfer

Further details (such as register details) can be found in the Programming and Applications Reference for the Audio Link Processor.

Uncompressed Video Interface (UVI)

The ALP provides an Uncompressed Video Interface to receive both the local and remote uncompressed video streams from the Px64 chip. The video frames from each source are interleaved and sent to the ALP at an average rate of 30 frames/sec. This interface also supports still frame capture to implement Annex D mode. The ALP acts as a PCI master to transfer the received video streams to a target GUI/host via the PCI interface.

Uncompressed Video Bus (UVB)

The ALP provides an Uncompressed Video Bus (UVB) capable of receiving video data from the Px64 chip at a sustained rate of 20.25MBytes/s. Refer to page xx for signal definitions of the UVB. These signals include an 8-bit data bus, UVB[7:0], a vertical sync, VSYNC, a data valid, UVRDY, and a field indicator, FIELD. SYSCLK is used for the bus clock.

A more complete discussion of the UV interface is contained in the HMP8364 data sheet.

UVB Transfer Protocol

The ALP will use the rising edge of SYSCLK to clock in video data when UVRDY is high.

Data Transfers Between UVB and PCI

The ALP functions as a PCI master to transfer two streams of uncompressed video data received on the UVB to the PCI bus. These transfers are controlled by a block of 32-bit registers in the Video Channel portion of the PCI Control/Status Register block. The ALP provides the following basic functionality:

a) UVB FIFO

b) Four buffer address registers (2 even/2 odd)

c) Two registers for controlling the gap between video lines (even/odd)

d) Two registers for controlling the dropping of video fields (even/odd)

e) Two lines per field counters and controls (even/odd)

f) Two pixels per line counters and controls (even/odd)

g) Two RGB Alpha fill registers (even/odd)

h) Controls for even/odd fields for overflow handling, Alpha mode enable, field capture mode and buffer enable.

i) Status for even/odd fields reflecting buffer and FIFO conditions and current buffer transfer state.

j) Control for the size of PCI Bus block transfers (0 to 64 double words).

Compressed Video Interface

The ALP provides a Compressed Video Interface through which data is transferred between the Host and the Px64 chip. This interface function converts ALP-Px64 data transfers over the Compressed Video Bus to ALP-Host transfers over the PCI bus, and converts Host-ALP transfers on the PCL bus to ALP-Px64 transfers on the compressed video bus. The ALP acts as master for transfers over both the PCI and Compressed Video Bus.

Compressed Video Bus (CVB)

The ALP provides a 5-wire CVB capable of transferring serially at rates up to 384kbits/s. These signals include a serial data clock, CVCLK, remote and local compressed video lines, CVR and CVL, and I/O data gates, CVGTR and CVGTL. The signal interface is depicted in Figure 2.

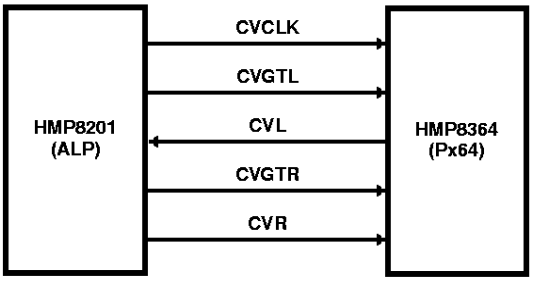


FIGURE 2. COMPRESSED VIDEO BUS SIGNALS

CVL/CVR Data Transfer Over CVB

The signaling protocol required to effect a master read compressed video data transfer is shown in Figure 3. The master uses the falling edge of CVCLK to latch in data when CVGTL is high. The corresponding master write is illustrated in Figure 4. The slave uses the falling edge of CVCLK to latch in data when CVGTR is high.

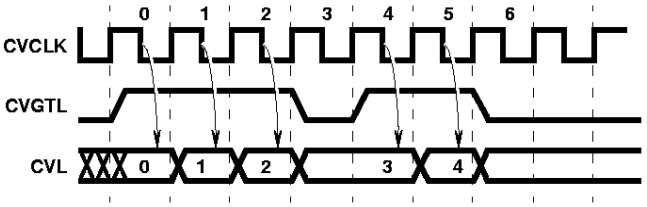


FIGURE 3. CVB MASTER READ

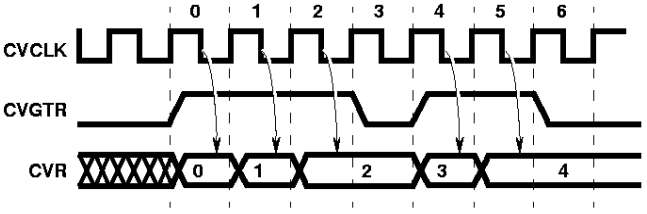


FIGURE 4. CVB MASTER WRITE

The source for the compressed video clock, CVCLK, is the Local Reference NCO. The CVCLK frequency is typically 2.048MHz. The gating signals are generated by the carry out of programmable NCOs. The gating signal frequency is set by loading the CVL and CVR Bit Rate Control Registers (see Section 3.1.2.7.3). The bit rate across the CVB is determined by the frequency with which the gating signals are asserted, and it is bounded at the upper end by the frequency of CVCLK (2.048MHz). Figure 5 depicts how the audio codec reference and Telecom signals are created and selected. Note: the gating signals are asserted synchronous with CVCLK.

The number of bits allocated to video in the H.221 multi frame sets the required bit rate over the CVB. Since the number of bits allocated to video in the H.221 frame can be variable over the course of a call, the host will update the Bit Rate Control registers to match changing bandwidth allocations for video in either the local or remote direction. The Px64 adapts compression to changes in bit rate based on the flow of data to and from its internal CVL and CVR buffers.

CVL/CVR Data Transfer Over PCI

The ALP acts as a PCI master to read CVR data and write CVL data to ping-pong buffers using a protocol similar to that used for CAR and CAL data. The CVR transfers are controlled by a PCI based register set that mirrors the CAR registers in functionary. Similarly, the CVL transfers are controlled by a registers that mirrors the CAL registers.

Telecom Interface and Signals

The ALP provides a five-wire Telecom interface through which H.221 data transfers occur with the system ISDN modem. This interface is compatible with ISDN modems using either a MVIP (Multi Vendor Integration Protocol) in the US or IOM-2 type interface (this consists of the combination of the GCI line card interface standard and the Special Circuit Interface T standard) in Europe and elsewhere.

The local and remote H.221 data streams are transferred directly through this interface from/to the host PCI bus. The maximum sustainable data rate through this interface is 128kbits/s.

This interface consists of the five signal lines which include a serial data clock (DCL) which runs at twice the data rate, a serial data input (DI), a serial data out put (DO), a frame sync (FSC) which runs at 8kHz, and an output data enable ($\overline{ODE}$). The ALP sources the frame sync and data clock signals and switch the interpretation of the data in and out signals.

The ALP uses the an MVIP/IOM2 signaling convention to transfer data over the Telecom interface; it is capable of mastering the Telecom bus and functions as a PCI master to transfer H.221 data to and from the Telecom Interface. Configuration of the Telecom Interface may be done through its PCI based control register (see Section xx).

The ALP sources the frame sync and data clock signals and switch the interpretation of the data in and out signals.

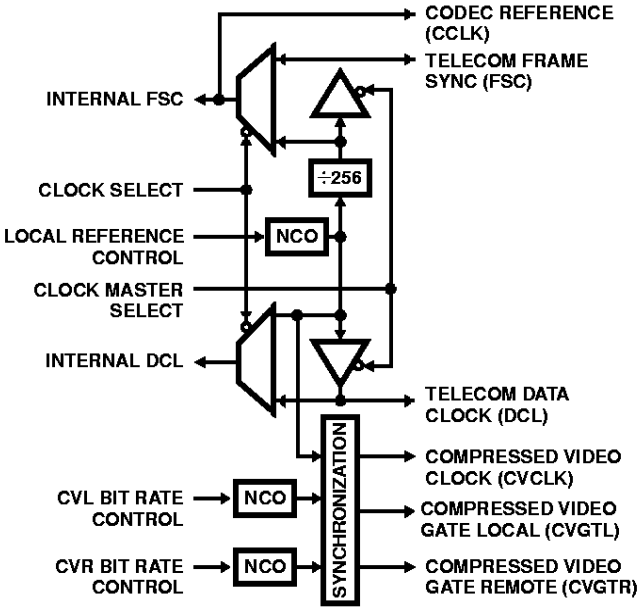


FIGURE 5. TELECOM, COMPRESSED VIDEO AND AUDIO REFERENCE CLOCK AND CONTROL

I^2C Bus Interface

The ALP provides an I^2C interface to communicate with peripheral devices such as the NTSC/PAL Encoder IC (HMP8112), the NTSC/PAL Decoder IC (HMP8115), a serial EPROM (used to upload PCI Interface configuration data), and any additional peripheral I^2C slave devices. I^2C is a two wire interface consisting of a serial clock line (SCL), and a serial data line (SDA) that can run up to up to 100 KBPS as specified in the inter-integrated circuit interface from Philips Semiconductor. The ALP only functions as an I^2C Bus Master. As a result, the ALP can only be connected to I^2C slave devices without bus contention.

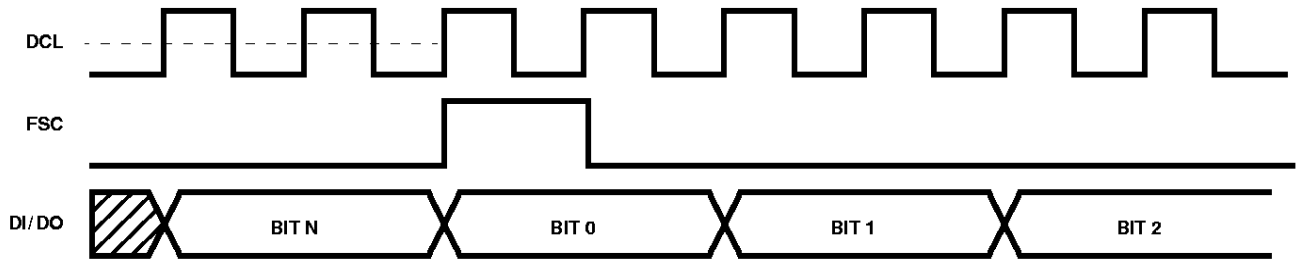


FIGURE 6. IOM-2 INTERFACE TIMING PROTOCOL

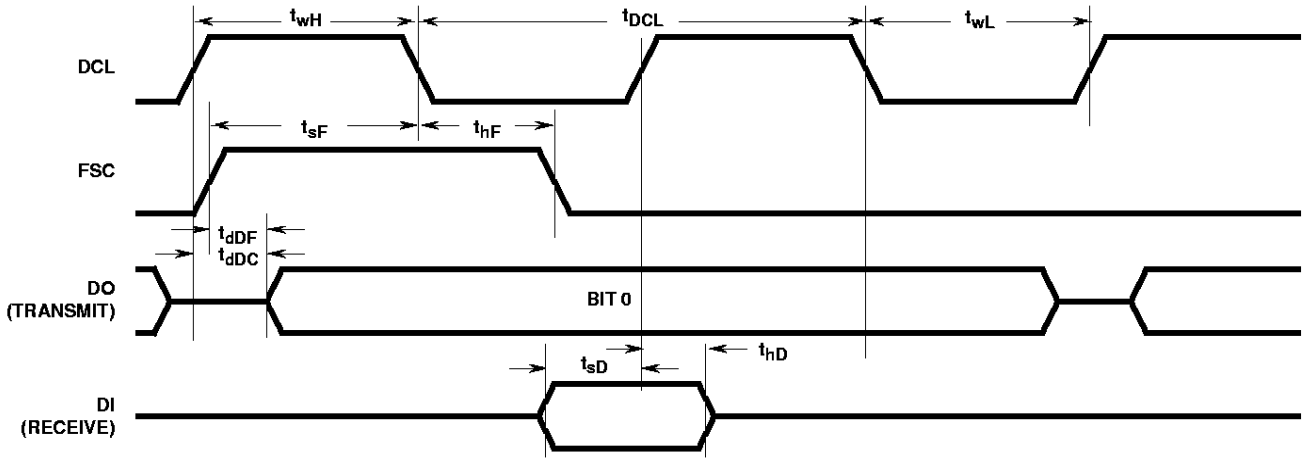


FIGURE 7. IOM-2 INTERFACE TIMING DETAILS (PER BIT)

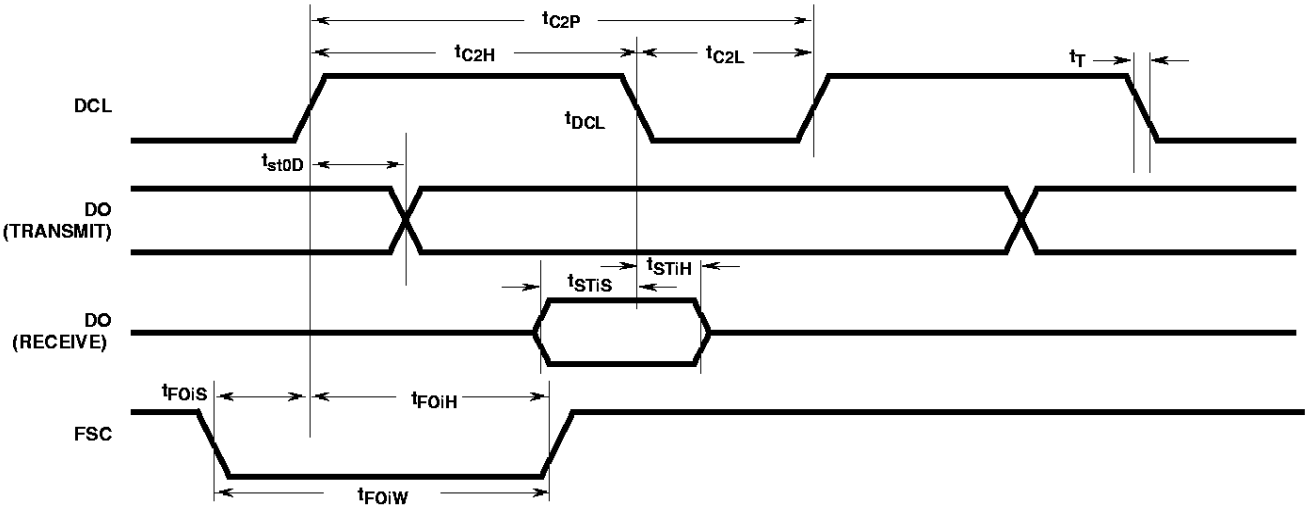


FIGURE 8. MVIP INTERFACE TIMING DETAILS (PER BIT)

PCI Configuration Via I^2C EEPROM

The ALP uploads the vendor specific information required for PCI interface configuration from an I^2C compatible serial EEPROM. The required information is 32 bits in length and represents the Subsystem Vendor ID and Subsystem ID. The ALP will read this information and load it into address 10_{16} of PCI Configuration Space (see section xx). The ALP reads the serial EEPROM and initializes the PCI Configuration Space after system reset.

I^2C EEPROM Address

The 8-bit slave address and broadcast on the I^2C bus for EEPROM read and write operations is given in Table 1. Refer to EEPROM data sheets for more information.

TABLE 1.

OPERATION	I^2C DEVICE ID	CHIP SELECT	R/W BIT
Read	10_{16}	xxx	1
Write	10_{16}	xxx	0

Data Transfers Between I^2C and PCI

Data transfers between the PCI and the ALP's I^2C bus are controlled by two PCI based I^2C control registers (refer to the programming/register reference). All I^2C operations are initiated when bit 24 of address 10_{16} is updated. The ALP will perform an I^2C master read or write depending on the value written to bit 23 of address 10_{16}. After completion of the I/O cycle, the appropriate status bits will be set.

For a detailed timing description on the I^2C bus, please refer to the Philips I^2C Specification.

I^2C Control Interface

The I^2C clock/data timing is shown in Figure 9. The HMP8112 contains 29 internal registers used to program and configure the Decoder. The I^2C control port contains a pointer register that auto-increments through the entire register space and can be written. The autoincrement pointer will wrap after the last register has been accessed (Product ID Register) and should be set to the desired starting address each time an access is started. For a write transfer, the I^2C device base address is the first part of a serial transfer. Then the internal register pointer is loaded. Then a series of registers can be written. If multiple registers are written, the pointer register will autoincrement up through the register address space. A stop cycle is used to end the transfer after the desired number of registers are programmed.

For a read transfer, the I^2C device address is the first part of the serial transfer. Then the internal register pointer is loaded. At this point another start cycle is initiated to access the individual registers. Multiple registers can be read and the pointer register will autoincrement up through the pointer register address space. On the last data read, an acknowledge should not be issued. A stop cycle is used to end the transfer after the desired number of registers are read.

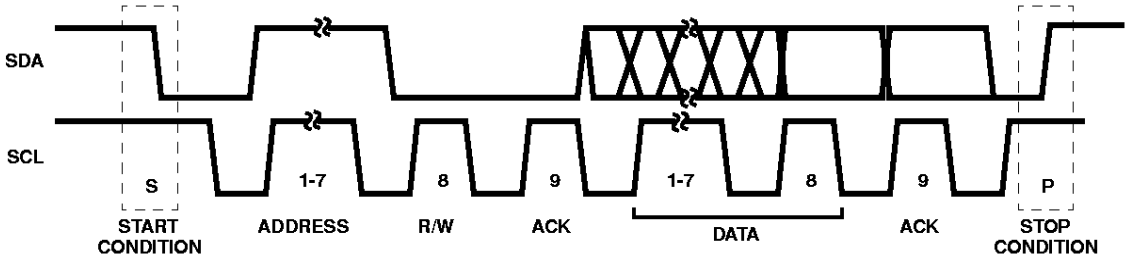
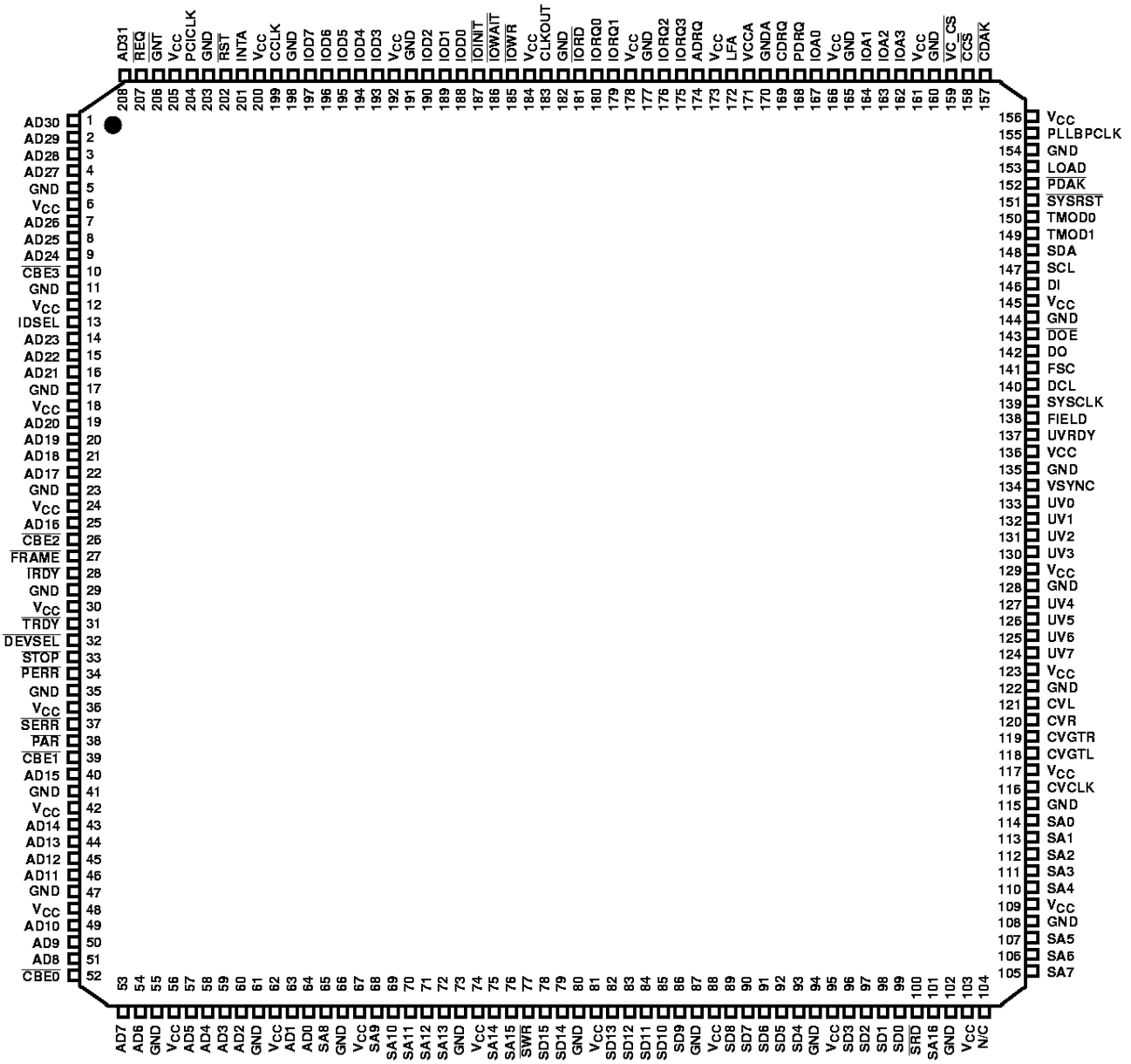


FIGURE 9. I^2C SERIAL TIMING FLOW

Pinout

HMP8201
(MQFP/PQFP)
TOP VIEW



Pin Description

NAME	PQFP PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
PCI INTERFACE (50 Pins, 4 In, 2 Out, 44 I/O)			
AD[31:0]	208, 1-4, 7-9, 14-16, 19-22, 25, 40, 43-46, 49-51, 53-54, 57-60, 63-64	I/O	PCI Address/Data Bus. Address and Data are multiplexed over this bus. A bus transaction consists of an address transfer followed by one or more data transfers. (Three-State I/O pins)
$\overline{\text{CBE}}$[3:0]	10, 26, 39, 52	I/O	Bus Command/Byte Enable. Defines bus command during address transfer. Defines which byte lanes are valid during data transfers. (Three-State I/O pins)
PAR	38	I/O	Parity. Set for even parity across AD[31:0] and $\overline{\text{CBE}}$[3:0]. The bus master sets PAR during address and write data phases. Target sets PAR during read data phases. (Three-State I/O pins)
$\overline{\text{FRAME}}$	27	I/O	Frame. This active low signal is asserted by the current bus master to indicate the beginning and duration of a bus transaction. (Sustained Three-State pin)
$\overline{\text{TRDY}}$	31	I/O	Target Ready. This active low signal indicates the target device's ability to complete the data phase of the transaction. (Sustained Three-State pin)
$\overline{\text{IRDY}}$	28	I/O	Initiator Ready. This active low signal indicates the Initiator's ability to complete the current data phase of the transaction. (Sustained Three-State pin)
$\overline{\text{STOP}}$	33	I/O	Stop. The current target asserts this signal low to stop the current transaction. (Sustained Three-State pin)
$\overline{\text{INTA}}$	201	O	Interrupt A. This active low PCI interrupt stays asserted until serviced by host.
IDSEL	13	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
$\overline{\text{DEVSEL}}$	32	I/O	Device Select. Asserted by a device recognizing its address as the target of an access. (Sustained Three-State pin)
$\overline{\text{PERR}}$	34	I/O	Parity Error. Indicates data parity errors during all PCI transactions except a Special Cycle. (Sustained Three-State pin)
$\overline{\text{SERR}}$	37	I/O	System Error. Indicates address parity errors, data parity errors during Special Cycle command, or any other system error where the result will be catastrophic
$\overline{\text{REQ}}$	207	O	Request. Indicates to arbiter that this agent desires use of the bus. Point to point signal (Three-State)
$\overline{\text{GNT}}$	206	I	Grant. Indicates to the agent that access to the bus has been granted. (Three-State)
PCICLK	204	I	Clock. This is the PCI clock input to every device. Every signal but $\overline{\text{RST}}$, are sampled on the rising edge of CLK.
$\overline{\text{RST}}$	202	I	Reset.
I^2C INTERFACE (2 Pins, 1 Out, 1 I/O)			
SCL	147	O	I^2C Serial Clock
SDA	148	I/O	I^2C Serial Data
I/O BUS (IOB), (27 Pins, 9 IN, 10 Out, 8 I/O)			
IOD[7:0]	197-193, 190-188	I/O	I/O Data Bus. Bidirectional data bus. (Three-State)
IOA[1:0]	164, 167	O	Programmed I/O addresses[1:0]
IOA[3:2]	162-163	O	Spare address signals.

Pin Description (Continued)

NAME	PQFP PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
$\overline{VC_CS}$	159	O	Px64 Chip Select. This active low output signals the Px64 to respond to I/O Bus commands. This signal also maps to IOA[4].
$\overline{CCS}$	158	O	Audio Codec Chip Select. This active low output signals the audio codec to respond to I/O Bus commands. This signal also maps to IOA[5].
$\overline{CDAK}$	157	O	Audio Codec Capture Acknowledge. This active low output signals that the next read cycle is a DMA read from the capture FIFO. This signal also maps to IOA[6].
$\overline{PDAK}$	152	O	Audio codec Playback Acknowledge. This active low output signals that the next write cycle is a DMA write to the playback FIFO. This signal also maps to IOA[7].
$\overline{IORD}$	181	O	I/O Read Strobe. This active low output defines an I/O Bus read cycle.
$\overline{IOWR}$	185	O	I/O Write Strobe. This active low output defines an I/O Bus write cycle.
$\overline{IOWAIT}$	186	I	I/O Wait. The target can extend the read or write by driving this input low after the assertion of either $\overline{IOWR}$ or $\overline{IORD}$. (Three-State).
$\overline{IOINT}$	187	I	I/O Bus Interrupt. Asserted by other components on IOB to initiate a PCI interrupt. Note: open drain input; external pull up required.
IORQ[3:0]	175-176, 179-180	I	Spare request signals (active high).
ADRQ	174	I	Px64 Data Request. This active high input signals that the Px64 chip requires an Annex D data transfer. This signal also maps to IORQ4.
CDRQ	169	I	Audio codec Capture Request. This active high input signals that the audio codec has at least one sample captured. This signal also maps to IORQ5.
PDRQ	168	I	Audio codec Playback Request. This active high input signals that the audio codec has room for at least one playback sample. This signal also maps to IORQ6.
TELECOM INTERFACE (5 Pins, 1 In, 2 Out, 2 I/O)			
DI	146	I	Serial Data Input. Serial data input from ISDN Modem. Synchronous to DCL.
DO	142	O	Serial Data Output. Serial data output to ISDN Modem. Synchronous to DCL.
DCL	140	I/O	Serial Data Clock. In systems using the MVIP interface this line would be tied to the C2 output which is a 2.048MHz clock synchronous to the bit rate. In systems using the IOM-2 modem interface, this signal would be tied to the DCL output which is synchronous to twice the bit rate, and is programmable in 64kHz steps from 512kHz to 4096kHz.
FSC	141	I/O	Frame Sync. This signal is an 8kHz sync indicating the start of a frame. Normally, this is generated by upstream device (tel-co). For test purposes, this sync may be locally generated and output from the ALP. This signal also serves as the audio sample rate reference to the audio codec.
$\overline{DOE}$	143	O	Data Output Enable. This active low output is asserted during an outgoing data transmission.
COMPRESSED VIDEO BUS (5 Pins, 1 In, 4 Out, 0 I/O)			
CVCLK	116	O	Compressed Video Clock.
CVGTL	118	O	Compressed Video Gate Local. This active high signal enables CVCLK to clock compressed video bits out of the Px64 chip.
CVL	121	I	Compressed Video Local. This is the serial input for compressed video. The bit value at this input is sampled by the falling edge of CVCLK when CVGTL is asserted.
CVGTR	119	O	Compressed Video Gate Remote. This active high signal is asserted simultaneously with data bits clocked out of CVR by CVCLK.

Pin Description (Continued)

NAME	PQFP PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
CVR	120	O	Compressed Video Remote. Compressed video data is serially clocked through this output at the rising edge of CVCLK.
UNCOMPRESSED VIDEO BUS (11 Pins, 11 In, 0 Out, 0 I/O)			
UV[7:0]	124-127, 130-133	I	Uncompressed Video. Uncompressed video from H.261 processor. Data on this bus is clocked into the ALP by the rising edge of SYSCLK when UVRDY is asserted.
VSYNC	134	I	Vertical Sync. This signal indicates the beginning of a new video field.
UVRDY	137	I	Uncompressed Video Ready. This active high input indicates that data present on UV[7:0] is valid.
FIELD	138	I	Video Field. The sense of this signal indicates whether an even or odd video field is currently being transferred (0 = even, 1 = odd). The state of this input is held constant through out the duration of the field transfer.
MISCELLANEOUS (9 Pins, 6 In, 3 Out, 0 I/O)			
SYSCLK	139	I	CLOCK. Video teleconferencing system clock. Typically 27MHz.
$\overline{\text{SYSRST}}$	151	O	Reset. This active low output echoes a PCI reset.
CLKOUT	183	O	DSP Processor clock. 40.5MHz output of PLL.
PLLBPCLK	155	I	External Test Clock Input.
CCLK	199	O	Codec clock. Audio reference (8kHz).
TMOD[1:0]	149-150	I	Test Mode. Selects one of three test modes. "00" = normal operation; “02” = PLL bypass.
LOAD	153	I	Boot Select. 0 loads from host, 1 loads from CDI.
LFA	172	I	Loop Filter Input. This pin is tied to ground via lump components required to control PLL Loop Filter bandwidth.
SRAM INTERFACE (35 Pins, 0 In, 19 Out, 16 I/O)			
SD[15:0]	78-79, 82-86, 89-93, 96-99		SRAM Data Bus. Bidirectional data bus.
SA[16:0]	101, 76-75, 72-68, 65, 105-107, 110-114		SRAM Address Bus. Note: SA16 allows paging of 128 kwords of external RAM, which is not required by the current firmware.
$\overline{\text{SRD}}$	100		SRAM Read Strobe. This active low output defines an SRAM read cycle.
$\overline{\text{SWR}}$	77		SRAM Write Strobe. This active low output defines an SRAM write cycle.
SUPPLY (63 Pins, 31 V_{CC}, 30 GND)			
V_{CC}		I	3.3V Digital Supply.
$V_{CC}A$		I	3.3V Analog Supply for PLL circuit.
GND		O	Digital Ground.
GNDA		O	Analog Ground for PLL circuit.

Absolute Maximum Ratings

Digital Supply Voltage (V_{CC} to DGND) 4.0V
Digital Input Voltages . . . . . GND -0.5V to V_{CC} 0.5V
ESD Classification . . . . . Class 1

Operating Temperature Range

HMP8201CN . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PQFP Package 32
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board

Electrical Specifications V_{CC} = 3.3V ±9%, T_A = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HMP8201			UNITS
			MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS						
Power Supply Voltage Range	DV_{CC}, AV_{CC}	Note 2	3.00	3.30	3.60	V
Power Supply Current	Digital I_{CCOP}	f_{SYSCLK} = 27MHz, f_{PCICLK} = 33MHz, DV_{CC} = 3.60V, Outputs Not Loaded	-	XXX	XXX	mA
	Analog I_{CAOP}	f_{SYSCLK} = 27MHz, AV_{CC} = 3.60V	-	XX	XX	mA
Total Power Dissipation	P_{TOT}	f_{SYSCLK} = 27MHz, f_{PCICLK} = 33MHz, DV_{CC} = AV_{CC} = 3.60V, Outputs Not Loaded	-	X.XX	X.XX	W
DIGITAL I/O						
Input Logic High Voltage	V_{IH}	DV_{CC} = Max	0.7xV_{CC} (2.52)	-	-	V
Input Logic Low Voltage	V_{IL}	DV_{CC} = Min	-	-	0.3xV_{CC} (0.9)	V
Input Leakage Current (High)	I_{IH}	DV_{CC} = Max, Input = DV_{CC} Note 4	-10	-	10	µA
Input Leakage Current (Low)	I_{IL}	DV_{CC} = Max, Input = 0V Note 4	-10	-	10	µA
Input/Output Capacitance	C_{IN}	CLK Frequency = 1MHz, Note 2, All Measurements Referenced to Ground T_A = 25°C	-	-	10	pF
Rise/Fall Time	t_r, t_f	Note 2	-	-	2.0	ns
Output Logic High Voltage	V_{OH}	I_{OH} = -400µA, DV_{CC} = Max	V_{CC} - 0.4	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 800µA, DV_{CC} = Min		-	0.4V	V

Electrical Specifications V_{CC} = 3.3V ±9%, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HMP8201 MIN	HMP8201 TYP	HMP8201 MAX	UNITS
PCI DIGITAL I/O						
PCI Bus Clock Frequency	CLK	Note 2	0	33	33	MHz
Clock Cycle Time	CLK		30	-	-	ns
Clock Waveform Symmetry			40	-	60	%
Clock Pulse Width High	t_{PWH}		12	-	-	ns
Clock Pulse Width Low	t_{PWL}		12	-	-	ns
Input Logic High Voltage	V_{IH}	DV_{CC} = Max	0.5*V_{CC}	-	V_{CC}+0.5	V
Input Logic Low Voltage	V_{IL}	DV_{CC} = Min	-0.5	-	0.3xV_{CC}	V
Input Leakage Current (High)	I_{IH}	DV_{CC} = Max, Input = DV_{CC} Note 2	-10	-	10	µA
Input Leakage Current (Low)	I_{IL}	DV_{CC} = Max, Input = 0V Note 2	-10	-	10	µA
Input/Output Capacitance	C_{IN}	CLK Frequency = 1MHz, All Measurements Referenced to Ground T_A = 25°C	-	8-10	-	pF
Rise/Fall Time	t_r, t_f	Note 2	-	-	2.0	ns
Output Logic High Voltage	V_{OH}	I_{OH} = -500µA, DV_{CC} = Max	0.9xV_{CC}	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 1.5mA, DV_{CC} = Min	0	-	0.1xV_{CC}	V
I^2C DIGITAL I/O (SDA, SCL, Fast Mode)						
Input Logic High Voltage	V_{IH}	DV_{CC} = Max	0.7xV_{CC}	-	-	V
Input Logic Low Voltage	V_{IL}	DV_{CC} = Min	-	-	0.3xV_{CC}	V
Input Logic Current	I_{IH}, I_{IL}	DV_{CC} = Max Input = 0V or 3.3V	-10	-	10	µA
Input/Output Capacitance	C_{IN}	CLK Frequency = 400kHz, Note 2, All Measurements Referenced to GND T_A = 25°C	-	-	8	pF
Output Logic High Voltage	V_{OH}	I_{OH} = -1mA, DV_{CC} = Max	0.9xV_{CC}	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 3mA, DV_{CC} = Min	0	-	0.1xV_{CC}	V
SCL Clock Frequency	f_{SCL}	Note 2	0	-	100	kHz
SCL Minimum Low Pulse Width	t_{LOW}		4.7	-	-	µs
SCL Minimum High Pulse Width	t_{HIGH}		4.0	-	-	µs
Data Hold Time	$t_{HD:DATA}$		0	-	-	ns
Data Setup Time	$t_{SU:DATA}$		250	-	-	ns
Rise Time	t_r	Note 2	-	-	1000	ns
Fall Time	t_f		-	-	300	ns

Electrical Specifications V_{CC} = 3.3V ±9%, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HMP8201			UNITS
			MIN	TYP	MAX	
TIMING CHARACTERISTICS						
Data Setup Time	t_{SU}	Notes 2, 3	10	-	-	ns
Data Hold Time	t_{HD}		0	-	-	ns
Clock to Out	t_{DVLD}		-	-	8.0	ns

NOTES:

2. Guaranteed by design or characterization.
3. Test performed with C_L = 40pF, I_{OL} = 3mA, I_{OH} = -1mA. Input reference level is 1.5V for all inputs. V_{IH} = 3.0V, V_{IL} = 0V.
4. Input leakage current includes hi-Z output leakage for all bidirectional/Three-State outputs.

Timing Waveforms

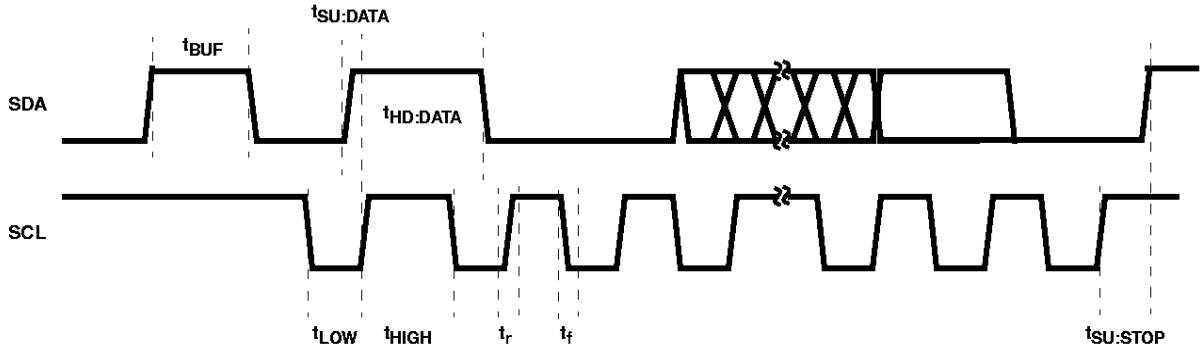


FIGURE 10. TIMING DIAGRAM

PCB Layout Considerations

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling. PCB trace lengths between groups of V_{CC} and GND pins should be as short as possible.

The optimum layout places the HMP8201 as close as possible to the PCI connector.

Component Placement

External components should be positioned as close as possible to the appropriate pin, ideally such that traces can be connected point to point. Chip capacitors are recommended where possible, with radial lead ceramic capacitors the second-best choice.

Power supply decoupling should be done using a 0.1µF ceramic capacitor in parallel with a 0.01µF chip capacitor for each group of V_{CC} pins to ground. These capacitors should be located as close to the V_{CC} and GND pins as possible, using short, wide traces.

Ground Plane

A common ground plane for all devices, including the HMP8201, is recommended. All GND pins on the HMP8201 must be connected to the ground plane.

Power Planes

All V_{CC} pins on the HMP8201 must be connected to the power plane.

Analog Signals

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize crosstalk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog output traces should also not overlay the HMP8201 and V_{CC} power planes to maximize high-frequency power supply rejection.

1.0 Data Flows

DATA FLOW	ACRONYM	DESCRIPTION
Local Scaled Uncompressed Video	LSUV	LSUV is generated by the Px64 IC to provide video for local display. The LSUV is received as 8-bit SIF (CIF, QCIF?) video at 20.25Mbytes/s for transmission over the PCI bus to the graphics accelerator. Local video is always at field rates or field interleaved with RSUV.
Remote Scaled Uncompressed Video	RSUV	RSUV is generated by the Px64 IC to provide video for remote display. The RSUV is received as 8-bit SIF (CIF, QCIF?) video at 20.25Mbytes/s for transmission over the PCI bus to the graphics accelerator. Remote video is always at frame rates or field interleaved with LSUV.
Local Uncompressed Still Frame Image	LUSFI	LUSFI is generated by the Px64 to support an “Annex D” image. This is a special transfer to the host component memory and can consist of a single SIF (CIF, QCIF?) image or a sequence of 4 SIF (CIF, QCIF?) images.
Compressed Video Local	CVL	CVL is a serial bit stream generated by the Px64 IC to transmit H.261 compressed video to the host component.
Local Compressed Still Frame Image	LCSFI	The LCSFI is generated by the Host Component software from the LUSFI. It consists of one or 4 compressed CIF frames of “Annex D” still video which are transmitted to the H.261 IC via the PCI bus and the ALP IC I/O Bus. The H.261 IC then inserts this compressed video in its outgoing CVL to the ALP.
Remote Compressed Still Frame Image	RCSFI	The Px64 extracts 1 or 4 CIF frames of compressed Annex D still frame images from the H.261 data stream to ship to the host for decompressing. The data is shipped *via* the I/O Bus to the ALP and then *via* the PCI Bus to the host.
Compressed Video Remote	CVR	CVR is a serial bit stream from the ALP IC to the H.261 IC which is fully compliant with the requirements of H.261 for the compressed video bit stream. This bit stream is extracted from the received H.221 stream within the ALP IC and then transmitted via a serial bus to the H.261 IC.
Digital Capture Audio	DCA	DCA is sampled locally to feed to audio processing for transmission to the remote end.
Digital Playback Audio	DPA	DPA is decompressed audio from the remote end to be played locally.
Compressed Audio Local	CAL	CAL is the digitally compressed version of the local audio stream. It is routed to the host via the PCI bus for inclusion in the H.221 data stream.
Compressed Audio Remote	CAR	CAR is the compressed audio stream from the remote end. It is extracted from the H.221 stream by the host and sent to audio processing section of the ALP via the PCI Bus.
Local Multiplexed Video Audio User Data	LVAU	Local teleconferencing (H.221) data from the host to the Telecom interface.
Remote Multiplexed Video Audio User Data	RVAU	Remote teleconferencing (H.221) data from the Telecom interface to the host.

1.1 Control Flows

DATA FLOW	ACRONYM	DESCRIPTION
Ntsc/pal Decoder Command	NPDC	Command issued to the NTSC/PAL Decoder.
Ntsc/pal Decoder Response	NPDR	Command response received from the NTSC/PAL Decoder.
Ntsc/pal Encoder Command	NPEC	Command issued to the NTSC/PAL Encoder.
Ntsc/pal Encoder Response	NPER	Command response received from the NTSC/PAL Encoder.
Px64 Processor Command	PPC	Command issued to the Px64 IC.
Px64 Processor Response	PPR	Command response received from the Px64 IC.
Audio Codec Command	ACC	Command issued to the Audio CODEC.
Audio Codec Response	ACR	Command response received from the Audio CODEC.
Telecommunications Device Command	TDC	Command issued to the Telecommunications Device.
Telecommunications Device Response	TDR	Command response received from the Telecommunications Device.
Bus Interface And Audio Processor Command	ALPC	Command issued to the Bus Interface and Audio Processor.
Bus Interface And Audio Processor Response	ALPR	Command response received from the Bus Interface and Audio Processor.
ALP Master Debug Command	DBGMC	Command issued to the ALP master DSP debug software.
ALP Master Debug Response	DBGMR	Command response received from the ALP master DSP debug software.
ALP Slave Debug Command	DBGSC	Command issued to the ALP slave DSP debug software.
ALP Slave Debug Response	DBGSR	Command response received from the ALP slave DSP debug software.

1.2 Major Data Paths

Table 1-1 describes data flows relative to the ALP. FIFO sizes are based on the assumption that a PCI bus request will be granted within 10 microseconds (µs).

TABLE 1-1. DATA FLOW DESCRIPTION

FLOW	PINS	RATE	HW	FIFO
LSUV: Local Uncompressed Video	In: Digital Video Out: PCI	20^{+}MB/s_{PEAK} 27^{+} on PCI	PCI Master	64 dw
RSUV: Remote Uncompressed Video	In: Digital Video Out: PCI	20^{+}MB/s_{PEAK} 27^{+} on PCI	PCI Master	64 dw
CVL: Compressed Video Local	In: IOB Out: PCI	16kB/s (G.728)	PCI Master	4 dw
CVR: Compressed Video Remote	In: PCI Out: IOB	16kB/s (G.728)	PCI Master	4 dw
CAL: Compressed Audio Local	In: PCI Out: SPI	8kB/s	PCI Master	5 dw
CAR: Compressed Audio Remote	In: SPI Out: PCI	8kB/s	PCI Master	5 dw
LCSFI/RCSFI: Annex D Compressed Image	In: PCI/IOB Out: IOB/PCI	16kB/s	PCI Master	8 dw
LVAU: Local Communications Output (2B Channel)	In: PCI Out: Telecom	16kB/s	PCI Master	8 dw
RVAU: Remote Communications Stream (2B Channel)	In: Telecom Out: PCI	16kB/s	PCI Master	8 dw
I^2C Command/Status (NPDC/NPDR, NPEC/NPER)	In: PCI/I^2C Out: I^2C/PCI	Very Low	PCI Target I2C Master	n/a
IOB Command/Status by Host (PPC/PPR, ACC/ACR)	In: PCI/IOB Out: IOB/PCI	Low	PCI Target IOB Master	n/a
IOB Download (PPC)	In: PCI Out: IOB		PCI Target IOB Master	
IOB Command/Status by DSP (ACC/ACR)	In: IOB/SPI Out: SPI/IOB		IOB Master	n/a
ALPC: Host->DSP Command Mailbox	In: PCI Out: SPI	Low	PCI Target	32 w
ALPR: DSP->Host Status Mailbox	In: SPI Out: PCI	Low	PCI Target	32 w
DBGMC: Host->MDSP Debug Command Mailbox	In: PCI Out: MDSP	Low	PCI Target	32 w
DBGMR: MDSP->Host Debug Status Mailbox	In: MDSP Out: PCI	Low	PCI Target	32 w
DBGSC: Host->SDSP dEbug Command Mailbox	In: PCI Out: SDSP	Low	PCI Target	32 w
DBGSR: SDSP->Host Debug Status Mailbox	In: SDSP Out: PCI	Low	PCI Target	32 w
DCA: Local Digital Audio	In: IOB Out: SPI	32kB/s	Channel	sw
DPA: Remote Digital Audio	In: SPI Out: IOB	32kB/s	Channel	sw
DSP Algorithms	In/Out SRAM	20MW/s_{PEAK}	Direct Access	sw
DSP Inter-Proc Comm	In/Out SRAM			
Board Identity	In/Out I2C	1/reboot	State Mach	n/a

2.0 Description of Functions

2.1 Bus Interface Component

2.1.1 PCI Interface

The PCI Interface provides a gateway through which video teleconferencing data and control are passed between a host computer and PCMS chip set. In some cases, the host computer performs the data transfer by acting as a PCI master, in others, the ALP acts as a PCI master to transfer the data.

The PCI Interface provides two sets of register address spaces which are visible on the PCI bus. The first register set is used to configure the ALP for PCI operation and includes the registers required for plug-and-play compatibility. The second register set, which supports double word transfers only, is used to provide control, status, and data transfer information associated with the PCMS chip set operation.

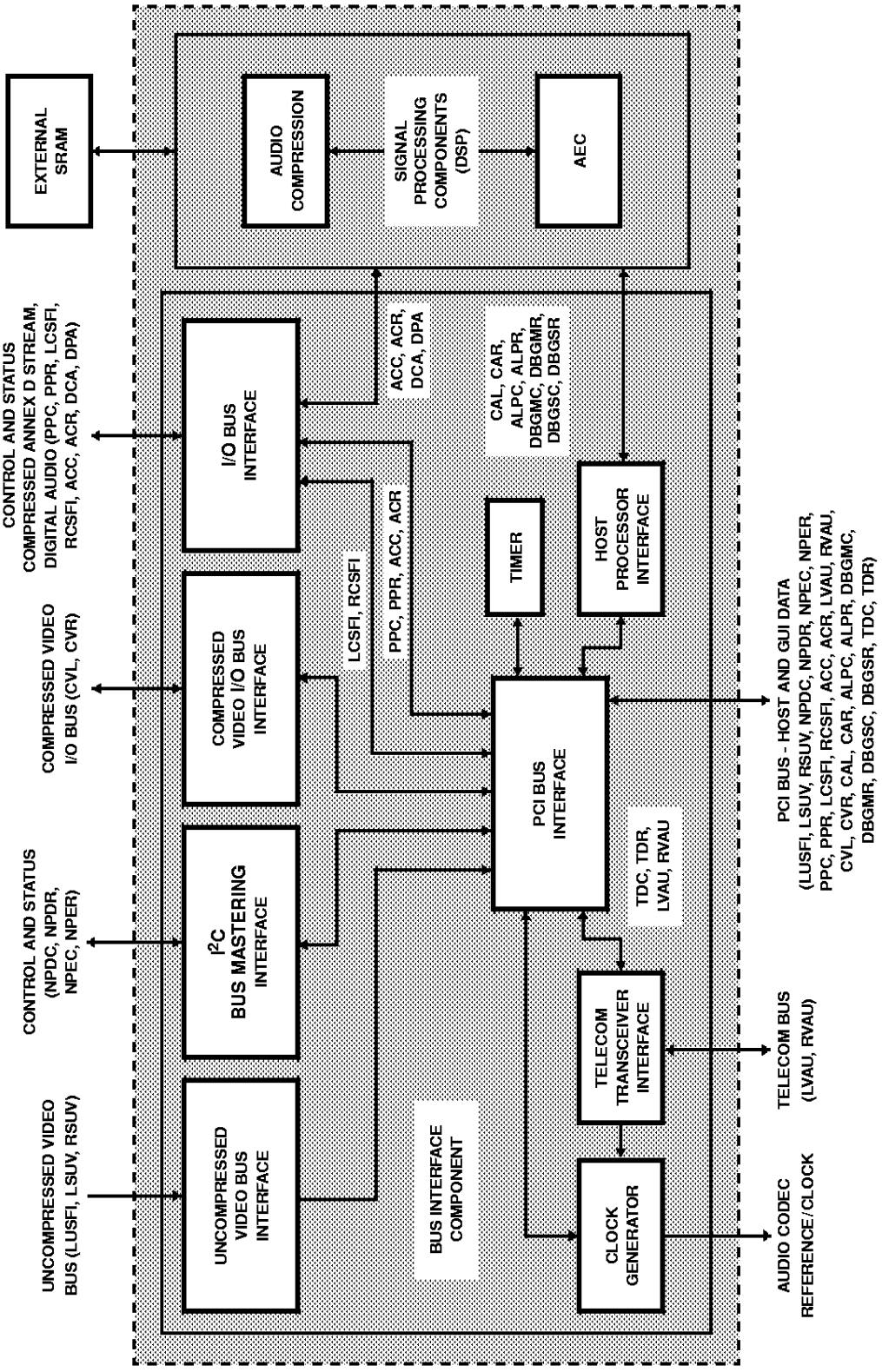
The ALP supports little endian transfers.

The following sections detail the data transfers that must be supported by the ALP and the register spaces that are visible to the PCI bus. The PCI interface conforms to the PCI 2.1 specification.

2.1.1.1 Transfers That Require the ALP as PCI Master

	ALP PCI BUS MASTER TRANSFERS	DATA FLOW ROUTING	DATA RATE
1	Uncompressed video data from local source	From UVI to Host/GUI	27MB/s_{PEAK}, 10MByte/s avg.
2	Uncompressed video data from remote source	From UVI to Host/GUI	27MB/s_{PEAK}, 10MByte/s avg.
3	Local H.221 bit stream	From Host to Telecom	16kByte/s
4	Remote H.221 bit stream	From Telecom to Host	16kByte/s
5	Local H.261 compressed video stream	From CVI to Host	up to 16kByte/s
6	Remote H.261 compressed video stream	From Host to CVI	up to 16kByte/s
7	Local G.7xx compressed audio stream	From SPI to Host	up to 8kByte/s
8	Remote G.7xx compressed audio stream	From Host to SPI	up to 8kByte/s
9	Annex D half-duplex data for the I/O Bus Interface	Host <-> IOB	16kByte/s_{PEAK}

Functional Block Diagram



2.1.1.2 Transfers That Require the ALP as PCI Target

	ALP PCI BUS TARGET TRANSFERS	DATA FLOW ROUTING	DATA RATE
1	I/O Bus control/status transfers	Host <-> IOB	Low
2	I^2C bus transfers	From Host to I^2C	200kbit/s
3	SPI command mailbox	From Host <-> SPI	Low
4	SPI status mailbox	From SPI to Host	Low
5	SPI MDSP debug command mailbox	From Host <-> MDSP	Low
6	SPI MDSP debug status mailbox	From MDSP to Host	Low
7	SPI SDSP debug command mailbox	From Host <-> SDSP	Low
8	SPI SDSP debug status mailbox	From SDSP to Host	Low
9	Timer Interface	From Host to BIF	Low
10	Miscellaneous PCI mapped registers	From Host to BIF	Low

2.1.1.3 PCI Configuration Registers

The PCI Configuration registers conform to the 256 byte Configuration Space specification set forth in the PCI 2.1 specification (Chapter 6). The first 16 bytes of the configuration space represent a read only universal header whose content is set by ROM on board the ALP. User specific vendor information is loaded into the Subsystem ID and Subsystem Vendor ID registers from an I^2C serial EEPROM (Section 2.1.3.2). The full address map and register description of the Configuration Register Space is contained in Section 3.1.

2.1.2 ALP PCI Based Control/Status Registers

The ALP has an 4000 byte block of PCI register space for control, status, and data transfer control. This register block is allocated in PCI space at boot up by the host. The base address of the register block is set by loading the appropriate PCI configuration register (see Section 3.1.1). The address map and register description for the ALP Control/Status registers is given in Section 3.1.2. This section contains functional descriptions of the simpler PCI control and status registers and the more complex register sets are detailed in succeeding sections.

2.1.2.1 Master Control Register

The Master Control Register provides bits for soft resets for the whole ALP and the DSP processors on the ALP, power-down mode, self-test initiation and fail-safe control. The ALP soft reset, resets the entire chip except for the PCI configuration registers and the Master Control Register. The ALP soft reset also generates the external system reset. The DSP soft reset resets the 2 DSP cores. The power-down mode permits the device to enter a low power state (this requires the ALP be reprogrammed after power-down is disabled). Self-test permits initiating internal diagnostics. Fail-safe control will force the Uncompressed Video PCI masters to stop writing to external PCI addresses.

2.1.2.2 PCI Based Timer Control Register

The ALP provides a free running timer counter for system synchronization and periodic interrupt generation. The operation of the timer is controlled via the PCI bus.

2.1.2.2.1 PCI Based Timer Resolution and Range

Timer resolution is determined by dividing the system clock (SYSCLK) by 54000. Assuming a 27MHz system CLK, this will result in a 2ms timer resolution. Since this is an 8-bit timer, the maximum timer interrupt cycle is 510ms. Note: 54000 can be factored into $2^4 * 3^3 * 5^3$.

2.1.2.2.2 PCI Based Timer Operation

The timer's interrupt period is set by loading a value into the PCI based Timer Period Register (see Section 3.1.2.1.2). When the timer is enabled, the contents of the Timer Period Register are loaded into the current count register which is decremented at a 2ms rate (assuming a 27MHz system CLK is used). When the current count register reaches zero, the IRQ bit in the Master Interrupt register (see Section 3.1.2.2.2) is set, and a PCI interrupt (if enabled) is posted via INTA. On the next timer clock, the contents of the Timer Period Register will be reloaded into the current count register and the decrement cycle continues. The contents of the current count register may be monitored by reading the PCI based Timer Count Register (see Section 3.1.2.1.2). The timer is enabled by setting the Timer Period register to a non-zero value and setting the Timer Enable bit in the Timer Control Register. The PCI interrupt generation is enabled by setting the Timer bit of the Interrupt Mask Register.

2.1.2.3 DSP Health Register

This register provides the host information about the internal state of the 2 DSP cores during boot load.

2.1.2.4 Test Mode Register

This register is for factory use only.

2.1.2.5 DSP Mailbox FIFOs

The DSP Mailbox FIFO, in conjunction with flag bits in the Master Interrupt Flag Register, provide a full duplex messaging capability between the host computer videoconferencing application and the 2 DSP cores. Messages are limited to 32 16-bit words.

The DSP Mailbox FIFO is implemented as two physical FIFOs with access to each FIFO controlled by whether data is read or written. A write to this register goes into an incoming message FIFO while reading this register pulls data out of an outgoing message FIFO. The state of the two FIFOs are reflected in the Master Interrupt Flag Register. The message length is defined by the type of message being transferred. The protocol for message passing in each direction is described in the paragraphs below.

While this interface looks like a FIFO from the host side, it is a RAM from the DSP side. The DSP side maintains count registers for both FIFOs. The Host to DSP count register is incremented for every word that the host writes to its FIFO. When the host signals the DSP *via* interrupt that it the data is available, the DSP reads the count register to determine the message size. In the DSP to Host direction, the DSP writes the message size directly to the count register and the host FIFO circuitry decrements the count and generates an empty flag when the count decrements to 0.

2.1.2.5.1 DSP to Host Message Protocol

When an DSP loads a message for the host into the outgoing FIFO, the ALP sets the Outgoing Mailbox FIFO Flag bit in the Master Interrupt Flag Register. If PCI interrupt generation is required for this operation, the corresponding mask bit must be set in the Master Interrupt Mask Register. The host either polls or sets up an interrupt service to respond to this message indicator. The host reads the DSP Mailbox FIFO Register until the DSP to Host FIFO Empty indicator in the DSP Mailbox FIFO Register is set. The indicator is the FIFO empty flag and means that the current read value is **not** valid. When the read is completed, the host resets the Outgoing Mailbox FIFO Flag bit by writing a '1' to that bit. Resetting this bit indicates to the DSPs that the FIFO is empty and ready for the next message.

2.1.2.5.2 Host to DSP Message Protocol

Before transferring a message to the DSPs, the host must first check the Incoming Mailbox FIFO Flag bit in the Master Interrupt Flag Register. If this bit is "high" the incoming FIFO is empty and ready to be written by the host. If PCI interrupt generation is required for this operation, the corresponding mask bit must be set in the Master Interrupt Mask Register. The host either polls or sets up an interrupt service to respond to this message indicator. Once the host has written its message to the FIFO, the host resets the Incoming Mailbox FIFO Flag bit "low" to signal the DSPs that a new message is available for reading. When an DSP has read the message, it signals the host that it is ready for another message by setting the Incoming Mailbox FIFO Flag bit "high".

2.1.2.6 Master DSP Debug Mailbox FIFOs

The Master DSP Debug Mailbox FIFO operation is very similar to the DSP Mailbox FIFO. The only exception comes in the location of the interrupt flag and mask bits. The interrupt flag and mask bits are located in the DSP Debug Control Register (Section 3.1.2.10.1).

2.1.2.7 Slave DSP Monitor Mailbox FIFOs

The Slave DSP Debug Mailbox FIFO operation is very similar to the DSP Mailbox FIFO. The only exception comes in the location of the interrupt flag and mask bits. The interrupt flag and mask bits are located in the DSP Debug Control Register (Section 3.1.2.10.1).

2.1.2.8 Local Reference Clock Interface

The ALP provides a local reference clock which is used as the compressed video bus clock. The local reference clock is also divided down to provide an 8kHz reference clock (CCLK) required to synchronize the sampling rate of the audio codec with the video teleconferencing data rate.

2.1.2.8.1 Programmable Codec Reference CLK

The ALP provides the capability to drive the FSC pin of the MVIP interface with a reference clocked produced by the carry out bit of a 32-bit NCO phase accumulator. The reference clock frequency will be set by programming the PCI based Frequency Control Word register (see Section 3.1.2.1.6). The frequency control word sets the clock frequency based on the following equation:

Clock Frequency = CLK * $(FCW/2^{32})$,

where FCW is the 32-bit frequency control word. To produce ~8kHz with a 27MHz CLK, FCW = $00136B07_{16}$. With a 32-bit phase accumulator, a tuning resolution of ~0.006Hz is achieved.

2.1.2.8.2 PCI Based Reference Clock Control Registers

The ALPs on board clock generation circuitry is enabled to drive the Telecom Interface's frame sync (FSC) and data clock (DCL) pins by setting the controls in the Telecom Interface Control/Status Register (see Section 3.1.2.5.3). In addition, the fixed or programmable clock source is also selected via the Master Control Register. The frequency of the programmable clock is set by the 32-bit value loaded into the Frequency Control register (see Section 3.1.2.1.6).

2.1.2.9 Master Interrupt Flag Register

The Master Interrupt Flag Register provides a means for determining the state of various circuits within the ALP IC. The bits in this register identify specific interrupt requests. When a bit is asserted "high" as the result of some interrupt event, the PCI interrupt $\overline{INTA}$ will be asserted low. The PCI interrupt will remain asserted until the host resets the bit by writing a "1" to the bit position or masks the interrupt via the Interrupt Mask Register. Writing a "0" to a bit position has no effect. Note: the interrupt state is indicated here whether or not is has been enabled to generate PCI interrupts via $\overline{INTA}$. All interrupt prioritization is left to the host software. Note that interrupts associated with the DSP debug interface are contained in the DSP Debug Control Register (Section 3.1.2.10.1). See Section 3.1.2.2.1 for detailed bit descriptions.

2.1.2.10 Master Interrupt Mask Register

The Master Interrupt Mask Register provides a means for selecting which of the Master Interrupt Flag Register bits will generate a PCI interrupt. See Section 3.1.2.2.1 for detailed bit descriptions.

2.1.3 I^2C Bus Interface

The ALP provides an I^2C interface which is used to program the internal registers of the NTSC/PAL Encoder IC and the NTSC/PAL Decoder IC. In addition, the ALP uses this interface to upload PCI Interface configuration data from an I^2C serial EPROM to the ALP shortly after system reset. The I^2C is a two wire interface consisting of a serial clock line, SCL, and a serial data line, SDA.

2.1.3.1 I^2C Master Operation

The ALP only functions as an I^2C Bus Master. As a result, the ALP can only be connected to I^2C slave devices without bus contention.

2.1.3.2 PCI Configuration via I^2C EEPROM

The ALP uploads the vendor specific information required for PCI interface configuration from an I^2C compatible serial EEPROM. The required information is 32 bits in length and represents the Subsystem Vendor ID and Subsystem ID. The ALP will read this information and load it into address $2C_{16}$ of PCI Configuration Space (see Section 3.1.1). The ALP reads the serial EEPROM and initializes the PCI Configuration Space after system reset.

2.1.3.3 Suggested I^2C EEPROMs

The suggested I^2C EEPROMs are the 24LC01B (128x8) 2.5V CMOS Serial EEPROM from Microchip Technology ($0.54 in 100s), or the NM24C02L 2K Bit Serial EEPROM with Extended Voltage from National Semiconductor ($1.01 in 100s).

2.1.3.4 I^2C EEPROM Address

The 8-bit slave address and broadcast on the I^2C bus for EEPROM read and write operations is given in the Table 2-1. See EEPROM data sheets for more information.

TABLE 2-1.

OPERATION	I^2C DEVICE ID	CHIP SELECT	$\overline{R/W}$ BIT
Read	1010	XXX	1
Write	1010	XXX	0

2.1.3.5 Data Transfers Between I^2C and PCI

Data transfers between the PCI and the ALP's I^2C bus are controlled by two PCI based I^2C control registers (see Section 3.1.2.3). All I^2C operations are initiated when bit 24 of address 10_{16} is updated. The ALP will perform an I^2C master read or write depending on the value written to bit 23 of address 10_{16}. After completion of the I/O cycle, the appropriate status bits will be set.

2.1.4 I/O Bus Interface

The I/O Bus is a general purpose 8-bit parallel interface used for control/data transfers to the Px64 chip and the audio codec. The ALP is the I/O Bus master.

2.1.4.1 I/O Bus Signals

The I/O bus consists of the signals listed in this document.

2.1.4.1.1 I/O Bus Data (IOD<>)

The I/O Bus has eight data lines. These lines are three-stated by all devices except during write cycles. Bit 0 of the bus contains the least significant bit (LSB) of the data and bit 7 contains the most significant bit (MSB).

2.1.4.1.2 I/O Bus Address (IOA<>)

The I/O Bus has eight address lines. All address lines are driven by the master device only. IOA[3:2] are spare. The two LSBs of address are used for target device register addressing. The remaining 4 address lines are dedicated to particular functions and are described in succeeding paragraphs. The mapping of the two LSBs is described in Table 2-2. Accesses to the target device's internal registers by using the Index Address and Indexed Data registers is known as programmed I/O (PIO).

TABLE 2-2. PIO REGISTER MAPPING

IOA1	IOA0	REGISTER NAME
0	0	Index Address register (PIO)
0	1	Indexed Data register (PIO)
1	0	Status register
1	1	Direct Data register

a) The Index Address register contains the index for the target device's internal registers. There are a maximum of 256 internal registers in a target device.
b) The Indexed Data register contains the data of/for the register indexed by the Index Address register (PIO).
c) The Status register contains the target device's internal status (for status mapping refer to the target device's register documentation).
d) The Direct Data register is for direct data access.

2.1.4.1.2.1 $\overline{VC_CS}$

$\overline{VC_CS}$ (IOA4) is the Px64 chip select. It is driven by the I/O Bus master. $\overline{VC_CS}$ is asserted when the Px64 chip is accessed.

2.1.4.1.2.2 $\overline{CCS}$

$\overline{CCS}$ (IOA5) is the Audio Codec chip select. It is driven by the I/O Bus master. $\overline{CCS}$ is asserted only when the Audio Codec chip is accessed for PIO transfers. The $\overline{CCS}$ signal and the $\overline{CDAK}$/$\overline{PDAQ}$ signals are mutually exclusive.

2.1.4.1.2.3 $\overline{CDAK}$

$\overline{CDAK}$ (IOA6) is the Audio Codec capture acknowledge. It is driven by the I/O Bus master and indicates that the following read cycle is a DMA read from the Audio Codec capture circuitry.

2.1.4.1.2.4 $\overline{\text{PDAK}}$

$\overline{\text{PDAK}}$ (IOA7) is the Audio Codec playback acknowledge. It is driven by the I/O Bus master and indicates that the following write cycle is a DMA write to the Audio Codec playback circuitry.

2.1.4.1.3 $\overline{\text{IORD}}$

The $\overline{\text{IORD}}$ signal (low active) is driven by the master device and is used to indicate a bus read cycle.

2.1.4.1.4 $\overline{\text{IOWR}}$

The $\overline{\text{IOWR}}$ signal (low active) is driven by the master device and is used to indicate a bus write cycle.

2.1.4.1.5 $\overline{\text{IOWAIT}}$

The $\overline{\text{IOWAIT}}$ signal (low active) is three-stated by all target devices except when the need arises to extend a bus cycle. A device has T_{WAIT} seconds to assert $\overline{\text{IOWAIT}}$ after the falling edge of $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$.

2.1.4.1.6 $\overline{\text{IOINT}}$

The $\overline{\text{IOINT}}$ signal is an open-drain output on all target devices. The line is connected to V_{CC} through a 10kΩ resistor. The $\overline{\text{IOINT}}$ remains asserted until cleared by the host processor.

2.1.4.1.7 IORQ<>

The I/O Bus has seven I/O request lines (**high** active). Four I/O request lines (IORQ[3:0]) are spare. The remaining 3 I/O request lines are dedicated to particular functions and are described in succeeding paragraphs. These lines indicate a target's request for an I/O transfer.

2.1.4.1.7.1 ADRQ

ADRQ (IORQ4) is both a data request and data available indication for the Px64 device. The data direction is determined by setting configuration registers in the master and target devices. This signal is active high.

2.1.4.1.7.2 CDRQ

CDRQ (IORQ5) indicates that the Audio Codec has data available. This signal remains active until the sample FIFO is empty. This signal is active high.

2.1.4.1.7.3 PDRQ

PDRQ (IORQ6) indicates that the Audio Codec is ready to accept data. This signal remains active while the sample FIFO is not full. This signal shall be active high.

2.1.4.2 I/O Bus Data Streams

The ALP supports the following data streams:

a) Px64 Control/Status

b) Input and output Annex D compressed video (Half-duplex)

c) Audio Codec Control/Status (Host and DSP)

d) Full Duplex Digital Audio Data

Arbitration circuitry shall be used to prioritize the allocation of bus cycles to pending data transfers. The data transfers are prioritized in order of the required data stream bandwidth. This results in the following prioritization from highest to lowest: Annex D I/O, Audio Codec Data, DSP-Audio Codec Control/Status, Host-Px64 Control/Status, Host-Audio Codec Control/Status.

To prevent undesired additional bus cycles, the slave device must de-assert its request signal within 54ns of the falling edge of $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$.

2.1.4.3 Data Transfers Between PCI and I/O Bus

The ALP supports the following transfers between the PCI and IOB:

a) Px64 Control/Status (ALP is a PCI Target)

b) Audio Codec Control/Status (ALP is a PCI Target)

c) Half duplex input and output Annex D compressed video (ALP is a PCI Master)

The host performs I/O Bus programmed input-output (PIO) data transfers to the Px64 and Audio Codec control/status registers via the PCI based I/O Bus Access registers (see Section 3.1.2.4).

Before the host can initiate any I/O Bus cycle, it must first check to make sure that all previous cycles have completed. This is accomplished by reading the I/O Bus Status/Read Data Register (Section 3.1.2.4.2) to verify that the previous read or write has completed.

After bus idle verification, the host performs an I/O Bus write by writing the 8-bit address, 8-bit data word, and setting the R/W (bit 16) to "0" in the I/O Bus Address/Write Data Register (section). The host may poll for the transaction to complete by waiting for a "1" to appear in the I/O Bus Write Status bit.

An 8-bit read is performed after idle verification by first writing the 8-bit read address and setting $\overline{\text{R/W}}$ to "1" in the I/O Bus Address/Write Data Register. After a "1" appears in the I/O Bus Read Status bit, the host may read the data in the LSB of the I/O Bus Status/Read Data Register.

2.1.5 Telecom Interface

The ALP provides a Telecom interface through which H.221 data transfers occur with the system ISDN modem. The local and remote H.221 data streams are transferred directly through the PCI interface to/from the host. The maximum sustainable data rate through this interface is 128kbits/s per local/remote data stream.

2.1.5.1 Telecom Interface Signals

The ALP provides a five wire interface that is compatible with ISDN modems using either a MVIP or IOM2 type interface. The signal lines include a serial clock (DCL), a serial data input (DI), a serial data output (DO), a frame sync (FSC), and an output data enable.

2.1.5.2 Telecom Interface Data Transfer Protocol

The ALP uses the an MVIP/IOM2 signaling convention to transfer data over the Telecom interface.

2.1.5.3 Telecom Bus Master

The ALP shall be capable of mastering the Telecom bus by software configuration of the Telecom Control register (Section 3.1.2.5). The ALP sources the frame sync and data clock signals and switch the interpretation of the data in and out signals.

2.1.5.4 Data Transfers between PCI and Telecom Interface

The ALP functions as a PCI master to transfer H.221 data to and from the Telecom Interface. The parameters governing these transfers are set in the PCI based Telecom Interface control registers (see Section 3.1.2.5).

2.1.6 Compressed Audio Interface

The Compressed Audio Interface is provided to handle the transfer of compressed audio data between the Host and the ALP via the PCI bus. The ALP provides separate PCI masters to read Compressed Audio Remote (CAR) from and write Compressed Audio Local (CAL) to host based ping-pong buffers. The compressed audio interface is controlled *via* the CAL/CAR Control Registers described in Section 3.1.2.6.

2.1.6.1 Compressed Audio Local (CAL) Data Transfers

The ALP acts as a PCI master to write local compressed audio to ping-pong buffers resident in host based memory. The host programs the base address of each ping-pong buffer by writing the CAL Buffer 1 and 2 Address registers (see Section 3.1.2.6.1). The size of the each buffer is set independently by the 15-bit values loaded into the CAL Buffer Length register.

CAL data transfers are initiated when the host sets the CAL Enable bit in the CAL/CAR Control/Status register. Once the CAL channel is enabled, the ALP begins writing data to CAL Buffer 1. The data transfer continues until the number of dwords specified in the CAL Buffer 1 Length register have been written. At this point, the CAL Buffer 1 Full bit in the Master Interrupt Register is set and a PCI interrupt is generated if enabled (see Interrupt Mask Register). The ALP will then begin writing data to CAL Buffer 2 provided the CAL Buffer 2 Full Bit in the Master Interrupt register has been reset by the host. When buffer 2 has been filled, buffer 1 will become the new target for data transfers completing the ping-pong cycle. If write attempt is made to a target buffer whose Buffer Full Bit has not been reset, CAL transfers are halted and the corresponding Buffer Overflow Bit will be set in the CAL Control/Status Registers. CAL transfers will resume once the Buffer Full bit for the target buffer has been reset.

CAL data transfers are halted when the ALP begins writing to a new target CAL Buffer and the corresponding buffer length has been set to zero in the CAL Buffer Length register. For example, if the ALP completes filling CAL Buffer 1 and then tries to write to CAL Buffer 2 when CAL Buffer 2 Length is zero, CAL Channel transfers are halted. Similarly, if the CAL channel is enabled when CAL Buffer 1 Length is zero, the CAL channel is immediately halted since Buffer 1 is the target buffer when the channel is enabled.

2.1.6.2 Compressed Audio Remote (CAR) Data Transfers

The ALP acts as a PCI master to read remote compressed audio from ping-pong buffers resident in host based memory. The host programs the base address of each ping-pong buffer by writing the CAR Buffer 1 and 2 Address registers (see Section 3.1.2.6.1). The size of the each buffer is set independently by the 15-bit values loaded into CAR Buffer Length register.

CAR data transfers are initiated when the host sets the CAR Enable bit in the CAL/CAR Control/Status register. Once the CAR channel is enabled, the ALP begins reading data from CAR Buffer 1. The data transfer continues until the number of dwords specified in the CAR Buffer 1 Length register have been read. At this point, the CAR Buffer 1 Empty bit in the Master Interrupt Register is set and a PCI interrupt is generated if enabled (see Interrupt Mask Register). The ALP will then begin reading data from CAR Buffer 2 provided the CAR Buffer 2 Full Bit in the Master Interrupt register has been reset by the host. When buffer 2 has been emptied, buffer 1 becomes the new target for data reads which completes the ping-pong cycle. If a read attempt is made to a target buffer whose Buffer Full Bit has not been reset, CAR transfers are halted and the corresponding Buffer Overflow Bit will be set in the CAR Control/Status Registers. CAR transfers will resume once the Buffer Full bit for the target buffer has been reset.

CAR data transfers are halted when the ALP starts to read a new target CAR Buffer and the corresponding buffer length has been set to zero in the CAR Buffer Length register. For example, if the ALP empties CAR Buffer 1 and then tries to read data from CAR Buffer 2 when the CAR Buffer 2 Length is zero, CAR data transfers are halted. Similarly, if the CAR channel is enabled when CAR Buffer 1 Length is zero, the CAR channel is immediately halted since Buffer 1 is the target buffer when the channel is enabled.

2.1.7 Compressed Video Interface

The ALP provides a Compressed Video Interface through which data is transferred between the Host and the Px64 chip. This interface function matches ALP-Px64 data transfers over the Compressed Video Bus with ALP-Host transfers over the PCI bus. The ALP acts as master for transfers over both the PCI and Compressed Video Bus.

2.1.7.1 Compressed Video Bus (CVB)

The ALP provides a 5 wire CVB capable of transferring serially at rates up to 384kbits/s. These signals include a serial data clock, CVCLK, remote and local compressed video lines, CVR and CVL, and I/O data gates, CVGTR and CVGTL. The signal interface is depicted in Figure 2-1.

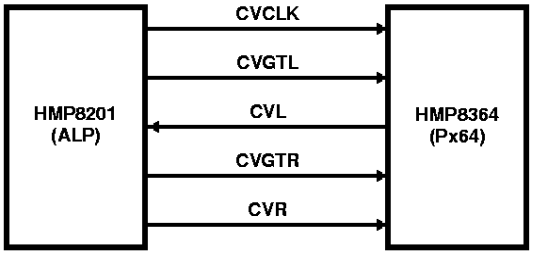


FIGURE 2-1. COMPRESSED VIDEO BUS SIGNALS

2.1.7.2 CVL/CVR Data Transfer Over CVB

The signaling protocol required to effect a master read compressed video data transfer is shown in Figure 2-2. The master uses the falling edge of CVCLK to latch in data when CVGTL is high. The corresponding master write is illustrated in 2-3. The slave shall use the falling edge of CVCLK to latch in data when CVGTR is high.

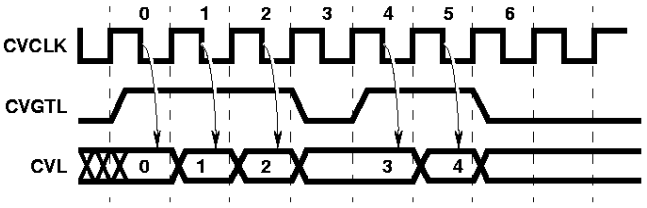


FIGURE 2-2. CVB MASTER READ

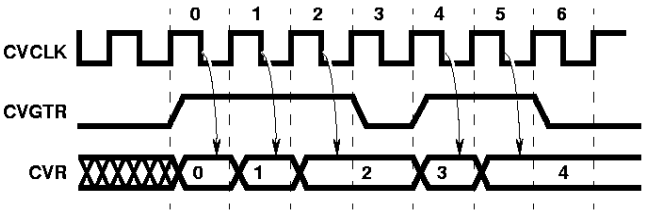


FIGURE 2-3. CVB MASTER WRITE

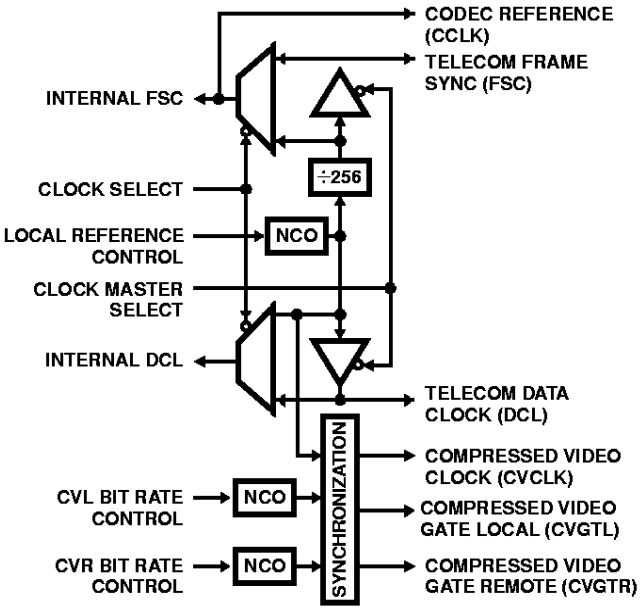


FIGURE 2-4. TELECOM, COMPRESSED VIDEO AND AUDIO REFERENCE CLOCK AND CONTROL

The source for the compressed video clock, CVCLK, is the Local Reference NCO. The CVCLK frequency is typically 2.048MHz. The gating signals are generated by the carry out of programmable NCOs. The gating signal frequency is set by loading the CVL and CVR Bit Rate Control Registers (see Section 3.1.2.7.3). The bit rate across the CVB is determined by the frequency with which the gating signals are asserted, and it is bounded at the upper end by the frequency of CVCLK (2.048MHz). Figure 2-4 depicts how the audio codec reference and Telecom signals are created and selected. Note: the gating signals are asserted synchronous with CVCLK.

The number of bits allocated to video in the H.221 multi frame sets the required bit rate over the CVB. Since the number of bits allocated to video in the H.221 frame can be variable over the course of a call, the host will update the Bit Rate Control registers to match changing bandwidth allocations for video in either the local or remote direction. The Px64 adapts compression to changes in bit rate based on the flow of data to and from its internal CVL and CVR buffers.

2.1.7.3 CVL/CVR Data Transfer over PCI

The ALP acts as a PCI master to read CVR data and write CVL data to ping-pong buffers using a protocol identical to that used for CAR and CAL data. The CVR transfers are controlled by a PCI based register set that mirrors the CAR registers in functionality. Similarly, the CVL transfers are controlled by a registers that mirrors the CAL registers. The control registers for used for compressed video transfer are described in Section 3.1.2.7.

2.1.8 Uncompressed Video (UV) Interface

The ALP provides a UV interface to receive both the local and remote UV streams from the Px64 chip. The video frames from each source are interleaved and sent to the ALP at an average rate of 30 frames/sec. This interface shall also support still frame capture to implement Annex D mode. The ALP shall act as a PCI master to transfer the received video streams to a target GUI/host via the PCI interface. The PCI interface provides the ability to

2.1.8.1 Uncompressed Video Bus (UVB)

The ALP provides an Uncompressed Video Bus (UVB) capable of receiving video data from the Px64 chip at a sustained rate of 20.25MB/s. These signals include an 8-bit data bus, UV[7:0], a vertical sync, VSYNC, a data valid, UVRDY, and a field indicator, FIELD. In addition, SYSCLK shall be used for the bus clock. A more complete discussion of the UV interface is contained in Sections 2.1.3 (Remote Display Scaler Requirements), 2.1.4 (Local Display Scaler Requirements), and 2.1.5 (Video Output Bus Logic) of the Px64 B-spec.

2.1.8.2 UVB Transfer Protocol

The ALP uses the rising edge of SYSCLK to clock in video data when UVRDY is high.

2.1.8.3 Data Transfers Between UVB and PCI

The ALP functions as a PCI master to transfer two streams of uncompressed video data received on the UVB to the PCI bus. These transfers are controlled by a block of 32-bit registers in the Video Channel portion of the PCI Control/Status Register block (Section 3.1.2.8). The ALP provides the following basic functionality:

a) Four 64 double word (32-bit) FIFOs (2 for the even field, 2 for the odd field)
b) Four buffer address registers (2 even/2 odd)
c) Two registers for controlling the gap between video lines (even/odd)
d) Two registers for controlling the dropping of video fields (even/odd)
e) Two lines per field counters and controls (even/odd)
f) Two pixels per line counters and controls (even/odd)
g) Two RGB Alpha fill registers (even/odd)
h) Controls for even/odd fields for overflow handling, Alpha mode enable, field capture mode and buffer enable.
i) Status for even/odd fields reflecting buffer and FIFO conditions and current buffer transfer state.
j) Control for the size of PCI Bus block transfers (0 to 64 double words).

3.0 Description of Registers

3.1 PCI Register Space

The host visible PCI space is divided into a PCI Configuration Space as required by Version 2.1 of the PCI spec, and a PCI Control/Status space as required for the operation of the Harris PCMS chip set.

3.1.1 PCI Configuration Space

The PCI Configuration Space consists of a 256 byte block of registers resident on the ALP. These registers map to the first 256 bytes of PCI address space, and they have an organization as shown in Table 3-1. For a complete register description, refer to version 2.1 of the PCI Local Bus Specification.

TABLE 3-1. PCI CONFIGURATION SPACE

BITS	TYPE	REGISTER DESCRIPTION
DEVICE AND VENDOR IDs (Offset 00_{16})		
31:16	R	**Device ID**: Harris part number
15:0	R	**Vendor ID**: Harris vendor ID
Default Value After Reset: 82 01 12 60		
STATUS AND COMMAND (Offset 04_{16})		
31:16	R	**Status**: Displays Status information for PCI related events
15:0	R/W	**Command**: Provides coarse control over bus transactions
Default Value After Reset: 00 00 00 00		
CLASS CODE AND REVISION ID (Offset 08_{16})		
31:8	R/W	**Class code**: Indicates generic function of device.
7:0	R/W	**Revision ID**: Silicon revision.
Default Value After Reset: 00 00 00 00		
BIST, HEADER TYPE, LATENCY TIMER AND CACHE LINE SIZE (Offset $0C_{16}$)		
31:24	R/W	**BIST**: Optional register for control and status of Built In Self Test (BIST)
23:16	R/W	**Header Type**: Identifies layout of configuration space, the ALP supports type 00_{16}
15:8	R/W	**Latency Timer**: See PCI specification for explanation
7:0	R/W	**Cache Line Size**: Specifies system cache line size in units of 32-bit words
Default Value After Reset: 00 00 00 00		
BASE ADDRESS REGISTERS 0 - 5 (Offset 10_{16} - 24_{16})		
31: 0	R/W	**Base Address Register n (BRn)**: Base addresses of the PCI Control/Status registers. These 6 registers provide the capability to map 6 different address spaces. A '1' in the LSB of the registers indicates that the address space is I/O mapped. A '0' in the LSB of the registers indicates that the address space is memory mapped. The ALP uses only BR0.

TABLE 3-1. PCI CONFIGURATION SPACE (Continued)

BITS	TYPE	REGISTER DESCRIPTION
Default Value After Reset: 00 00 00 00		
CARDBUS CIS POINTER (Offset 28_{16})		
31:0	R/W	**Cardbus CIS Pointer:** Optional register for devices that share silicon between Card Bus and PCI
Default Value After Reset: 00 00 00 00		
SUBSYSTEM ID AND SUBSYSTEM VENDOR ID (Offset $2C_{16}$)		
31:16	R/W	**Subsystem ID:** Add-in-card maker's product ID, loaded from configuration EEPROM
15:0	R/W	**Subsystem Vendor ID:** Add-in-card maker's vendor ID, loaded from configuration EEPROM
Default Value After Reset: 82 01 12 60		
EXPANSION ROM BASE ADDRESS (Offset 30_{16})		
31:0	R/W	**Expansion ROM Base Address:** Expansion ROM base Address (see PCI specification)
Default Value After Reset: 00 00 00 00		
RESERVED (Offset 34_{16} - 38_{16})		
31:0	-	Reserved
Default Value After Reset: 00 00 00 00		
Max_Lat, Min_Gnt, INTERRUPT PIN AND INTERRUPT LINE (Offset $3C_{16}$)		
31:24	R/W	**Max_Lat**: ALP desired latency
23:16	R/W	**Min_Gnt**: ALP's desired burst period
15:8	R/W	**Interrupt Pin**: Indicates which interrupt pin is use by ALP (1 = $\overline{\text{INTA}}$)
7:0	R/W	**Interrupt Line**: Communicates interrupt routing (see PCI specification)
Default Value After Reset: 00 00 00 00		
RETRY TIMER AND TRDY TIMER (Offset 40_{16})		
31:16	-	Reserved
15:8	R/W	**Retry Timer**: Number of master transaction retries. This count is decremented every time the ALP is granted bus mastership. If the count decrements to 0, the NOTE: Placing a '0' in this register disables the timer.
7:0	R/W	**TRDY Timer**: Number of PCI clocks permitted per transaction. The count is decremented every PCI clock. If the count decrements to 0, the NOTE: Placing a '0' in this register disables the timer.
Default Value After Reset: 00 00 80 80		

3.1.2 PCI Control/Status Space

The ALP provides 200 bytes block of control/status interface for the PCMS chip set. The Control/Status space begins at a base address written by the host to the Base Address Register 0 (BR0) in the configuration space (see Section 3.1.1). The address map for the PCI Control/Status Space is given in Table 3-2.

TABLE 3-2. PCI CONTROL/STATUS ADDRESS MAP

REGISTER	OFFSET	REGISTER	OFFSET
GENERAL PURPOSE REGISTERS		**COMPRESSED VIDEO LOCAL/REMOTE (CVL/CVR)**	
Master Control	00_{16}	CVL Buffer 1 Addr	70_{16}
Timer Control	04_{16}	CVL Buffer 2 Addr	74_{16}
DSP Health	08_{16}	CVL Buffer Lengths	78_{16}
Test Mode	$0C_{16}$	CVR Buffer 1 Addr	$7C_{16}$
DSP Mailbox FIFO	10_{16}	CVR Buffer 2 Addr	80_{16}
Audio Reference Clock	14_{16}	CVR Buffer Lengths	84_{16}
INTERRUPT CONTROL		CVL/CVR Buffer Count	88_{16}
Interrupt Mask	18_{16}	CVL/CVR Channel Control/Status	$8C_{16}$
Master Interrupt Register	$1C_{16}$	CVL Bit Rate Control	90_{16}
I^2C BUS		CVR Bit Rate Control	94_{16}
I^2C Address/Write Data	20_{16}	**EVEN/ODD FIELD UNCOMPRESSED VIDEO**	
I^2C Status/Read Data	24_{16}	Even Field Buffer 1 Addr	98_{16}
I/O BUS		Even Field Buffer 2 Addr	$9C_{16}$
I/O Bus Address/Write Data	28_{16}	Lines Per Even Field	$A0_{16}$
I/O Bus Status/Read Data	$2C_{16}$	Even Field Line Length/Line Gap	$A4_{16}$
TELECOM TX/RX CHANNELS		Even Field Drop Count/RGB Alpha	$A8_{16}$
Telecom TX Buffer 1 Addr	30_{16}	Odd Field Video Buffer 1 Addr	AC_{16}
Telecom TX Buffer 2 Addr	34_{16}	Odd Field Video Buffer 2 Addr	$B0_{16}$
Telecom TX Buffer Lengths	38_{16}	Lines Per Odd Field	$B4_{16}$
Telecom RX Buffer 1 Addr	$3C_{16}$	Odd Field Line Length/Line Gap	$B8_{16}$
Telecom RX Buffer 2 Addr	40_{16}	Odd Field Drop Count/RGB Alpha	BC_{16}
Telecom RX Buffer Lengths	44_{16}	Line Count	$C0_{16}$
Telecom RX/TX Buffer Count	48_{16}	Uncompressed Video Control/Status	$C4_{16}$
Telecom Interface Control/Status	$4C_{16}$	Video Channel Block Size	$C8_{16}$
COMPRESSED AUDIO LOCAL/REMOTE (CAL/CAR)		**ANNEX D**	
CAL Buffer 1 Addr	50_{16}	Annex D Buffer 1 Addr	CC_{16}
CAL Buffer 2 Addr	54_{16}	Annex D Buffer 2 Addr	$D0_{16}$
CAL Buffer Lengths	58_{16}	Annex D Buffer Lengths	$D4_{16}$
CAR Buffer 1 Addr	$5C_{16}$	Annex D Buffer Count	$D8_{16}$
CAR Buffer 2 Addr	60_{16}	Annex D Control/Status	DC_{16}
CAR Buffer Lengths	64_{16}	**DEBUG/MONITOR**	
CAL/CAR Buffer Count	68_{16}	Debug Control/Status	$E0_{16}$
CAL/CAR Channel Control/Status	$6C_{16}$	Master DSP Monitor Mailbox FIFO	$E4_{16}$
		Slave DSP Monitor Mailbox FIFO	$E8_{16}$

3.1.2.1 General Purpose Registers

3.1.2.1.1 Master Control Register (Offset 00_{16})

BITS	TYPE	REGISTER DESCRIPTION
31:6	-	Reserved
5	R/W	**Fail Safe Mode**: 0 = Enable Fail Safe Mode of Operation 1 = Disable Fail Safe Mode
4	R/W	**Selftest Fault**: 1 = selftest failure.
3	R/W	**Selftest Initiation**: Writing "1" to this bit position initiates an ALP selftest. Reads of this bit position will return "1" until the selftest is completed. Reading a value of "0" indicates the selftest is completed and the Selftest Fault bit is valid.
2	R/W	**Power Down Enable**: Setting this bit activates power down mode. 1 = Enable power down mode. 0 = Disable power down mode.
1	R/W	**DSP Processor Reset**: This bit is used to reset the DSPs by booting them from ROM code. The reset is initiated when the host sets this bit "high". The reset is cleared when the host writes this bit low. NOTE: This bit must remain asserted "high" for at least 1µs for proper operation.
0	R/W	**Soft Reset**: This bit is used to reset "everything" but the PCI Configuration Space Registers. It spawns software resets in the encoder, decoder, Px64, and the audio codec. On board the ALP, the DSPs and the data channel interfaces are reset. All the Control/Status registers in this section are reset to their default state. A reset is initiated by writing this bit "high". The reset is cleared by writing this bit low. NOTE: This bit must remain asserted "high" for at least 100µs for proper operation.
Default Value After Reset: 00 00 00 00		

3.1.2.1.2 Timer Control Register (Offset 04_{16})

BITS	TYPE	REGISTER DESCRIPTION
31:24	-	Reserved.
23:16	R	**Timer Count**: The value read from this register mirrors the contents of the timer counter's current count register. The count corresponds to the number of 2ms counter clocks that will occur before an interrupt is generated (see Section 2.1.7).
15:9	-	Reserved
8	R/W	**Timer Enable**: Enables timer operation. Note: once enabled, the timer counter is free running. 1 = Enable Timer Counter 0 = Disable Timer Counter
7:0	R/W	**Timer Period**: The value written to these bits is loaded into the timer counter when the counter is enabled or when it reaches the terminal count, "0". Note: the timer counter is disabled by a zero timer period value.
Default Value After Reset: 00 00 00 00		

3.1.2.1.3 DSP Health Register (Offset 08_{16})

BITS	TYPE	REGISTER DESCRIPTION
31	R/RST	**Slave DSP Interrupt To Host:** Slave DSP uses this interrupt to signal host. This bit is reset by writing a '1'.
30	R/W	**Slave DSP Interrupt to Host Mask Bit**: Setting this to '1' enables Slave DSP interrupt to Host.
29:24	-	Reserved.
23:16	R	**Slave DSP Status**: Provides basic status information about Slave DSP Processor before the mailbox system is functional (e.g. at boot time).
15	R/RST	**Master DSP Interrupt to Host**: Master DSP uses this interrupt to signal host. This bit is reset by writing a '1'.
14	R/W	**Master DSP Interrupt to Host Mask Bit**: Setting this to '1' enables Master DSP interrupt to Host.
13:8	-	Reserved.
7:0	R	**Master DSP Status**: Provides basic status information about Master DSP Processor before the mailbox system is functional (e.g. at boot time).
Default Value After Reset: 00 00 00 00		

3.1.2.1.4 Test Mode Register (Offset $0C_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31:16	R/W	**Test Pattern [15:0]**: Test pattern used in testing of PCI timer.
15:8	R/W	**Test Route [7:0]**: Routing mode control bits for timer counter state observability.
7:6	R/W	**Test Mode**: These bits are used for programming timer tests.
5:3	R/W	**SIG Test Mode**: These bits are used for programming SIG tests.
2:0	R/W	**PLL Control**: These bits are used for controlling the compute clock PLL.
Default Value After Reset: 00 00 00 00		

3.1.2.1.5 DSP Mailbox FIFOs (Offset 10_{16})

BITS	TYPE	REGISTER DESCRIPTION
31	R	**DSP to Host FIFO Empty**: This bit, when high, indicates that the current value being read is not valid because the FIFO went empty.
30:16	-	Reserved.
15:0	R/W	**Message Data**: Each message transfer is 2 bytes to match the data path of the DSPs, and to avoid packing and unpacking on both the host and ALP.
Default Value After Reset: 80 00 00 00		

3.1.2.1.6 Local Reference Clock Register (Offset 14_{16})

BITS	TYPE	REGISTER DESCRIPTION
31:0	R/W	**Frequency Control Word**: This 32-bit value sets the frequency of the NCO used to generate the reference clock (see Section 2.1.8.2).
Default Value After Reset: 13 6B 06 E7 (2047999.999719Hz for 27MHz CLK)		

3.1.2.2 Interrupt Control

These registers provide for PCI interrupt masking, request, and acknowledgment.

3.1.2.2.1 Master Interrupt Mask Register (Offset 18_{16})

BITS	TYPE	REGISTER DESCRIPTION
31	R/W	UV Halt:
30	R/W	Watch Dog Timer Reset of DSPs:
29	-	Reserved.
28	R/W	Outgoing Mailbox FIFO:
27	R/W	Incoming Mailbox FIFO:
26	R/W	Timer:
25	R/W	**I^2C Transfer Complete:** Read or Write operation complete.
24	R/W	I/O Bus Transfer Complete:
23	R/W	I/O Bus Interrupt :
22	R/W	Telecom Buffer Error:
21	R/W	Telecom TX Buffer 1 Empty:
20	R/W	Telecom TX Buffer 2 Empty:
19	R/W	Telecom RX Buffer 1 Full:
18	R/W	Telecom RX Buffer 2 Full :
17	R/W	CVL/CVR Error:
16	R/W	**CVL Buffer 1**: Buffer Full
15	R/W	**CVL Buffer 2**: Buffer Full
14	R/W	**CVR Buffer 1**: Buffer Empty
13	R/W	**CVR Buffer 2**: Buffer Empty
12	R/W	CAL/CAR Error:
11	R/W	**CAL Buffer 1**: Buffer Full
10	R/W	**CAL Buffer 2**: Buffer Full
9	R/W	**CAR Buffer 1**: Buffer Empty
8	R/W	**CAR Buffer 2**: Buffer Empty
7	R/W	UV FIFO Overflow:
6	R/W	**UV Even Field Video Buffer 1**: Buffer Full
5	R/W	**UV Even Field Video Buffer 2**: Buffer Full
4	R/W	**UV Odd Field Video Buffer 1**: Buffer Full
3	R/W	**UV Odd Field Video Buffer 2**: Buffer Full
2	R/W	Annex D Error:
1	R/W	Annex D Buffer 1 Done:
0	R/W	Annex D Buffer 2 Done:
Default Value After Reset: 00 00 00 00		

3.1.2.2.2 Master Interrupt Register (Offset $1C_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31	R/RST	**UV Halt**: When set, it indicates that the transmission of uncompressed video has been halted by the fail safe mechanism. Transmissions are halted at a field boundary. Resetting this bit once transmissions have been halted will cause transfers to start with the next VSYNC. To prevent a Fail Safe halt, this bit must be reset at least once per 16 VSYNCs (16 x 16.67ms).
30	R/RST	**Watch Dog Timer Reset of DSPs**: Set when DSPs have been reset by watchdog timer.
29	-	Reserved.
28	R/RST	**Outgoing Mailbox FIFO**: ALP sets “high” to indicate message available. Host resets when message read.
27	R/RST	**Incoming Mailbox FIFO**: ALP sets “high” when FIFO empty. Hosts resets when FIFO contains new message.
26	R/RST	**Timer**: ALP sets “High” to indicate timer terminal count has been reached. Has no effect on timer counter.
25	R/RST	**I^2C Transfer Complete**: Read or Write operation complete. This interrupt will not be set after the configuration ROM is read.
24	R/RST	**I/O Bus Transfer Complete**: This bit indicates that a host initiated I/O Bus transfer has been completed. This does not include Annex D or DSP initiated transfers.
23	R	**I/O Bus Interrupt**: This bit reflects the state of the $\overline{IOINT}$ pin. Not resettable by host in this register. The host must poll the I/O Bus devices to determine the source of the interrupt and clear it at the source.
22	R/RST	**Telecom Error**: This bit Indicates that a Buffer/FIFO error bit in the Telecom Control/Status Register is set. Read the Telecom Control/Status register to determine the exact error. Resetting this bit resets all of the error bits in the Telecom Control/Status Register.
21	R/RST	**Telecom TX Buffer 1 Empty**: This bit indicates that the buffer is empty and ready to be written with data by host. This bit is reset by the host when the buffer has been filled.
20	R/RST	**Telecom TX Buffer 2 Empty**: Description same as the Telecom TX Buffer 1 Empty bit.
19	R/RST	**Telecom RX Buffer 1 Full**: This bit indicates that the buffer is full and should be read by host. This bit is reset by the host when the buffer read is complete.
18	R/RST	**Telecom RX Buffer 2 Full** : Description same as Telecom RX Buffer 1 Full bit.
17	R/RST	**CVL/CVR Error**: This bit Indicates that a Buffer/FIFO error bit in the CVL/CVR Control/Status Register is set. Read the CVL/CVR Control/Status register to determine the exact error. Resetting this bit resets all of the error bits in the CVL/CVR Control/Status Register.
16	R/RST	**CVL Buffer 1**: Description same as Telecom RX Buffer 1 Full bit.
15	R/RST	**CVL Buffer 2**: Description same as Telecom RX Buffer 1 Full bit.
14	R/RST	**CVR Buffer 1**: Description same as the Telecom TX Buffer 1 Empty bit.
13	R/RST	**CVR Buffer 2**: Description same as the Telecom TX Buffer 1 Empty bit.
12	R/RST	**CAL/CAR Error**: This bit Indicates that a Buffer/FIFO error bit in the CAL/CAR Control/Status Register is set. Read the CAL/CAR Control/Status register to determine the exact error. Resetting this bit resets all of the error bits in the CAL/CAR Control/Status Register.
11	R/RST	**CAL Buffer 1**: Description same as Telecom RX Buffer 1 Full bit.
10	R/RST	**CAL Buffer 2**: Description same as Telecom RX Buffer 1 Full bit.
9	R/RST	**CAR Buffer 1**: Description same as the Telecom TX Buffer 1 Empty bit.
8	R/RST	**CAR Buffer 2**: Description same as the Telecom TX Buffer 1 Empty bit.
7	R/RST	**UV Error**: This bit indicates the UV FIFO has overflowed.
6	R/RST	**UV Even Field Video Buffer 1**: Description same as Telecom RX Buffer 1 Full bit.
5	R/RST	**UV Even Field Video Buffer 2**: Description same as Telecom RX Buffer 1 Full bit.
4	R/RST	**UV Odd Field Video Buffer 1**: Description same as Telecom RX Buffer 1 Full bit.
3	R/RST	**UV Odd Field Video Buffer 2**: Description same as Telecom RX Buffer 1 Full bit.
2	R/RST	**Annex D Error**: This bit Indicates that a Buffer/FIFO error bit in the Annex D Control/Status Register is set. Read the Annex D Control/Status register to determine the exact error. Resetting this bit resets all of the error bits in the Annex D Control/Status Register.
1	R/RST	**Annex D Buffer 1 Done**: Indicates Annex D Buffer 1 is full or empty depending on direction of data transfer.
0	R/RST	**Annex D Buffer 2 Done**: Indicates Annex D Buffer 2 is full or empty depending on direction of data transfer.
Default Value After Reset: 09 00 00 00		

3.1.2.3 I²C Bus

These registers provide the interface to perform I²C bus transfers.

3.1.2.3.1 I²C Address/Write Data (Offset 20_{16})

An I²C operation is initiated by writing this register with the I²C slave address, the write data (if required), and the I²C bus RD/WR bit. In Bit Bang Mode, the state of bit 0 and bit 1 is clocked through to SDA and SCL respectively by the PCI clock.

NOTE: Only bits 1 and 0 are used during bit bang mode.
Bits 1:0 must be set "high" before returning to normal I²C mode.

BITS	TYPE	REGISTER DESCRIPTION
31:25	R/W	**Slave Address** (7-bit address Mode)
24	R/W	**RD/WR**: 1 = Perform I²C read operation 0 = Perform I²C write operation
23:16	R/W	**Slave Address Extension**: These 7 bits are used together with bits 27:25 in 10-bit address mode. Bit 27 is the MSB. Bits 31-28 must be set to "11110" to indicate to I²C devices that 10-bit address mode is being used.
15:8	R/W	**Slave Sub-Address**: Slave address to be accessed
7:0	R/W	**Write Data**: During a write operation, this byte is transferred to the I²C target. In Bit Bang mode bits 1 and 0 map to SCL and SDA respectively.
Default Value After Reset: 00 00 00 00		

3.1.2.3.2 I²C Status/Read Data (Offset 24_{16})

This register contains data returned from an I²C read operation, status of an initiated RD/WR transfer, and one configuration bit to set the data rate of the I²C bus. This register must be monitored to verify that pending RD/WR operations have been completed before initiating a new RD/WR operation. In bit bang mode the state the SCL and SDA Read bits reflect the state of SCL and SDA as sampled by the ? clock. Only SCL Read and SDA Read are used in Bit bang mode.

BITS	TYPE	REGISTER DESCRIPTION
31:16	-	Reserved
15	R/W	**I²C Bus Data Rate**: 1 = High speed 400kbit/s operation 0 = Low speed 100kbit/s operation
14	R/W	**Bit Bang Mode**: 1 = Data transfers performed using bit bang mode 0 = Normal I²C transfer mode
13	R	**SCL Read**: This bit reflects the state of the SCL signal as sampled by SYSCLK.
12	R	**SDA Read**: This bit reflects the state of the SDA signal as sampled by SYSCLK.
11	-	Reserved
10	R	**I²C Error**: Always reflects status of last RD/WR operation. 1 = RD/WR operation produced an error 0 = RD/WR operation completed successfully
9	R	**I²C Read Status**: 1 = Read operation completed 0 = Read operation in progress, wait to initiate next transfer
8	R	**I²C Write Status**: 1 = Write operation completed 0 = Write operation in progress, wait to initiate next transfer
7:0	R	**Read Data**: Valid when RD operation complete and no I²C error
Default Value After Reset: 00 00 33 00		

3.1.2.4 I/O Bus

3.1.2.4.1 I/O Bus Address/Write Data (Offset 28_{16})

An I/O Bus Transfer is initiated by writing this register with the I/O Bus address, the write data (if required), and the RD/WR transfer bit. On completion a RD/WR cycle, a PCI interrupt is generated, otherwise, the I/O Bus Status/Read data register must be monitored to determine if previously initiated RD/WR cycles are finished before a new cycle is initiated.

BITS	TYPE	REGISTER DESCRIPTION
31:17	-	Reserved
16	R/W	**RD/WR Transfer**: 1 = Perform I/O Bus read operation 0 = Perform I/O Bus write operation
15:8	R/W	**I/O Bus Address**: 8-Bit I/O Bus target address (see section for address bit mapping).
7:0	R/W	**Write Data**: During a write operation, this byte is transferred to the I/O Bus target.
Default Value After Reset: 00 00 00 00		

3.1.2.4.2 I/O Bus Status/Read Data (Offset $2C_{16}$)

This register contains data returned from an I/O Bus read operation and the status of initiated RD/WR transfers.

BITS	TYPE	REGISTER DESCRIPTION
31:10	-	Reserved
9	R	**I/O Bus Read Status**: 1 = Read operation completed 0 = Read operation in progress, wait to initiate next transfer.
8	R	**I/O Bus Write Status**: 1 = Write operation completed 0 = Write operation in progress, wait to initiate next transfer.
7:0	R	**Read Data**: Data returned from a read operation. NOTE: Last read value remains until completion of another read.
Default Value After Reset: 00 00 03 00		

3.1.2.5 Telecom Interface

These registers are used to set up Telecom interface data transfers between host based buffers and the ALP.

3.1.2.5.1 Telecom Buffer Setup (Offset 30_{16} - 48_{16})

These registers contain the buffer configuration data required by the ALP to perform PCI master transfers of data to/from memory in PCI space.

BITS	TYPE	REGISTER DESCRIPTION
TELECOM TX BUFFER 1 ADDR (Offset 30_{16})		
31: 0	R/W	**TX Buffer 1 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
TELECOM TX BUFFER 2 ADDR (Offset 34_{16})		
31: 0	R/W	**TX Buffer 2 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
TELECOM TX BUFFER LENGTHS (Offset 38_{16})		
31	-	Reserved.

BITS	TYPE	REGISTER DESCRIPTION
30:16	R/W	**TX Buffer 2 Length**: Buffer length in dwords.
15	-	Reserved.
14: 0	R/W	**TX Buffer 1 Length**: Buffer length in dwords.
Default Value After Reset: 00 00 00 00		
TELECOM RX BUFFER 1 ADDR (Offset $3C_{16}$)		
31: 0	R/W	**RX Buffer 1 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
TELECOM RX BUFFER 2 ADDR (Offset 40_{16})		
31: 0	R/W	**RX Buffer 2 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
TELECOM RX BUFFER LENGTHS (Offset 44_{16})		
31	-	Reserved.
30:16	R/W	**RX Buffer 2 Length**: Buffer length in dwords.
15	-	Reserved.
14: 0	R/W	**RX Buffer 1 Length**: Buffer length in dwords.
Default Value After Reset: 00 00 00 00		
TELECOM RX/TX BUFFER COUNT (Offset 48_{16})		
31	R	**TX Target Buffer**: 1 = Count represents transfers to TX Buffer 2 0 = Count represents transfers to TX Buffer 1
30:16	R	**TX Transfer Count**: Number of double words written to target TX Buffer. The register is incremented from 0 to a maximum value set by the TX Buffer Length register. When the terminal count is reached, a PCI interrupt is generated if enabled (see Master Interrupt register). The count is reset to zero when transfers begin to an empty buffer.
15	R	**RX Target Buffer**: See TX Target Buffer Register
14:0	R	**RX Transfer Count**: See TX Transfer Count Register
Default Value After Reset: 00 00 00 00		

3.1.2.5.2 Handshake Protocol for ALP/Telecom Buffer Transfers

The handshaking required to transfer Telecom data between the host and the ALP is handled through the Master Interrupt register.

a) Transfers Between ALP and Host

Data received from the Telecom Interface is written by the ALP to one of the two enabled RX Buffers. When the target buffer is filled, the appropriate RX Buffer full bit is set in the Master Interrupt Register and a PCI interrupt is generated if enabled. The buffer is disabled for writing until the host resets the RX Buffer Full bit in the Master Interrupt Register. The host may need to mask the RX Buffer Full bit to prevent assertion of the PCI interrupt line until the host is prepared to reset the bit. Note: If both buffers are enabled when data transfers are initiated, RX Buffer 1 will be the target buffer.

b) Transfers Between Host and ALP

The ALP reads data from an enabled TX Buffer that will be output through the Telecom Interface. When the host specified number of dwords have been read from the TX Buffer, the ALP sets the TX Buffer Empty bit and generates a PCI interrupt if enabled. The TX Buffer is disabled for reading until the host has reset the TX Buffer Empty bit in the Master Interrupt Register. The host may need to mask the TX Buffer Empty bit to prevent assertion of the PCI interrupt line until the host is prepared to reset the bit. Note: If both buffers are enabled when data transfers are initiated, TX Buffer 1 will be the target buffer.

3.1.2.5.3 Telecom Interface Control/Status Register (Offset $4C_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31: 28	-	Reserved.
27	R/W	**MVIP/IOM2 Select**: 1 = MVIP Interface Selected 0 = IOM2 Interface Selected
26:22	R/W	**Start Channel**: Indicates the first time slot where valid data can be found.
21:17	R/W	**Stop Channel**: Indicates the last time slot where valid data can be found.
16	R/W	**Local Loop Back**: Reflects ISDN transfers back to host. 1 = Local loopback ON 0 = Local Loopback OFF
15	R/W	**Remote Loop Back**: Reflects ISDN transfers back to remote end. 1 = Remote Loopback ON 0 = Remote Loopback OFF
14	R/W	**Clock Master**: This bit selects source for the ISDN modem serial clock and frame sync (DCL and FSC respectively). 1 = The ALP drives DCL and FSC with internally generated clocks. 0 = The ISDN modem drives DCL and FSC, (normal state) NOTE: When set to “1”, the serial data output and input pins, DO and DI are swapped, i.e., the DO pin functions as the serial input and DI function s as the serial output. Also when set to “1” the clock select bit must be equal to “1”.
13	R/W	**Clock Select**: This bit selects the clock source used internally by the ALP. 1 = Uses internal NCOs to generate the DCL and FSC clocks required for processing. Also, uses NCO derived FSC signal to drive the audio codec reference clock, CCLK. 0 = Uses FSC and DCL from ISDN modem. In this mode, the externally provided FSC is used to drive the codec reference clock. (normal state)
12	R/W	**Active Clock Edge**: Selects active edge of serial data clock, DCL. 1 = Rising Edge 0 = Falling Edge
11	R/W	**Clock Frequency**: Selects serial clock frequency relative to data rate on DI/DO. 1 = Serial data clock, DCL, is 2x data rate 0 = Serial date clock is 1x data rate
10	R/W	**Frame Sync Polarity**: 1 = Frame Sync Active “High” 0 = Frame Sync Active “Low”
9	R/W	**Receive Enable**: 1 = Enable data transfers from ISDN Modem 0 = Disable data transfers from ISDN Modem NOTE: If data transfers are disabled, RX buffer transfers are halted and RX data is ignored.
8	R/W	**Transmit Enable**: 1 = Enable data transfers to ISDN Modem 0 = Disable data transfers to ISDN Modem NOTE: If data transfers are disabled, TX buffer transfers are halted and TX data is ignored.
7-4	-	Reserved
3	R	**TX Buffer Underflow**: This bit, when set “high”, indicates that the host based MVIP TX buffer has overflowed. Indicates host processing problem.
2	R	**RX Buffer Overflow**: This bit, when set “high”, indicates that the host based MVIP RX buffer has underflowed. Indicates host processing problem.
1	R	**TX FIFO Underflow**: When set “high”, the ALP’s TX FIFO has underflowed. Indicates PCI latency problem if Telecom RX Buffer enabled.
0	R	**RX FIFO Overflow**: When set “high”, the ALP’s RX FIFO has overflowed. Indicates PCI latency problem if Telecom RX Buffer enabled.
Default Value After Reset: 00 00 00 00		

3.1.2.6 Local/Remote Compressed Audio Control Registers

3.1.2.6.1 Compressed Audio Local/Remote (CAL/CAR) Buffers (Offset 50_{16} - 68_{16})

These registers contain the buffer configuration data required by the ALP to perform PCI master transfers of CAL/CAR data to/from buffers in PCI space.

BITS	TYPE	REGISTER DESCRIPTION
CAL BUFFER 1 ADDR (Offset 50_{16})		
31: 0	R/W	**CAL Buffer 1 Address**: Written by host to set buffer start address in PCI space. Note: the 2 LSBs of this address are hard coded to zero to force dword boundary, and these two bits read as zero.
Default Value After Reset: 00 00 00 00		
CAL BUFFER 2 ADDr (Offset 54_{16})		
31: 0	R/W	**CAL Buffer 2 Address**: Written by host to set buffer start address in PCI space. Note: the 2 LSBs of this address are hard coded to zero to force dword boundary, and these two bits read as zero.
Default Value After Reset: 00 00 00 00		
CAL BUFFER LENGTHS (Offset 58_{16})		
31	-	Reserved
30:16	R/W	**CAL Buffer 2 Length**: Buffer length in dwords. Data transfers will be halted when CAL Buffer 2 becomes the target buffer for data transfers and these bits are set to zero.
15	-	Reserved
14: 0	R/W	**CAL Buffer 1 Length**: Buffer length in dwords. Data transfers will be halted when CAL Buffer 1 becomes the target buffer for data transfers and these bits are set to zero.
Default Value After Reset: 00 00 00 00		
CAR BUFFER 1 ADDr (Offset $5C_{16}$)		
31: 0	R/W	**CAR Buffer 1 Address**: Written by host to set buffer start address in PCI space.7
Default Value After Reset: 00 00 00 00		
CAR BUFFER 2 ADDR (Offset 60_{16})		
31: 0	R/W	**CAR Buffer 2 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
CAR BUFFER LENGTHS (Offset 64_{16})		
31	-	Reserved
30:16	R/W	**CAR Buffer 2 Length**: Buffer length in dwords. Data transfers will be halted when CAR Buffer 2 becomes the target buffer for data transfers and these bits are set to zero.
15	-	Reserved
14: 0	R/W	**CAR Buffer 1 Length**: Buffer length in dwords. Data transfers will be halted when CAR Buffer 1 becomes the target buffer for data transfers and these bits are set to zero.
Default Value After Reset: 00 00 00 00		

BITS	TYPE	REGISTER DESCRIPTION
CAR/CAL BUFFER COUNT (Offset 68_{16})		
31	R	**CAL Target Buffer**: 1 = Count represents transfers to CAL Buffer 2 0 = Count represents transfers to CAL Buffer 1
30:16	R	**CAL Transfer Count**: Number of double words written to the target CAL Buffer. The register is incremented from 0 to a maximum value set by the CAL Buffer length register. When the terminal count is reached, a PCI interrupt is generated if enabled (see Master Interrupt register). The count is reset to zero when transfers begin to an empty buffer.
15	R	**CAR Target Buffer**: See CAL Target Buffer.
14:0	R	**CAR Transfer Count**: See CAL Transfer Count.
Default Value After Reset: 00 00 00 00		

3.1.2.6.2 CAL/CAR Control/Status Register (Offset $6C_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31: 6	-	Reserved
5	R	**CAL Buffer Overflow**: This active “high” bit indicates that one of the host based CAL ping-pong buffers has overflowed. This condition occurs when the ALP tries to write data to a host based CAL buffer whose Buffer Full Bit in the Master Interrupt Register has not been reset. This error indicates that the CAL Ping-Pong buffers are being written with data by the ALP faster than the host can process the data. This bit is reset when the CAL/CAR Error Bit is reset in the Master Interrupt Register or the CAL Channel Enable bit is set to zero.
4	R	**CAL FIFO Overflow**: This active “high” bit indicates that the ALP based CAL FIFO has overflowed. Indicates a PCI latency problem. NOTE: This bit is reset when the CAL/CAR Error Bit is reset in the Master Interrupt Register or the CAR Channel Enable bit is set to zero.
3	R	**CAR Buffer Underflow**: This active “high” bit indicates that one of the host based CAR ping-pong buffers has underflowed. This condition occurs when the ALP tries to read data from a host based CAR buffer whose Buffer Empty Bit in the Master Interrupt Register has not been reset. This error indicates that the ALP is reading the CAR Ping-Pong buffers faster than the host can load the buffers with data. NOTE: This bit is reset when the CAL/CAR Error Bit is reset in the Master Interrupt Register or the CAR Channel Enable bit is set to zero.
2	R	**CAR FIFO Underflow**: This active “high” bit indicates that the ALP based CAR FIFO has underflowed. Indicates PCI latency. NOTE: This bit is reset when the CAL/CAR Error Bit is reset in the Master Interrupt Register or the CAR Channel Enable bit is set to zero.
1	R/W	**CAL Channel Enable**: Setting this bit “high” enables the CAL channel to transfer data from the host based CAL buffers. Transfers always begin with buffer 1. Writing a ‘0’ to this bit clears the CAL FIFOs to empty and resets the CAL status bits in this register. NOTE: The bit in the Master Interrupt Register corresponding to the CAL/CAR status bits must be cleared explicitly.
0	R/W	**CAR Channel Enable**: Setting this bit “high” enables the CAR channel to transfer data from the host based CAR buffers. Transfers always begin with buffer 1. Writing a ‘0’ to this bit clears the CAR FIFOs to empty and resets the CAR status bits in this register. NOTE: The bit in the Master Interrupt Register corresponding to the CAL/CAR status bits must be cleared explicitly.
Default Value After Reset: 00 00 00 00		

3.1.2.7 Compressed Video Local/Remote Control Registers

3.1.2.7.1 Compressed Video Local/Remote (CVL/CVR) Buffers (Offset 70_{16} - 88_{16})

These registers contain the buffer configuration data required by the ALP to perform PCI master transfers of CVL/CVR data to/from buffers in PCI space.

BITS	TYPE	REGISTER DESCRIPTION
CVL BUFFER 1 ADDR (Offset 70_{16})		
31: 0	R/W	**CVL Buffer 1 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
CVL BUFFER 2 ADDR (Offset 74_{16})		
31: 0	R/W	**CVL Buffer 2 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
CVL BUFFER LENGTHS (Offset 78_{16})		
31	-	Reserved
30:16	R/W	**CVL Buffer 2 Length**: Buffer length in dwords. Data transfers will be halted when CVL Buffer 2 becomes the target buffer for data transfers and these bits are set to zero.
15	-	Reserved
14: 0	R/W	**CVL Buffer 1 Length**: Buffer length in dwords. Data transfers will be halted when CVL Buffer 1 becomes the target buffer for data transfers and these bits are set to zero.
Default Value After Reset: 00 00 00 00		
CVR BUFFER 1 ADDR (Offset $7C_{16}$)		
31: 0	R/W	**CVR Buffer 1 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
CVR BUFFER 2 ADDR (Offset 80_{16})		
31: 0	R/W	**CVR Buffer 2 Address**: Written by host to set buffer start address in PCI space.
Default Value After Reset: 00 00 00 00		
CVR BUFFER LENGTHS (Offset 84_{16})		
31	-	Reserved
30:16	R/W	**CVR Buffer 2 Length**: Buffer length in dwords. Data transfers will be halted when CVR Buffer 2 becomes the target buffer for data transfers and these bits are set to zero.
15	-	Reserved
14: 0	R/W	**CVR Buffer 1 Length**: Buffer length in dwords. Data transfers will be halted when CVR Buffer 1 becomes the target buffer for data transfers and these bits are set to zero.
Default Value After Reset: 00 00 00 00		
CVL/CVR BUFFER COUNT (Offset 88_{16})		
31	R	**CVL Target Buffer**: 1 = Count represents transfers to CVL Buffer 2 0 = Count represents transfers to CVL Buffer 1
30:16	R	**CVL Transfer Count**: Number of double words written to the target CVL Buffer. The register is incremented from 0 to a maximum value set by the CVL Buffer length register. When the terminal count is reached, a PCI interrupt is generated if enabled (see Master Interrupt register). The count is reset to zero when transfers begin to an empty buffer.
15	R	**CVR Target Buffer**: See CVL Target Buffer.
14:0	R	**CVR Transfer Count**: See CVL Transfer Count.
Default Value After Reset: 00 00 00 00		

3.1.2.7.2 CVL/CVR Control/Status Register (Offset $8C_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31: 6	-	Reserved
5	R	**CVL Buffer Overflow**: This active "high" bit indicates that one of the host based CVL ping-pong buffers has overflowed. This condition occurs when the ALP tries to write data to a host based CVL buffer whose Buffer Full Bit in the Master Interrupt Register has not been reset. This error indicates that the CVL Ping-Pong buffers are being written with data by the ALP faster than the host can process the data. NOTE: This bit is reset when the CVL/CVR Error Bit is reset in the Master Interrupt Register or the CVL Channel Enable bit is set to zero.
4	R	**CVL FIFO Overflow**: This active "high" bit indicates that the ALP based CVL FIFO has overflowed. Indicates a PCI latency problem. NOTE: This bit is reset when the CVL/CVR Error Bit is reset in the Master Interrupt Register or the CVL Channel Enable bit is set to zero.
3	R	**CVR Buffer Underflow**: This active "high" bit indicates that one of the host based CVR ping-pong buffers has underflowed. This condition occurs when the ALP tries to read data from a host based CVR buffer whose Buffer Empty Bit in the Master Interrupt Register has not been reset. This error indicates that the ALP is reading the CVR Ping-Pong buffers faster than the host can load the buffers with data. NOTE: This bit is reset when the CVL/CVR Error Bit is reset in the Master Interrupt Register or the CVR Channel Enable bit is set to zero.
2	R	**CVR FIFO Underflow**: This active "high" bit indicates that the ALP based CVR FIFO has underflowed. Indicates PCI latency. NOTE: This bit is reset when the CVL/CVR Error Bit is reset in the Master Interrupt Register or the CVR Channel Enable bit is set to zero.
1	R/W	**CVL Channel Enable**: Setting this bit "high" enables the CVL channel to transfer data from the host based CVL buffers. Transfers always begin with buffer 1. Writing a '0' to this bit clears the CVL FIFOs to empty and resets the CVL status bits in this register. NOTE: The bit in the Master Interrupt Register corresponding to the CVL/CVR status bits must be cleared explicitly.
0	R/W	**CVR Channel Enable**: Setting this bit "high" enables the CVR channel to transfer data from the host based CVR buffers. Transfers always begin with buffer 1. Writing a '0' to this bit clears the CVR FIFOs to empty and resets the CVR status bits in this register. NOTE: The bit in the Master Interrupt Register corresponding to the CVL/CVR status bits must be cleared explicitly.
Default Value After Reset: 00 00 00 00		

3.1.2.7.3 CVL/CVR Bit Rate Registers (Offset 90_{16} - 94_{16})

These registers are used to set the average bit rate for data transfers across the Compressed Video Bus. The bit rate is set by using the carry out of an NCO phase accumulator to enable the compressed video bus gating signals (CVGTI and CVGTO section 3.3). The gating signal frequency is equivalent to the bit rate. The 32-bit value loaded into the CVL/CVR Bit Rate Control registers determine the bit rates as given by:

Bit Rate = 27MHz * (BRC)/2^{32}

where 27MHz is the system clock and BRC is the 32-bit control value. This provides a bit rate resolution of 0.006Hz. The upper 3 bits of the Bit Rate Control registers are hard coded to zero to limit the maximum bit rate (see register descriptions). The gating signal and the 2.048MHz Compressed Video Clock (CVCLK) must be synchronized. The gating signal may extend over multiple CVCLKs for a burst mode of operation. The burst length will be less than 32 bits and will be determined by Design. Note: the maximum bit rate across the compressed video bus is determined by the compressed video clock (CVCLK).

BITS	TYPE	REGISTER DESCRIPTION
CVL BIT RATE CONTROL (Offset 90_{16})		
31: 0	R/W	**CVL Bit Rate Control**: 32-bit frequency control value for enabling CVGTL. NOTE: The 3 MSBs of this register are hard coded to zero to limit the bit rate to a maximum value of ~3.375MHz using a 27MHz clock. (1F FF FF FF/2^{32}) * 27e6
Default Value After Reset: 00 00 00 00		
CVR BIT RATE CONTROL (Offset 94_{16})		
31: 0	R/W	**CVR Bit Rate Control**: 32-bit frequency control value for enabling CVGTR (same as CVL Bit Rate Control).
Default Value After Reset: 00 00 00 00		

3.1.2.8 Uncompressed Video Interface Registers

These registers are used to set up uncompressed video data transfers between the ALP and host based frame buffers or a PCI resident GUI. Uncompressed video is received from the Px64 chip at a rate of up to 30 frames/sec via the Uncompressed Video Interface (see Section 6.x.x). Typically, two video sources (Local and Remote) are multiplexed into the even and odd video fields comprising each frame output from the Px64. The ALP uses the FIELD input from the Px64 to direct the video data to even and odd field buffers in PCI space.

3.1.2.8.1 Even/Odd Uncompressed Video Field Buffer Control (Offset 98_{16} - $C0_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
EVEN FIELD BUFFER 1 ADDRESS (Offset 98_{16})		
31:0	R/W	**Even Field Buffer 1 Address**: Written by host to set buffer start address in PCI space. Video data input to the ALP while FIELD = 0 is written to this buffer. NOTE: Lower 2 bits of this address are hard coded to zero to force double word boundary. The lowest two bits read as zero.
Default Value After Reset: 00 00 00 00		
EVEN FIELD BUFFER 2 ADDRESS (Offset $9C_{16}$)		
31: 0	R/W	**Even Field Buffer 2 Address**: Same as Even Field Buffer 1 Address.
Default Value After Reset: 00 00 00 00		
LINES PER EVEN FIELD (Offset $A0_{16}$)		
31:12	-	Reserved
11:0	R/W	**Lines Per Field**: This register specifies the number of lines per even video field.
Default Value After Reset: 00 00 00 00		
EVEN FIELD LINE LENGTH/LINE GAP (Offset $A4_{16}$)		
31:28	-	Reserved
27:16	R/W	**Line Length**: Number of double words per line of even field video.
15:12	-	Reserved
11:0	R/W	**Line Gap**: This value is used to indicate the gap in dwords between video lines in the PCI field buffer memory.
Default Value After Reset: 00 00 00 00		
EVEN FIELD DROP COUNT/RGB ALPHA (Offset $A8_{16}$)		
31:12	-	Reserved
11:8	R/W	**Field Drop Count**: This value specifies the number of fields to drop for each field written to the PCI. For example, 0 = all fields written, 1 = one field dropped for each field written, 2 = two fields dropped for each field written, etc.
7:0	R/W	**RGB Alpha**: Fading constant for RGB Alpha Mode. See section 5.x.x for data packing.
Default Value After Reset: 00 00 00 00		
ODD VIDEO FIELD BUFFER 1 ADDRESS (Offset AC_{16})		
31:0	R/W	**Odd Field Buffer 1 Address**: Same as Even Field Buffer 1 Address except FIELD = 1.
Default Value After Reset: 00 00 00 00		
ODD VIDEO FIELD BUFFER 2 ADDRESS (Offset $B0_{16}$)		

BITS	TYPE	REGISTER DESCRIPTION
31: 0	R/W	**Odd Field Buffer 2 Address**: Same as Odd Field Buffer 1 Address.
Default Value After Reset: 00 00 00 00		
LINES PER ODD FIELD (Offset $B4_{16}$)		
31:12	-	Reserved
11:0	R/W	**Lines Per Field**: Functions the Same as Lines Per Even Field.
Default Value After Reset: 00 00 00 00		
ODD FIELD LINE LENGTH/ODD FIELD LINE GAp (Offset $B8_{16}$)		
31:28	-	Reserved
27:16	R/W	**Line Length**: Functions the same as Even Field Line Length.
15:12	-	Reserved
11:0	R/W	**Line Gap**: Functions the same as Even Field Line Gap.
Default Value After Reset: 00 00 00 00		
ODD FIELD DROP COUNT/ODD FIELD RGB ALPHA (Offset BC_{16})		
31:12	-	Reserved
11:8	R/W	**Field Drop Count**: Functions the same as Even Field Drop Count.
7:0	R/W	**RGB Alpha**: Functions the same as Even Field RGB Alpha.
Default Value After Reset: 00 00 00 00		
LINE COUNT (Offset $C0_{16}$)		
31:14	-	Reserved
13	R	**Active Video Field**: 1 = Odd field data is being transferred. 0 = Even field data is being transferred.
12	R	**Target Buffer Indicator**: 1 = Field Buffer 2 is the target buffer. 0 = Field Buffer 1 is the target buffer.
11:0	R	**Line Count**: This register contains the number of video lines transferred to the target buffer for the current active video field. The number is incremented from 0 to a maximum value set by Lines Per Field register for the active video field.
Default Value After Reset: 00 00 00 00		

3.1.2.8.2 Uncompressed Video Control/Status (Offset $C4_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31:30	-	Reserved
29	R	**Even Field FIFO Overflow**: This active "high" bit indicates that the ALP based UV even field FIFO has overflowed. NOTE: This bit is reset when the UV FIFO Overflow Bit is reset in the Master Interrupt Register.
28	R/W	**Even Field FIFO Overflow Handling**: 1 Continue writing after FIFO overflow, and wait for VSYNC to terminate buffer transfer. (Details by Design) 0 On FIFO overflow, halt transfers to buffer memory and wait for VSYNC to initiate transfers to the appropriate buffer indicated by FIELD.
27:24	R/W	**Even Field Number 1**: These bits are loaded with the contents of the field counter when a field transfer to the Even Video Field Buffer 1 is complete. NOTE: The Field Counter increments with the assertion of VSYNC.
23:20	R/W	**Even Field Number 2**: These bits are loaded with the contents of the Field Counter when a field transfer to the Even Video Field Buffer 2 is complete.
19	R/W	**Even Field Alpha Mode Enable**: 1 RGB Alpha mode enabled, alpha mode video bytes packed into dword. 0 Alpha mode disabled, uncompressed video packed into dwords.
18	R/W	**Even Field Capture Mode**: 1 Non-Continuous Capture: Even fields are captured to the enabled even field buffers. Once a buffer is filled, the corresponding buffer full bit is set and writing to that buffer is disabled. Data transfers are re-enabled by resetting the corresponding buffer full bit in the Master Interrupt register. 0 Continuous Capture: Video data is continuously captured to the enabled Even Field Buffers without host interaction. Writing to buffers are not disabled on buffer full condition.
17	R/W	**Even Field Buffer 2 Enable**: Enables Buffer 2 as a data transfer target. '1' enables buffer, '0' disables buffer. NOTE: A buffer must be disabled before changing any of the configuration registers (buffer address, line length, etc.). NOTE: Data transfers to a particular buffer are only possible if the buffer is enabled and the buffer full bit is not active.
16	R/W	**Even Field Buffer 1 Enable**: See Even Field Buffer 2 Enable Description.
15:14	-	Reserved
13	R	**Odd Field FIFO Overflow**: This active "high" bit indicates that the ALP based UV odd field FIFO has overflowed. NOTE: This bit is reset when the UV FIFO Overflow Bit is reset in the Master Interrupt Register.
12	R/W	**Odd Field FIFO Overflow Handling**: See Even Field FIFO Overflow Description.
11:8	R/W	**Odd Field Number 1**: See Even Field Number Description.
7:4	R/W	**Odd Field Number 2**: See Even Field Number Description.
3	R/W	**Odd Field Alpha Mode Enable**: See Even Field Alpha Mode Description.
2	R/W	**Odd Field Capture Mode**: See Even Field Capture Mode Description.
1	R/W	**Odd Field Buffer 2 Enable**: See Even Field Buffer 2 Enable Description.
0	R/W	**Odd Field Buffer 1 Enable**: See Even Field Buffer 1 Enable Description.
Default Value After Reset: 00 00 00 00		

3.1.2.8.3 Video Channel Block Size Register (Offset $C8_{16}$)

BITS	TYPE	REGISTER DESCRIPTION
31:6	-	Reserved
5:0	R/W	**Video Channel Block Size**: This register is used to specify the desired block size for PCI Master transfers of video data in dwords.
Default Value After Reset: 00 00 00 08		

3.1.2.9 Annex D to I/O Bus Interface

This interface supports the transfer of Annex D data to the Px64 via the I/O Bus.

3.1.2.9.1 Annex D Buffers (Offset CC_{16} - $D8_{16}$)

These registers contain the buffer configuration data required by the ALP to perform PCI master transfers of Annex D data between host memory and the Px64. Note: before changing any of the following buffer configuration registers, Annex D transfers to the buffers must be disabled by clearing the enable bit in the Annex D Control/Status Register or writing a zero to the buffer length registers associated with Annex D Buffer 1 and 2.

BITS	TYPE	REGISTER DESCRIPTION
ANNEX D BUFFER 1 ADDR (Offset CC_{16})		
31: 0	R/W	**Annex D Buffer 1 Address**: Written by host to set buffer start address in PCI space. Note: the 2 LSBs of this address are hard coded to zero to force dword boundary, and these two bits read as zero.
Default Value After Reset: 00 00 00 00		
ANNEX D BUFFER 2 ADDR (Offset $D0_{16}$)		
31: 0	R/W	**Annex D Buffer 2 Address**: Written by host to set buffer start address in PCI space. Note: the 2 LSBs of this address are hard coded to zero to force dword boundary, and these two bits read as zero.
Default Value After Reset: 00 00 00 00		
ANNEX D BUFFER LENGTHS (Offset $D4_{16}$)		
31	-	Reserved
30:16	R/W	**Annex D Buffer 2 Length**: Buffer length in dwords. Writing zero to this register disables the buffer for transfers.
15	-	Reserved
14: 0	R/W	**Annex D Buffer 1 Length**: Buffer length in dwords. Writing a zero to this register disables the buffer for transfers.
Default Value After Reset: 00 00 00 00		
ANNEX D BUFFER COUNT (Offset $D8_{16}$)		
31:16	-	Reserved
15	R	**Annex D Target Buffer**: 1 = Count represents transfers to Annex D Buffer 2 0 = Count represents transfers to Annex D Buffer 1
14:0	R	**Annex D Transfer Count**: Number of double words written/read to/from the target Annex D Buffer. The register is incremented from 0 to a maximum value set by the Annex D Buffer length register. When the terminal count is reached, a PCI interrupt is generated if enabled (see Master Interrupt register). The count is reset to zero when transfers begin to an empty buffer.
Default Value After Reset: 00 00 00 00		

3.1.2.9.2 Annex D Control/Status Register (Offset DC_{16})

BITS	TYPE	REGISTER DESCRIPTION
31:16	-	Reserved
15	R	**Annex D Remote FIFO Empty**: This active “high” bit indicates that the ALP Annex D Remote FIFO is empty. This is a status bit that reflects the FIFO status and does not have a reset.
14	R	**Annex D Buffer Over/Under flow**: This active “high” bit indicates that one of the host based Annex D ping-pong buffers has overflowed. This condition occurs when the ALP tries to write/read Annex D data to/from the host but neither of the Annex D ping-pong buffers are enabled. Indicates host can’t keep up. Note: this bit is reset when the Annex D Error Bit is reset in the Master Interrupt Register.
13	R	**Annex D FIFO Over/Under Flow**: This active “high” bit indicates that the FIFOs used by the ALP to transfer Annex D data have either over or underflowed depending on the direction of the data transfer. In either case, this bit indicates that the Annex D data has been corrupted.
12:10	R/W	**I/O Bus Request**: Identifies which I/O Bus request line will be asserted by the Px64 chip. For example, 011 b indicates that IORQ3 will be used by the Px64 to request data. (default value = 100)
9	R/W	**Annex D Direction**: 1 = Annex D data transferred from Px64 to host 0 = Annex D data transferred from host to Px64
8	R/W	**Annex D Channel Enable**: Setting this bit “high” enables the Annex D channel. Writing a ‘0’ to this bit clears the Annex D FIFOs to empty and resets the Annex D status bits in this register. NOTE: The bit in the Master Interrupt Register corresponding to the Annex D status bits must be cleared explicitly.
7:0	R/W	**I/O Bus Address**: 8-bit I/O Bus address (see section).
Default Value After Reset: 00 00 10 EF		

3.1.2.10 DSP Debug Interface

3.1.2.10.1 DSP Debug Control Register (Offset $E0_{16}$)

The DSP Debug Control register contains control bits analogous to the DSP Group CDI interface that facilitate DSP software debugging over the PCI Bus.

BITS	TYPE	REGISTER DESCRIPTION
SLAVE DSP DEBUG REGISTER		
31:30	-	Reserved
29	R/W	**Slave DSP Outgoing Mailbox FIFO mask**. Setting mask to '1' allows flag to pass to interrupt.
28	R/W	**Slave DSP Incoming Mailbox FIFO mask**. Setting mask to '1' allows flag to pass to interrupt.
27:26	-	Reserved
25	R/RST	**Slave DSP Outgoing Mailbox FIFO flag**: ALP sets "high" to indicate message available. Host resets when message read. Writing '1' resets.
24	R/RST	**Slave DSP Incoming Mailbox FIFO flag**: ALP sets "high" when FIFO empty. Host resets when FIFO contains new message. Writing '1' resets.
23:21	-	Reserved
20	R/W	**Slave DSP WDT Override**: High active signal that prevents the Slave WDT from resetting the DSPs.
19	R/W	**Slave DSP Boot**: Slave DSP boot address selector (0 = 0000_{16}, 1 = $FFFE_{16}$).
18	R/W	**Slave DSP Debug**: High active signal that enables the Slave DSP OCEM.
17	R/W	**Slave DSP Reset**: Low active signal that resets the Slave DSP.
16	R/W	**Slave DSP Abort**: Low active signal that forces the Slave DSP to take a TRAP vector. The monitor code begins running once this vector is taken.
MASTER DSP DEBUG REGISTER		
15:14	-	Reserved
13	R/W	**Master DSP Outgoing Mailbox FIFO mask**. Setting mask to '1' allows flag to pass to interrupt.
12	R/W	**Master DSP Incoming Mailbox FIFO mask**. Setting mask to '1' allows flag to pass to interrupt.
11:10	-	Reserved
9	R/RST	**Master DSP Outgoing Mailbox FIFO flag**: ALP sets "high" to indicate message available. Host resets when message read. Writing '1' resets.
8	R/RST	**Master DSP Incoming Mailbox FIFO flag**: ALP sets "high" when FIFO empty. Host resets when FIFO contains new message. Writing '1' resets.
7:5	-	Reserved
4	R/W	**Master DSP WDT Override**: High active signal that prevents the Master WDT from resetting the DSPs.
3	R/W	**Master DSP Boot**: Master DSP boot address selector (0 = 0000_{16}, 1 = $FFFE_{16}$).
2	R/W	**Master DSP Debug**: High active signal that enables the Master DSP OCEM.
1	R/W	**Master DSP Reset**: Low active signal that resets the Master DSP.
0	R/W	**Master DSP Abort**: Low active signal that forces the Master DSP to take a TRAP vector. The monitor code begins running once this vector is taken.
Default Value After Reset: 01 03 01 03		

3.1.2.10.2 Master DSP Debug Mailbox FIFOs (Offset $E4_{16}$)

The mailbox data register is used to transfer "messages" between the Master DSP's monitor software and the debugger software on the host. A write to this register goes into an incoming message FIFO while reading this register pulls data out of an outgoing message FIFO. The FIFOs support messages up to 32 words (64 bytes) in length. Each message transfer is 2 bytes to match the data path of the DSPs, and to avoid packing and unpacking. The message length is defined by the type of message being transferred.

BITS	TYPE	REGISTER DESCRIPTION
31	R	**DSP to Host FIFO Empty**: This bit, when high, indicates that the current value being read is not valid because the FIFO went empty.
30:16	-	Reserved
15:0	R/W	**Message Data**: Each message transfer is 2 bytes to match the data path of the DSPs, and to avoid packing and unpacking on both the host and ALP.
Default Value After Reset: 80 00 00 00		

3.1.2.10.3 Slave DSP Debug Mailbox FIFOs (Offset $E8_{16}$)

The mailbox data register is used to transfer "messages" between the Slave DSP's monitor software and the debugger software on the host. A write to this register goes into an incoming message FIFO while reading this register pulls data out of an outgoing message FIFO. The FIFOs support messages up to 32 words (64 bytes) in length. Each message transfer is 2 bytes to match the data path of the DSPs, and to avoid packing and unpacking. The message length is defined by the type of message being transferred.

BITS	TYPE	REGISTER DESCRIPTION
31	R	**DSP to Host FIFO Empty**: This bit, when high, indicates that the current value being read is not valid because the FIFO went empty.
30:16	-	Reserved
15:0	R/W	**Message Data**: Each message transfer is 2 bytes to match the data path of the DSPs, and to avoid packing and unpacking on both the host and ALP.
Default Value After Reset: 80 00 00 00		

4.0 Timing Diagrams

4.1 Pin Timing

4.1.1 SRAM Interface - Signals to Off-Chip Memory

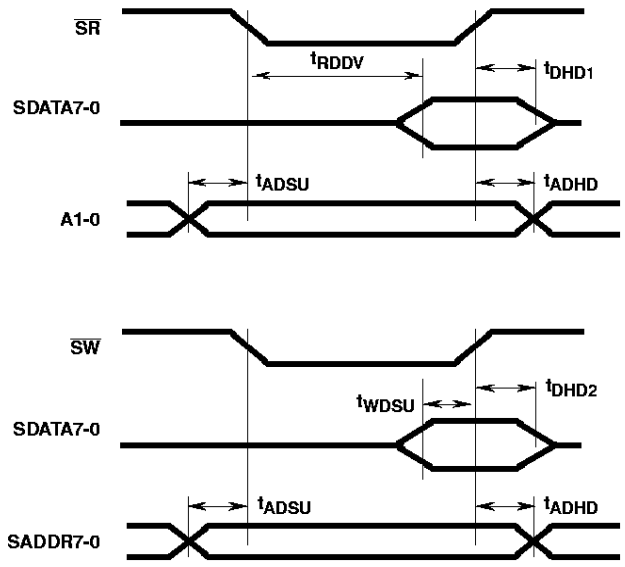


FIGURE 4-1. SRAM INTERFACE PIO READ CYCLE

4.1.2 IOB (I/O Bus) - a.k.a. PCB or Host Bus

4.1.2.1 I/O Bus Signal Timing

The I/O Bus shall support four distinct bus cycles: programmed I/O (PIO) read, PIO write, direct memory access (DMA) read, and DMA write. Note that read and write designations are with respect to the master device.

DMA cycles shall directly access the Status and Direct Data registers. The I/O Bus shall support single and multiple byte DMA cycles. Target devices which support both read and write DMA accesses shall use the $\overline{IORD}$ or $\overline{IOWR}$ signal to determine the appropriate registers to be accessed.

Any type of cycle can be extended by a target device through the use of the $\overline{IOWAIT}$ signal.

4.1.2.1.1 I/O Bus PIO Read Cycle Timing

PIO read cycles (Figure 4-2) shall start with a write cycle to the Index Address register, followed by the read cycle of the Indexed Data register. Note that the two cycles do not have to be contiguous I/O Bus cycles. Successive accesses of the same internal register are permissible without the need for writing to the Index Address register.

4.1.2.1.2 I/O Bus PIO Write Cycle Timing

PIO write cycles (Figure 4-3) shall start with a write cycle to the Index Address register, followed by the write cycle to the Indexed Data register. Note that the two cycles do not have to be contiguous I/O Bus cycles. Successive accesses of the same internal register are permissible without the need for writing to the Index Address register.

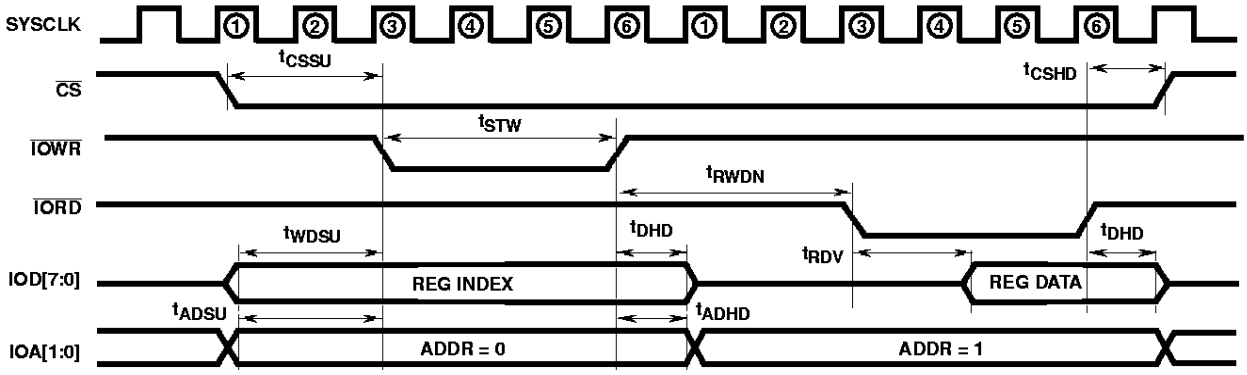


FIGURE 4-2. PIO READ CYCLE

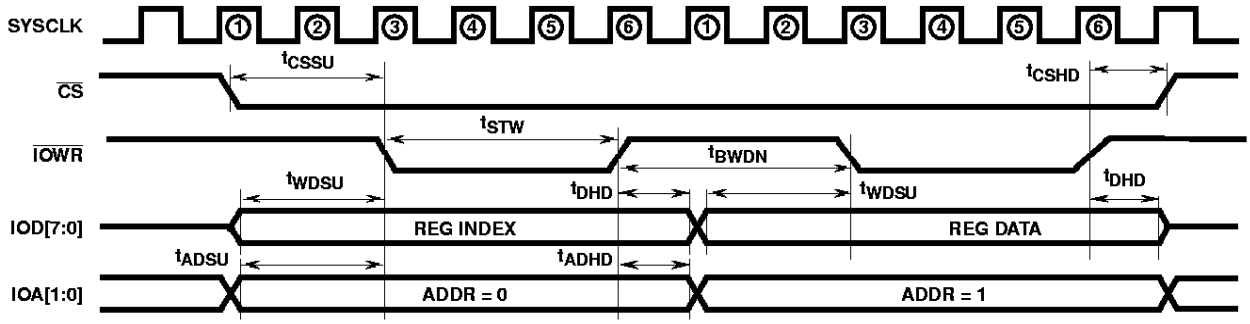


FIGURE 4-3. PIO WRITE CYCLE

4.1.2.1.3 I/O Bus DMA Read Cycle Timing

DMA Read Cycles (Figure 4-4) shall be limited to accessing the PIO Data register on target devices.

4.1.2.1.4 I/O Bus DMA Write Cycle Timing

DMA Write Cycles (Figure 4-5) shall be limited to accessing the PIO Data register on target devices.

4.1.2.1.5 I/O Bus DMA Read Cycle with $\overline{\text{WAIT}}$ Timing

The $\overline{\text{WAIT}}$ signal is used to extend bus cycles for slower devices as illustrated in Figure 4-6. While the illustration shows the DMA Read Cycle, all four cycle types may be extended in this fashion. The target device shall assert the $\overline{\text{IOWAIT}}$ signal t_{WAIT} seconds after it detects the $\overline{\text{IORD}}$ signal.

4.1.2.1.6 I/O Bus Multiple Byte DMA Read Cycle Timing

Figure 4-7 illustrates a two byte DMA Read Cycle. The I/O Bus shall support multiple byte transfers for both DMA Read and DMA Write cycles. The number of bytes transferred shall be controlled by the presence of the target device's RQ signal. The target device's RQ signal shall go inactive t_{RQHD} seconds after the target detects the $\overline{\text{IORD}}$ signal for the last byte in the transfer.

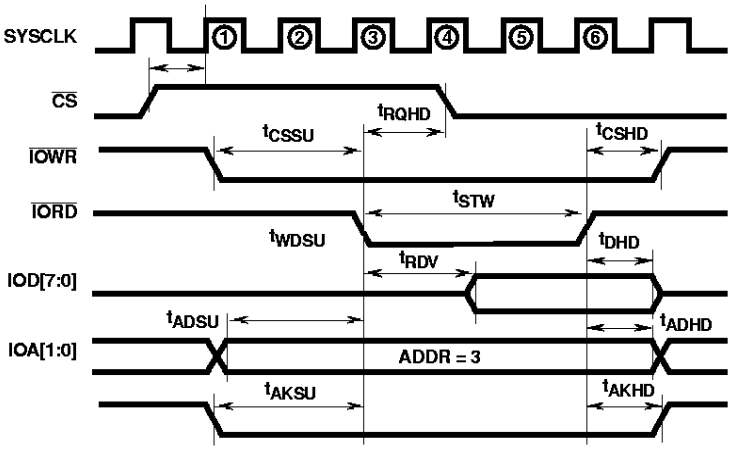


FIGURE 4-4. DMA READ CYCLE

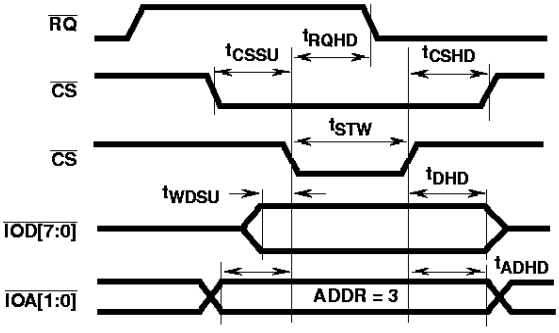


FIGURE 4-5. DMA WRITE CYCLE

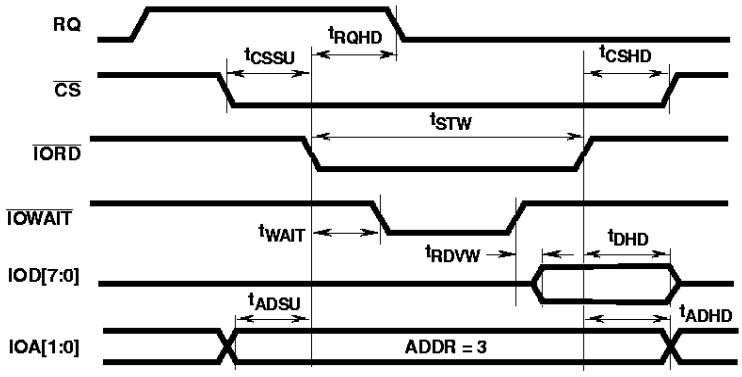


FIGURE 4-6. DMA READ CYCLE WITH $\overline{\text{IOWAIT}}$

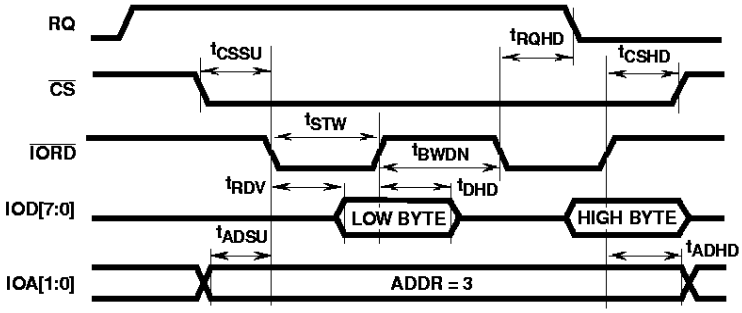


FIGURE 4-7. MULTIPLE BYTE DMA READ CYCLE

4.1.2.1.7 I/O Bus Absolute Timing

The absolute times for the bus cycles illustrated above are shown in Table 4-1.

TABLE 4-1. I/O BUS ABSOLUTE TIMING PARAMETERS

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{Φ}	I/O Bus Cycle phase period	1/27MHz	-	ns
t_{STW}	$\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ strobe width	$3t_{\Phi}$	-	ns
t_{BWDN}	Time from rising edge of $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ to the next falling edge of $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$	$3t_{\Phi}$	-	ns
t_{WDSU}	Data Valid to $\overline{\text{IOWR}}$ falling edge (write cycle)	$2t_{\Phi}$	-	ns
t_{RDV}	$\overline{\text{IORD}}$ falling edge to data valid (read cycle)	$1.5t_{\Phi}$	-	ns
t_{RDSUW}	$\overline{\text{IOWAIT}}$ rising edge to data valid (wait read cycle)	-	$0.5t_{\Phi}$	ns
t_{DHD}	Data hold from $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ rising edge	0	$1t_{\Phi}$	ns
t_{CSSU}	$\overline{\text{CS}}$ setup to $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ falling edge	$2t_{\Phi}$	-	ns
t_{CSHD}	$\overline{\text{CS}}$ hold from $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ rising edge	$1t_{\Phi}$	-	ns
t_{ADSU}	IOA<> setup to $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ falling edge	$2t_{\Phi}$	-	ns
t_{ADHD}	IOA<> hold from $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ rising edge	$1t_{\Phi}$	-	ns
t_{RQHD}	IORQ hold from $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ falling edge	-	$0.5t_{\Phi}$	ns
t_{WAIT}	Time from $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ falling edge to $\overline{\text{IOWAIT}}$ falling edge	$1.5t_{\Phi}$		ns

4.1.3 MVIP/IOM2 - Connection to the Telephone Board

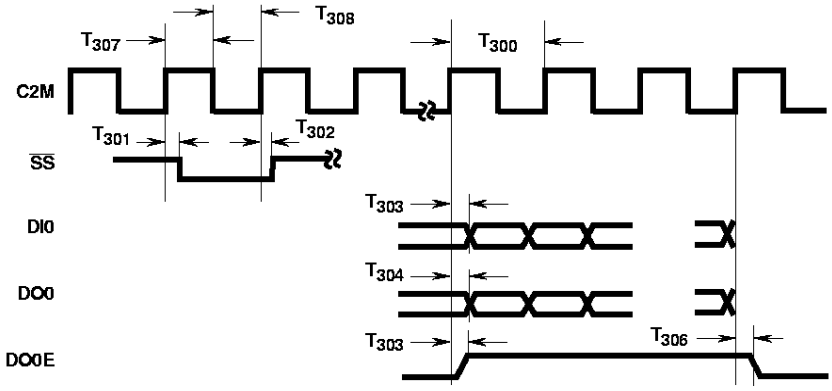


FIGURE 4-8.

4.1.4 PCI - Connection to the Host Computer System

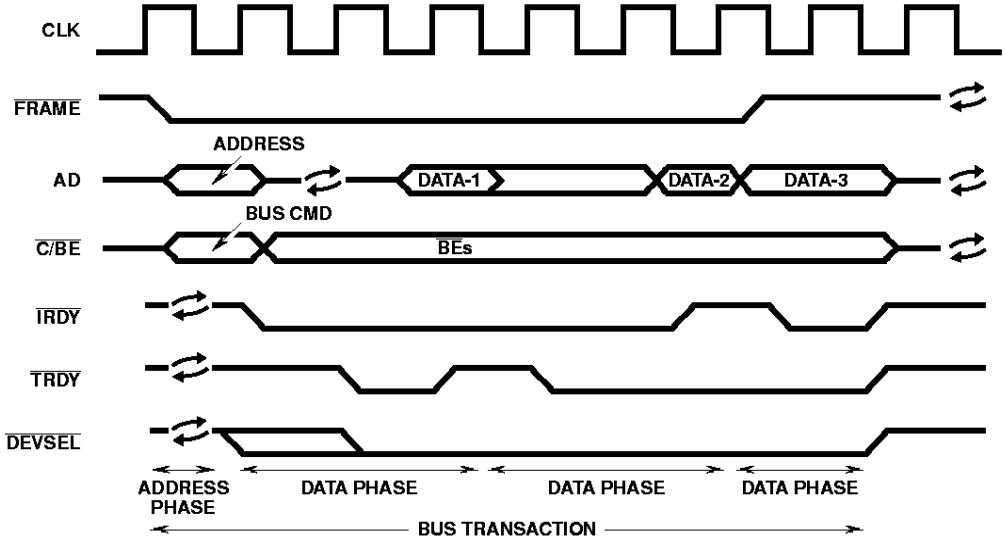


FIGURE 4-9. BASIC READ OPERATION

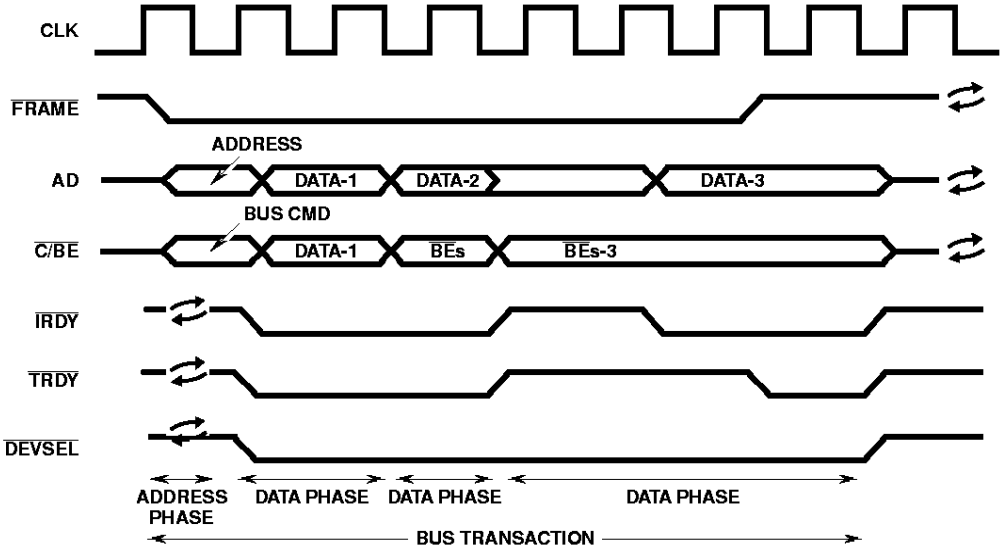


FIGURE 4-10. BASIC WRITE OPERATION

4.1.5 Uncompressed (Raw) Video

4.1.6 Compressed Video

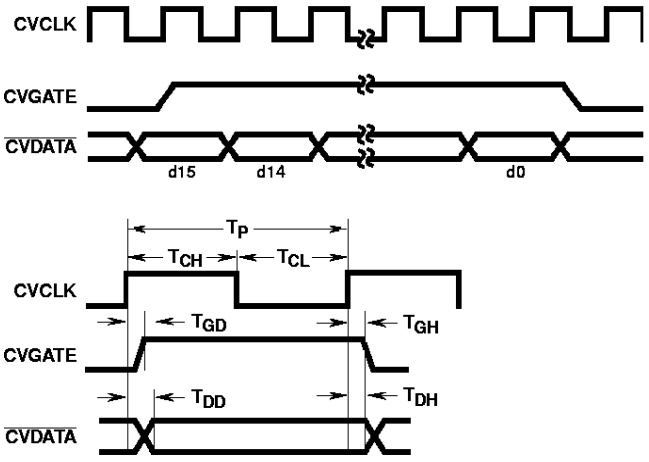


FIGURE 4-11.

4.1.6.1 CVB Transfer Protocol

The signaling protocol required to effect a master read compressed video data transfer is shown in Figure 4-12. The master shall use the falling edge of CVCLK to latch in data when CVGTL is high. The corresponding master write is illustrated in Figure 4-13. The slave shall use the falling edge of CVCLK to latch in data when CVGTR is high.

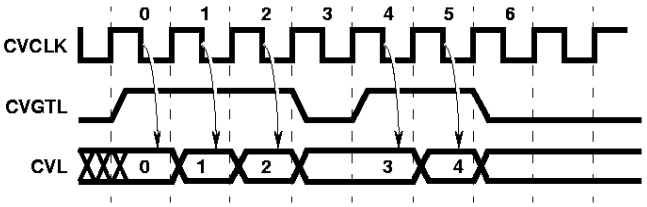


FIGURE 4-12. CVB MASTER READ

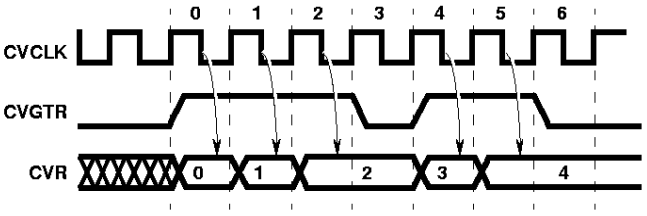


FIGURE 4-13. CVB MASTER WRITE

4.1.7 I^2C - Serial Control Bus

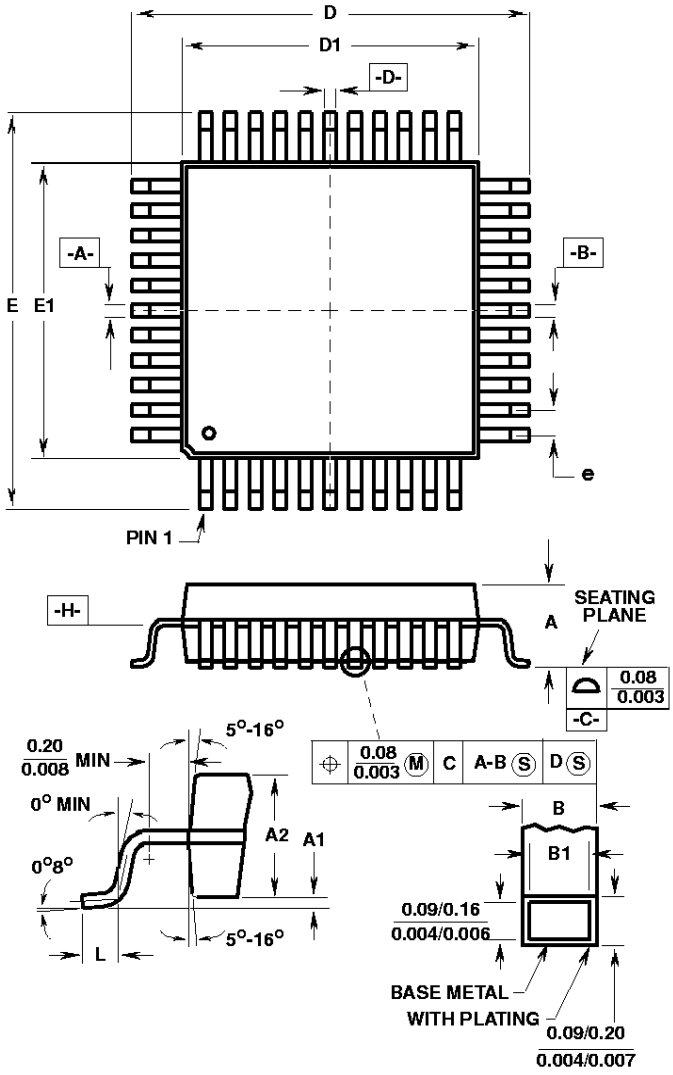
4.1.8 Miscellaneous

4.1.9 Supply

4.2 External Cycle Timing

4.3 Internal Cycle Timing

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q208.28x28

208 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.161	-	4.10	-
A1	0.010	-	0.25	-	-
A2	0.126	0.141	3.20	3.60	-
B	0.007	0.010	0.17	0.27	6
B1	0.007	0.009	0.17	0.23	-
D	1.197	1.212	30.40	30.80	3
D1	1.095	1.110	27.80	28.20	4, 5
E	1.197	1.212	30.40	30.80	3
E1	1.095	1.110	27.80	28.20	4, 5
L	0.018	0.029	0.45	0.75	-
N	208		208		7
e	0.020 BSC		0.50 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.
8. Dimensions conform to JEDEC outline MO-143 Issue C.

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Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
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ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
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