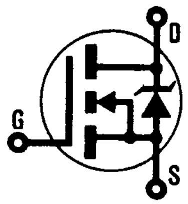
Data Sheet No. PD-9.527A

INTERNATIONAL RECTIFIER IOR

T-39-15

REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET® TRANSISTORS

IRF644
IRF645



N-CHANNEL

TO-220

250 Volt, 0.28 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

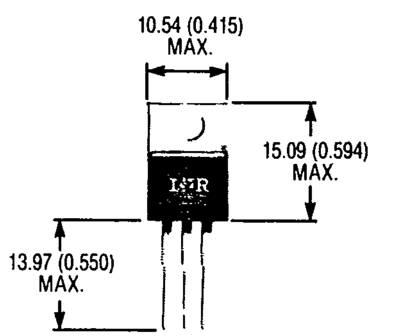
Product Summary

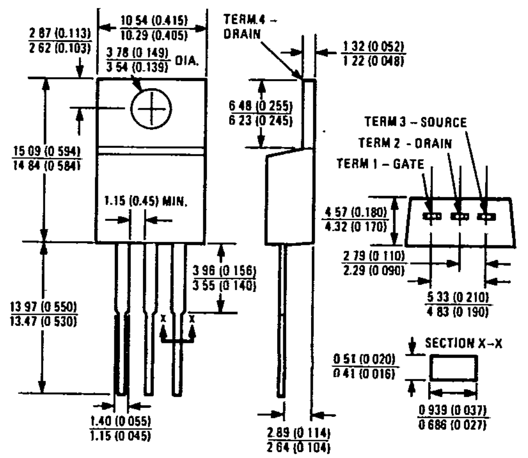
Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRF644	250V	0.28Ω	14A
IRF645	250V	0.34Ω	13A

FEATURES:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

CASE STYLE AND DIMENSIONS



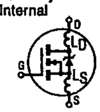


Case Style TO-220AB
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter		IRF644	IRF645	Units
I_D @ T_C = 25°C	Continuous Drain Current	14	13	A
I_D @ T_C = 100°C	Continuous Drain Current	8.8	8.0	A
I_{DM}	Pulsed Drain Current ①	56	52	A
P_D @ T_C = 25°C	Max. Power Dissipation	125		W
	Linear Derating Factor	1.0		W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	550 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	14 (See E_{AR})		A
E_{AR}	Repetitive Avalanche Energy ①	13 (See I_{AR})		mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.8 (See Fig. 17)		V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRF644 IRF645	250	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ④	IRF644	—	0.25	0.28	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF645	—	0.28	0.34		
$I_{D(on)}$	On-State Drain Current ④	IRF644	14	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ Max. V_{GS} = 10V
		IRF645	13				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ④	ALL	6.7	10	—	S(℧)	V_{DS} ≥ 50V, I_{DS} = 8.0A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 × Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	—	39	59	nC	V_{GS} = 10V, I_D = 14A,
Q_{gs}	Gate-to-Source Charge	ALL	—	6.6	9.9	nC	V_{DS} = 0.8 × Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	20	30	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	24	ns	V_{DD} = 125V, I_D ≈ 14A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	67	100	ns	R_D = 9.1Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	53	80	ns	See Fig. 15
t_f	Fall Time	ALL	—	49	74	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	320	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	69	—	pF	See Fig. 10

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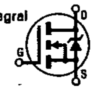
Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	14	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	56	A	
V_{SD}	Diode Forward Voltage ④	ALL	–	–	1.8	V	T_J = 25°C, I_S = 14A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	150	300	640	ns	T_J = 25°C, I_F = 14A, dI/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.6	3.4	7.2	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W⑤	
R_{thCS}	Case-to-Sink	ALL	–	0.50	–	K/W⑤	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W⑤	Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.6mH, R_G = 25Ω, Peak I_L = 14A

③ I_{SD} ≤ 14A, di/dt ≤ 150 A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C Suggested R_G = 9.1Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ K/W = °C/W W/K = W/°C

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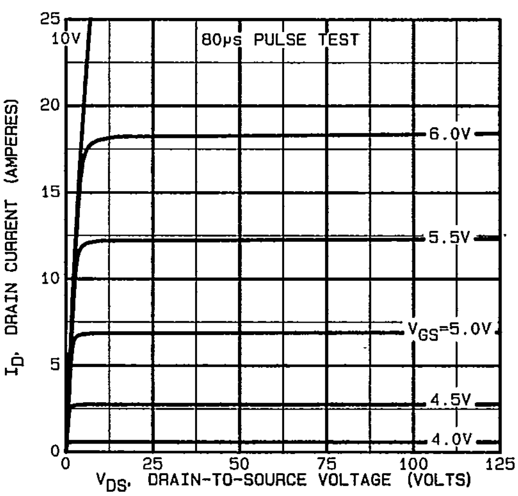

Fig. 1 — Typical Output Characteristics

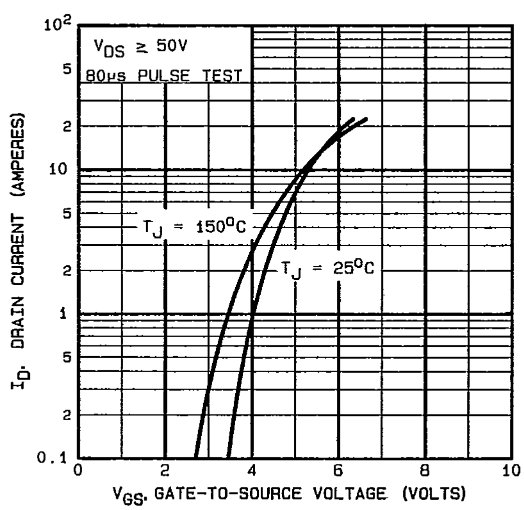

Fig. 2 — Typical Transfer Characteristics

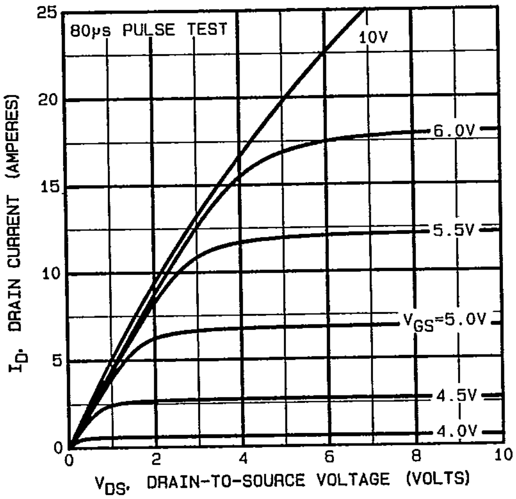

Fig. 3 — Typical Saturation Characteristics

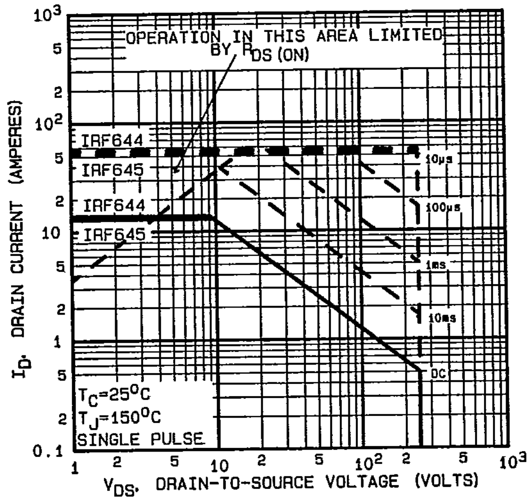

Fig. 4 — Maximum Safe Operating Area

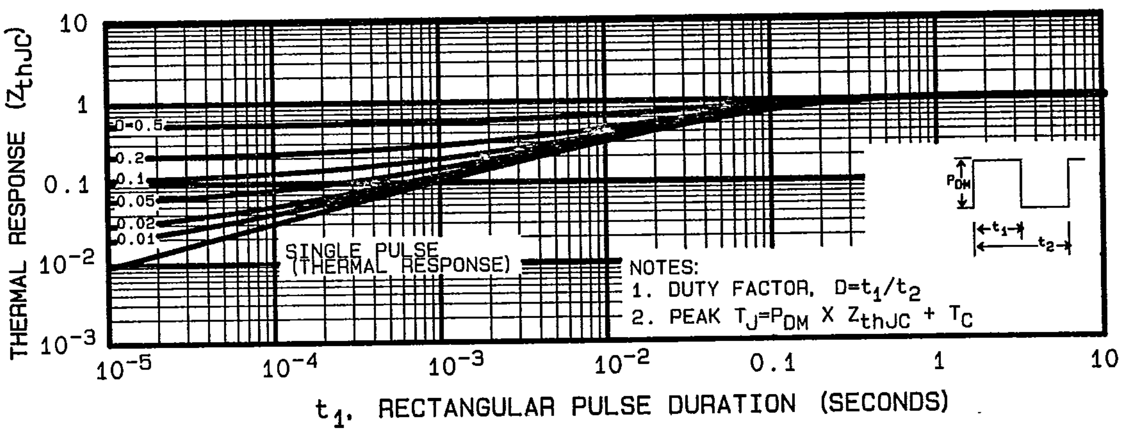

Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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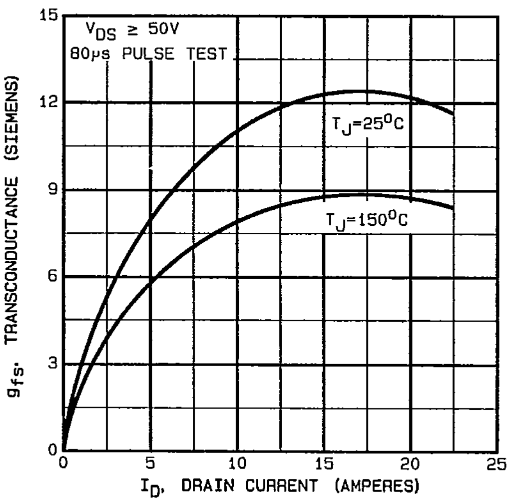

Fig. 6 — Typical Transconductance Vs. Drain Current

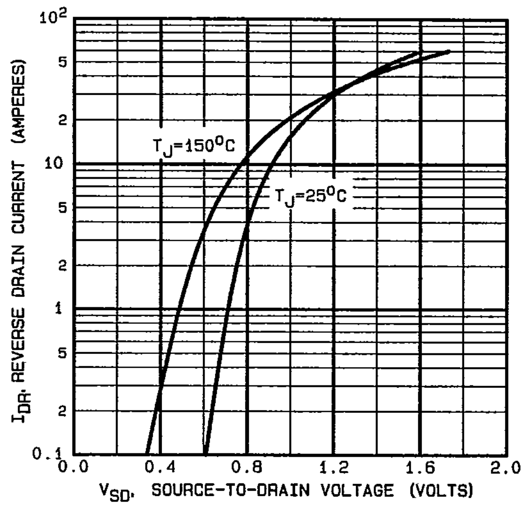

Fig. 7 — Typical Source-Drain Diode Forward Voltage

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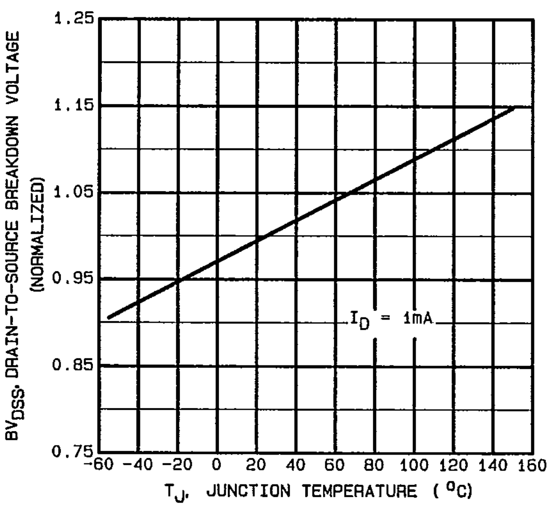

Fig. 8 — Breakdown Voltage Vs. Temperature

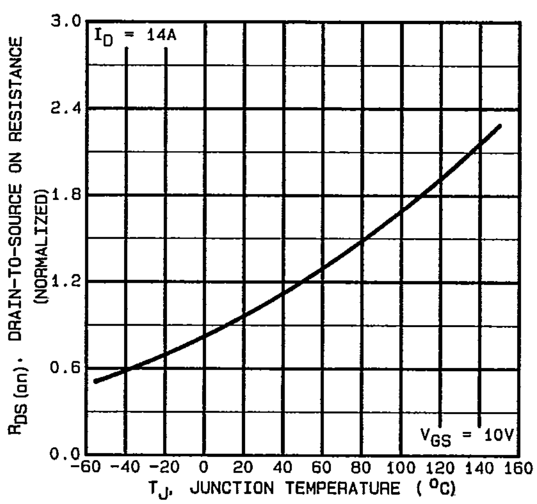

Fig. 9 — Normalized On-Resistance Vs. Temperature

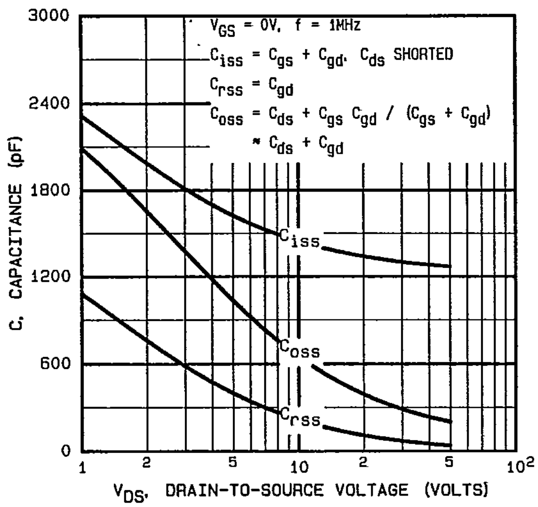

Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

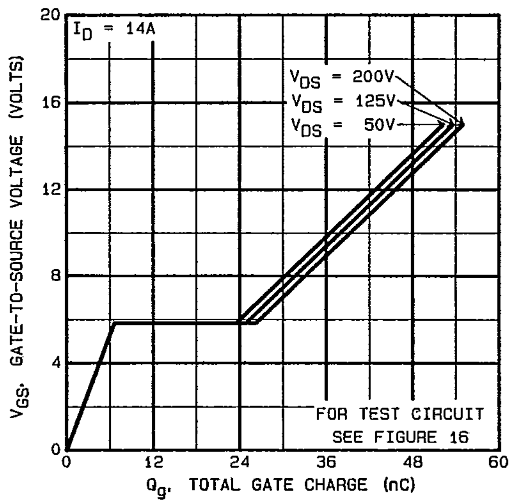

Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

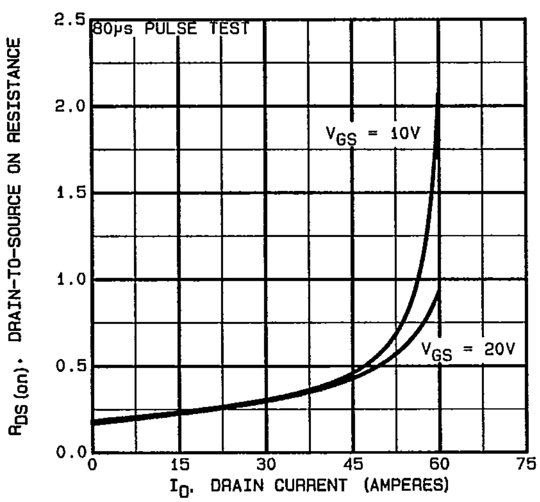

Fig. 12 — Typical On-Resistance Vs. Drain Current

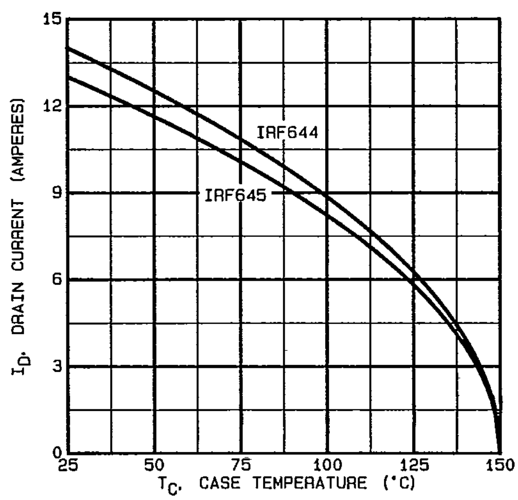

Fig. 13 — Maximum Drain Current Vs. Case Temperature

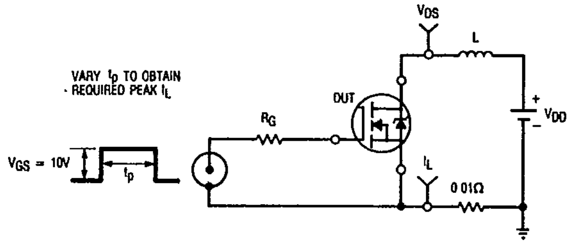

Fig. 14a — Unclamped Inductive Test Circuit

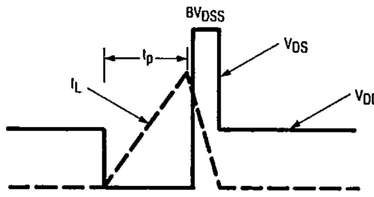

Fig. 14b — Unclamped Inductive Waveforms

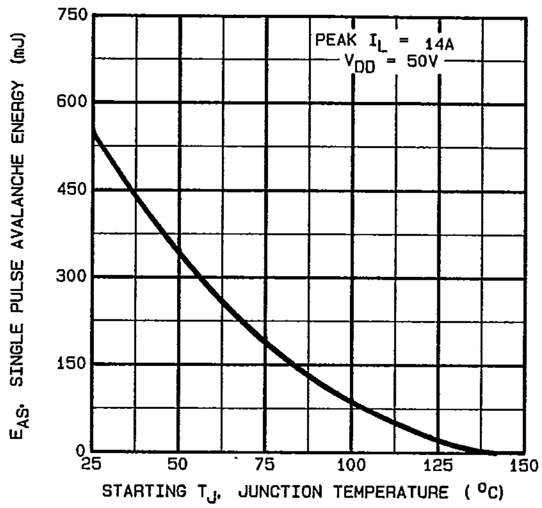

Fig. 14c — Maximum Avalanche Energy Vs. Starting Junction Temperature

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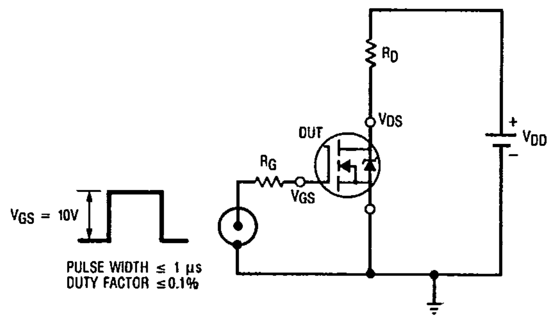

Fig. 15a — Switching Time Test Circuit

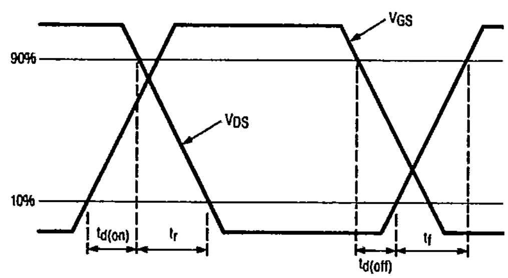

Fig. 15b — Switching Time Waveforms

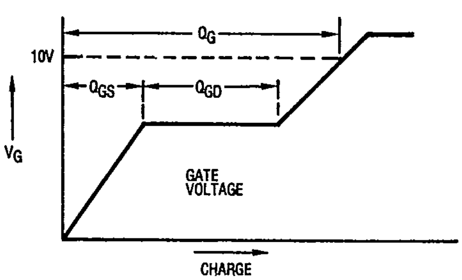

Fig. 16a — Basic Gate Charge Waveform

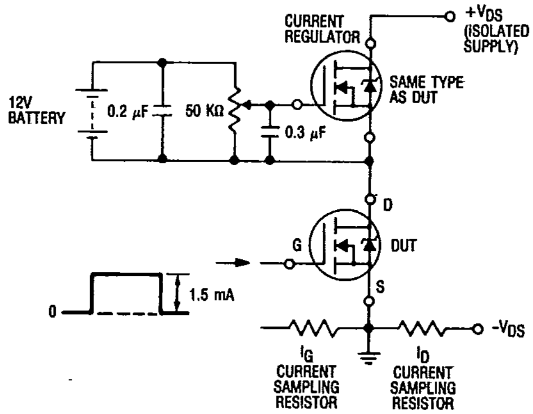

Fig. 16b — Gate Charge Test Circuit

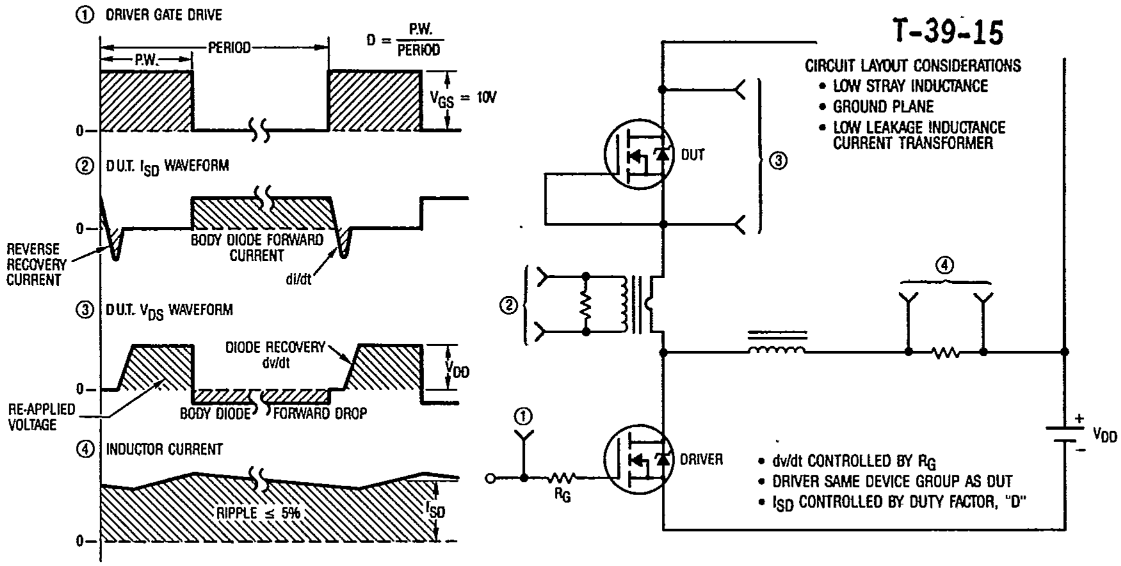

Fig. 17 — Peak Diode Recovery dv/dt Test Circuit

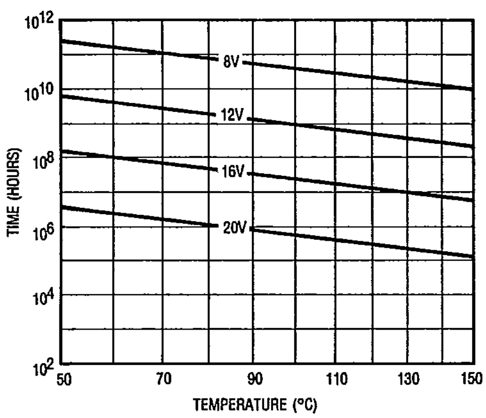

***Fig. 18 — Typical Time to Accumulated 1% Gate Failure**

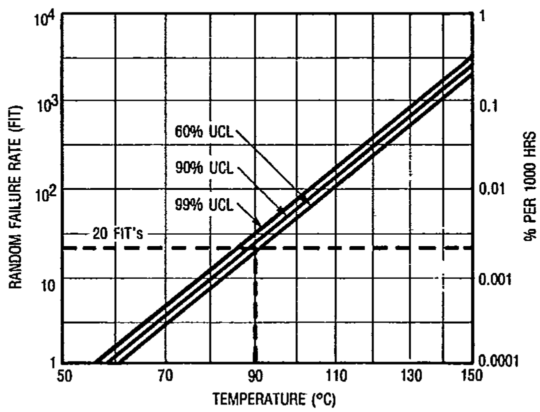

***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.