QLogic Corporation

ISP12160 Intelligent, Dual SCSI Processor

Data Sheet

Features

- 33-MHz, 64-bit PCI host bus interface (ISP12160/33), compliant with *PCI Local Bus Specification* rev 2.1
- Compliance with ANSI draft T10/1302D *SCSI-3 Parallel Interface* (SPI-3)
- Supports Ultra160/m SCSI
- SCSI feature set: dual transition, cyclical redundancy check (CRC), domain validation
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC98)
- Two concurrently operating wide, Ultra160/m SCSI channels
- Up to 160 Mbytes/sec parallel SCSI transfer rates per channel
- Supports single-ended, low voltage differential (LVD) SCSI
- SCSI initiator and target modes of operation
- Onboard RISC processor to execute operations at the I/O control-block level from the host memory
- Supports PCI dual-address cycle (64-bit addressing)
- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads
- JTAG boundary scan support

Product Description

The ISP12160 supports dual channel, Ultra160/m (Fast-80) SCSI functionality and is pin compatible with QLogic's ISP1280 Ultra2 SCSI processor. The product is a single-chip, highly integrated bus master, dual-channel SCSI I/O processor for SCSI initiator and target applications. This device interfaces the PCI bus to two Ultra160/m SCSI buses and contains an onboard RISC processor. The product is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP12160 provides power management feature support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP12160 is host-software compatible with the QLogic ISP1280 chip. The ISP12160 block diagram is illustrated in figure 1.

ISP Initiator and Target Firmware

The ISP12160 firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery, while the multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP12160 can switch between initiator and target modes.

Software Drivers

Software drivers are available for all major operating systems. ISP12160 BIOS firmware is also available.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP12160 incorporates a high-speed proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP12160 RISC interface requires external program and data memory.

The complete I/O subsystem solution including the ISP12160 and associated supporting memory devices is shown in figure 2.

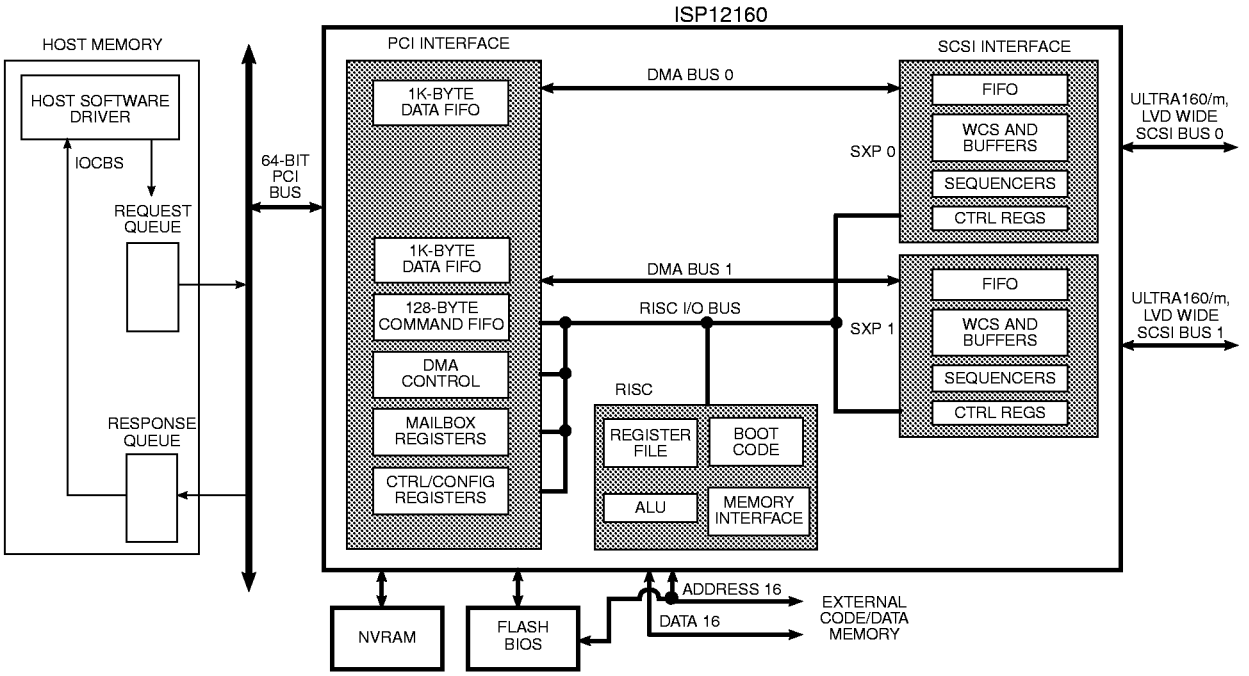

Figure 1. ISP12160 Block Diagram

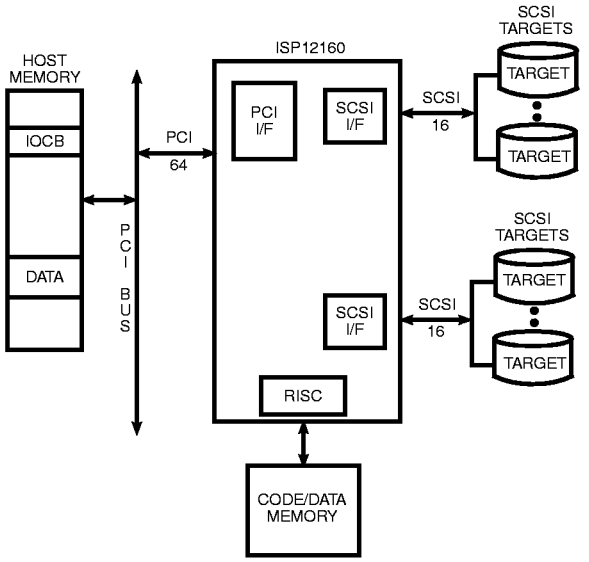

Figure 2. I/O Subsystem Design Using the ISP12160

Product Architecture

The following sections describe the ISP12160 modules.

PCI Interface

The ISP12160 PCI interface supports the following:

- 33-MHz, 64-bit, intelligent bus master interface
- 64-bit (address and data), intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers

- Supports PCI dual-address cycle (64-bit memory addressing)
- Backward compatible to 32-bit PCI
- Triple-channel DMA controller
- Two 1K-byte data DMA FIFOs and a 128-byte command DMA FIFO with threshold control
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter and gather operations
- 32-bit DMA transfer counter for I/O transfer lengths of up to four gigabytes
- Support for subsystem ID
- Support for flash BIOS PROM and serial NVRAM
- Support for PCI cache commands
- 3.3-V and 5.0-V tolerant PCI I/O buffers

The ISP12160 is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard DMA FIFO. It also allows the host to access the ISP12160 internal registers and communicate with the onboard RISC processor through the PCI target mode operation.

The ISP12160 supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP12160 supports power states D0, D3 hot, and D3 cold.

The ISP12160 onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The three DMA channels consist of one command DMA channel and two data DMA channels. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channels transfer data between the two SCSI buses and the PCI bus.

The PBIU internally arbitrates between the data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The ISP12160 SXP supports the following:

- Ultra (Fast-20), Ultra2 (Fast-40), and Ultra160/m (Fast-80) SCSI synchronous data transfer rates up to 160 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec
- Programmable SCSI processor
  - Specialized instruction set with 16-bit microword
  - 512 x 16 internal RAM control store
- 32-bit, configurable SCSI transfer counter
- Command, status, message in, and message out buffers
- Device information storage area
- On-chip, LVD SCSI transceivers
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

RISC Processor

The ISP12160 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The onboard RISC processor enables the ISP12160 to handle complete I/O transactions with no intervention from the host. The ISP12160 RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCB); and maintains the required thread information for each transfer.

Interfaces

The ISP12160 interfaces consist of the 64-bit PCI bus interface, two SCSI interfaces, RISC interface, BIOS PROM interface, and NVRAM interface. Pins that support these interfaces and other chip operations are shown in figure 3.

Packaging

The ISP12160 is available in a 492-pin plastic ballgrid array (PBGA) package.

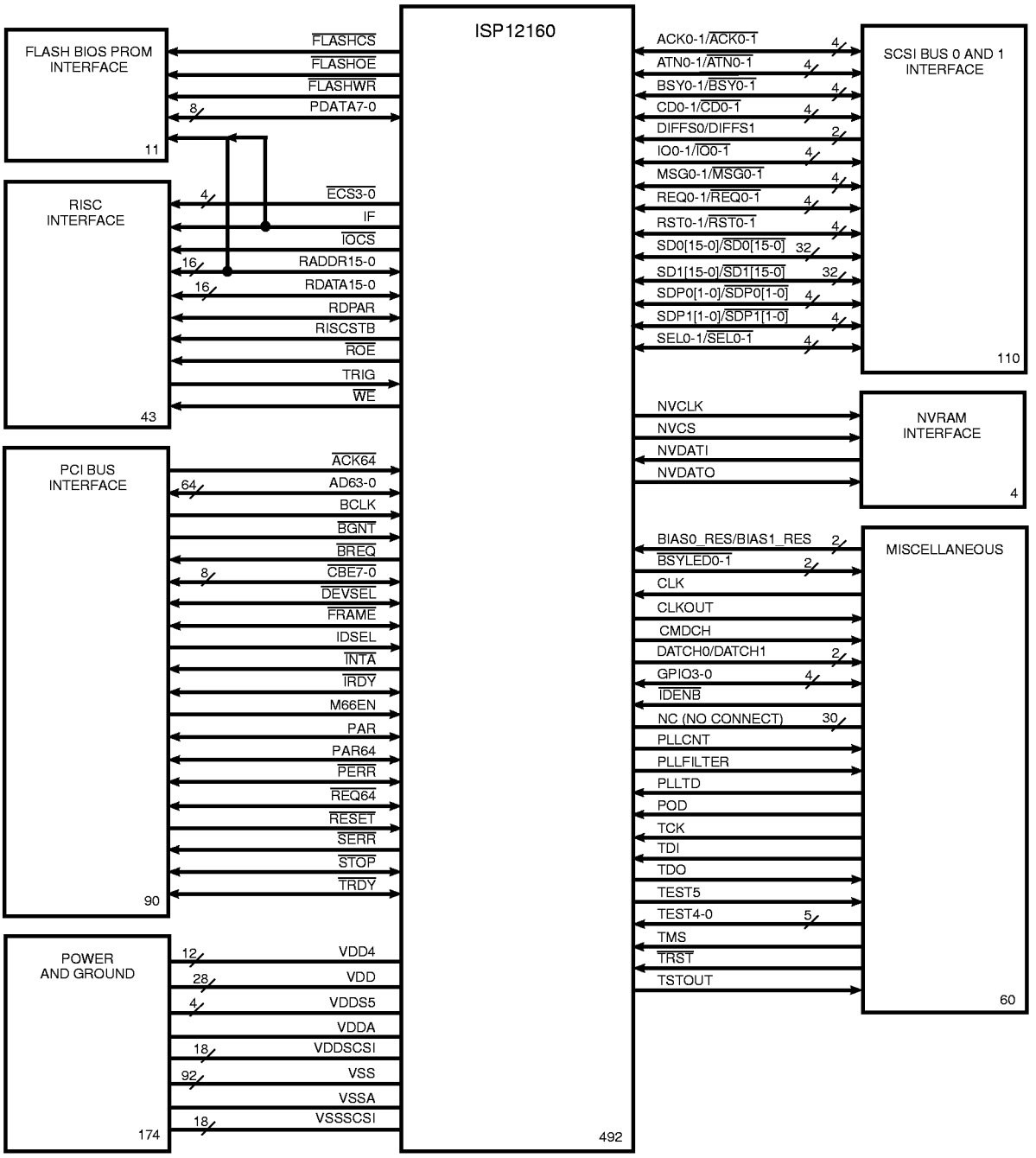

Figure 3. ISP12160 Functional Signal Grouping

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