82284
CLOCK GENERATOR AND READY INTERFACE FOR iAPX 286 PROCESSORS

(82284, 82284-6)

- **Generates System Clock for iAPX 286 Processors**
- **Uses Crystal or TTL Signal for Frequency Source**
- **Provides Local READY and Multibus* READY Synchronization**
- **18-pin Package**
- **Single +5V Power Supply**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The 82284 is a clock generator/driver which provides clock signals for iAPX 286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

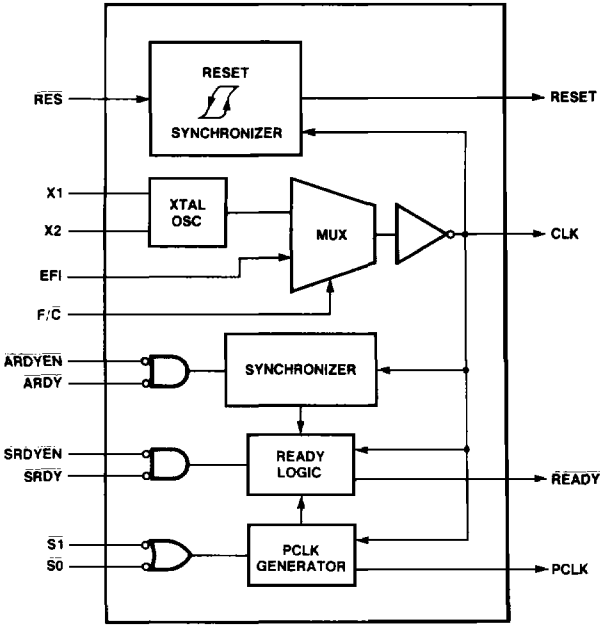

Figure 1. 82284 Block Diagram

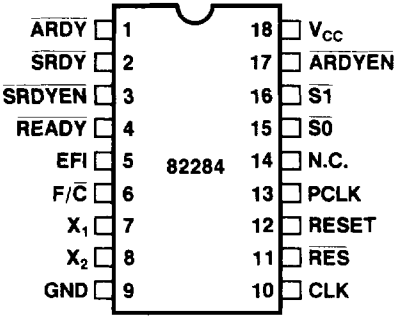

Figure 2. 82284 Pin Configuration

* Multibus is a patented bus of Intel

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Table 1. Pin Description

The following pin function descriptions are for the 82284 clock generator.

Symbol	Type	Name and Function
CLK	O	**System Clock** is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/$\overline{C}$	I	**Frequency/Crystal Select** is a strapping option to select the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	**Crystal In** are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	**External Frequency In** drives CLK when the F/$\overline{C}$ input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	**Peripheral Clock** is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PLCK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{ARDYEN}$	I	**Asynchronous Ready Enable** is an active LOW input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{ARDY}$	I	**Asynchronous Ready** is an active LOW input used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to $\overline{ARDY}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{SRDYEN}$	I	**Synchronous Ready Enable** is an active LOW input which qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{SRDY}$	I	**Synchronous Ready** is an active LOW input used to terminate the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{READY}$	O	**Ready** is an active LOW output which signals the current bus cycle is to be completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$ and $\overline{RES}$ inputs control $\overline{READY}$ as explained later in the $\overline{READY}$ generator section. $\overline{READY}$ is an open collector output requiring an external 300 ohm pullup resistor.
$\overline{S0}$, $\overline{S1}$	I	**Status** inputs prepare the 82284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	**Reset** is an active HIGH output which is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW).
$\overline{RES}$	I	**Reset In** is an active LOW input which generates the system reset signal RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{RES}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{CC}		**System Power**: +5V power supply
GND		**System Ground**: 0 volts

FUNCTIONAL DESCRIPTION

Introduction

The 82284 generates the clock, ready, and reset signals required for iAPX 286 processors and support components. The 82284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic and system reset generation logic.

Clock Generator

The CLK output provides the basic timing control for an iAPX 286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When

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F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the 82284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pines. Decouple V_{CC} and GND as close to the 82284 as possible.

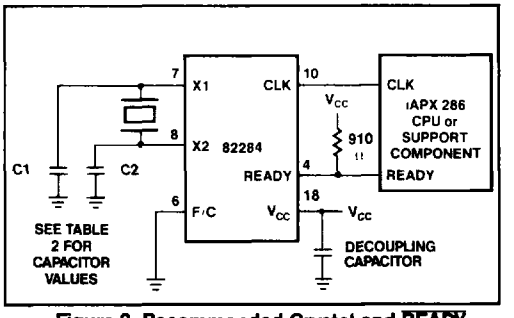

Figure 3. Recommended Crystal and $\overline{READY}$ Connections

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have have a stable V_{CC} and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. iAPX 286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 4, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

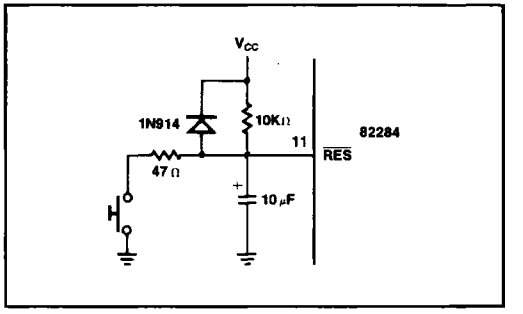

Figure 4. Typical RC $\overline{RES}$ Timing Circuit

A Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches between HIGH to LOW from the input voltage level at which the circuit output switches between LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$ LOW to HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the 82284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire or'ed with it, as shown in Figure 3. The $\overline{READY}$ signal of an iAPX 286 system requires an external 910 ohm ± 5% pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

Figure 5 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 6 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ have been resolved as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at end of T_S (see figure 6).

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, or the ready inputs are sampled as inactive.

Table 2. 82284 Crystal Loading Capacitance Values

Crystal Frequency	C1 Capacitance (pin 7)	C2 Capacitance (pin 8)
1 to 8 MHz	60 pF	40 pF
8 to 16 MHz	25 pF	15 pF

NOTE: Capacitance values must include stray board capacitance.

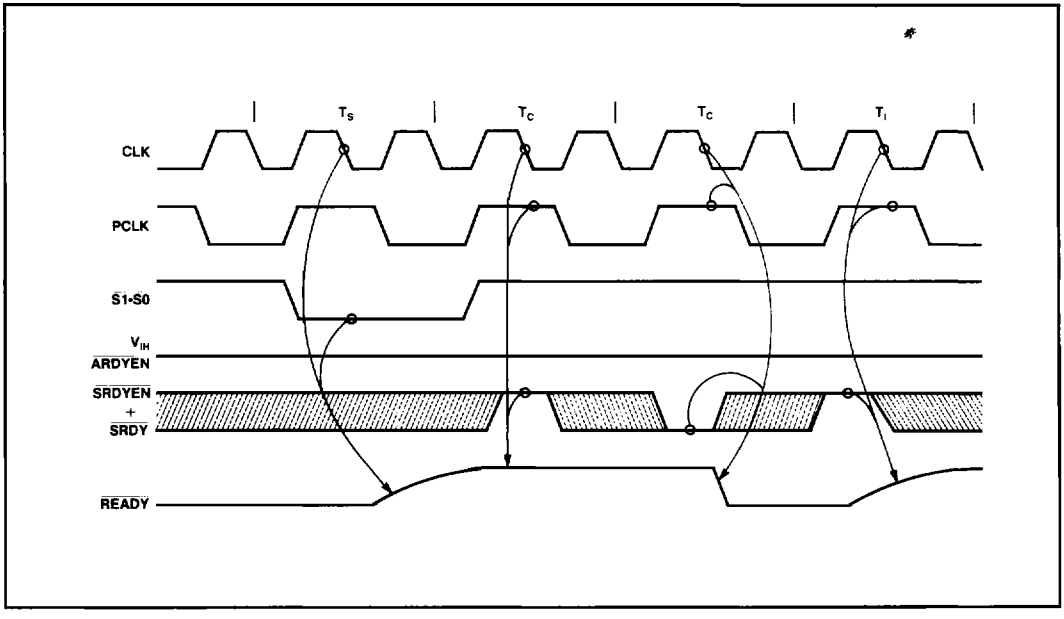

Figure 5. Synchronous Ready Operation

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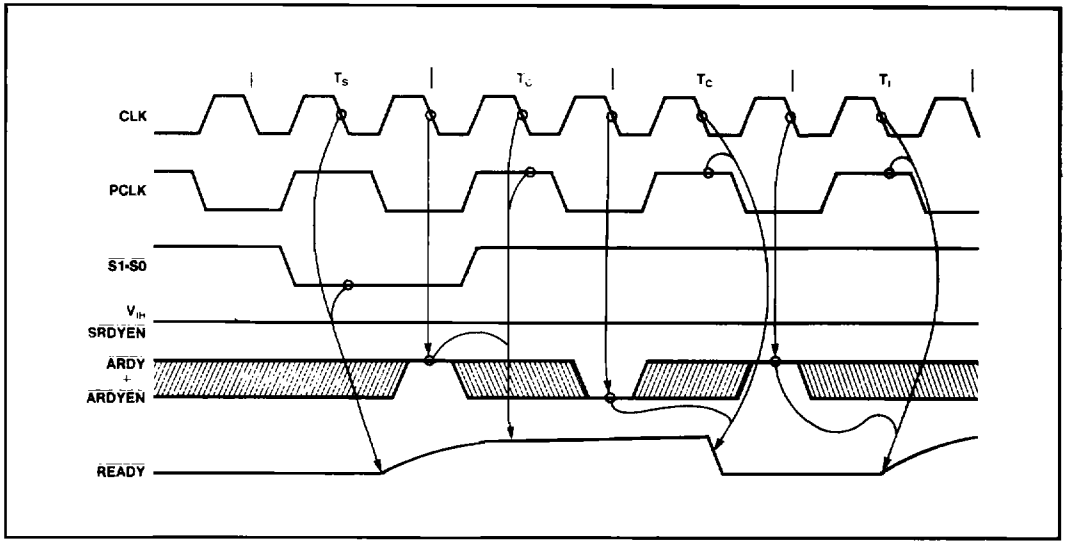

Figure 6. Asynchronous Ready Operation

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... -65°C to +150°C

All Output and Supply Voltages ..... -0.5V to +7V

All Input Voltages ..... -1.0V to +5 5V

Power Dissipation ..... 1 Watt

Notice: Stresses above those listed under "Absolute Maxmum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V, ± 10%)

		6 MHz		8 MHz			
Sym	Parameter	-6 Min	-6 Max	Min	Max	Unit	Test Condition
V_{IL}	Input LOW Voltage		.8		.8	V	
V_{IH}	Input HIGH Voltage	2.0		2.0		V	
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage	2.6		2.6		V	
V_{HYS}	$\overline{RES}$ Input hysteresis	0 25		0.25		V	
V_{OL}	RESET, PCLK Output LOW Voltage		.45		.45	V	I_{OL} = 5mA
V_{OH}	RESET, PCLK Output HIGH Voltage	2.4		2.4		V	I_{OH} = -1mA
V_{OLR}	$\overline{READY}$ Output LOW Voltage		.45		.45	V	I_{OL} = 7mA
V_{OLC}	CLK Output LOW Voltage		.45		.45	V	I_{OL} = 5mA
V_{OHC}	CLK Output HIGH Voltage	4 0		4.0		V	I_{OH} = -800μA
V_C	Input Forward Clamp Voltage		-1.0		-1.0	V	I_C = -5mA
I_F	Forward Input Current		-.5		-.5	mA	V_F = .45V
I_R	Reverse Input Current		50		50	uA	$V_R = V_{CC}$
I_{CC}	Power Supply Current		145		145	mA	
C_I	Input Capacitance		10		10	pF	F_C = 1MHz

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V, ± 10%)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

		6 MHz		8 MHz			
Sym	Parameter	-6 Min	-6 Max	Min	Max	Unit	Test Condition
1	EFI to CLK Delay		35		30	ns	at 1.5V Note 1
2	EFI LOW Time	35		32		ns	at 0.8V Note 1
3	EFI HIGH Time	35		28		ns	at 2.0V Note 1
4	CLK Period	83	500	62	500	ns	
5	CLK LOW Time	20		15		ns	at 0.6V Note 1 Note 2
6	CLK HIGH Time	25		20		ns	at 3.8V Note 1 Note 2
7	CLK Rise Time		10		10	ns	1.0V to 3.5V Note 1
8	CLK Fall Time		10		10	ns	3.5V to 1.0V Note 1
9	Status Setup Time	28		22.5		ns	Note 1
10	Status Hold Time	0		0		ns	Note 1
11	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	25		15		ns	Note 1
12	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	0		0		ns	Note 1
13	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	5		0		ns	Note 1 Note 3
14	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	30		16		ns	Note 1 Note 3
15	$\overline{RES}$ Setup Time	25		16		ns	Note 1 Note 3
16	$\overline{RES}$ Hold Time	10		0		ns	Note 1 Note 3
17	$\overline{READY}$ Inactive Delay	5		5		ns	at 0.8V Note 4
18	$\overline{READY}$ Active Delay	0	33	0	24	ns	at 0.8V Note 4
19	PCLK Delay	0	45	0	40	ns	Note 5
20	RESET Delay	0	50	0	40	ns	Note 5
21	PCLK LOW Time	t4-20.		t4-13.		ns	Note 5 Note 6
22	PCLK HIGH Time	t4-20.		t4-13.		ns	Note 5 Note 6

NOTE 1: CLK loading: C1 = 150pF.

NOTE 2: With the internal crystal oscillator using recommended crystal and capacitive loading, or with the EFI input meeting specifications t2, and t3. Use a parallel-resonant, fundamental mode crystal. The recommended crystal loading for CLK frequencies of 8-16MHz are 25pF from pin X_1 to ground, and 15pF from pin X_2 to ground. These recommended values are ± 5pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82284 as possible.

NOTE 3: This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

NOTE 4: $\overline{READY}$ loading: I_{OL} = 7mA, C_L = 150pF. In system application, use 910 ohm ±5% pullup resistor to meet 80286, 80286-6 and 80286-4 timing requirements.

NOTE 5: PCLK and RESET loading: C_L = 75pF.

NOTE 6: t4 refers to any allowable CLK period.

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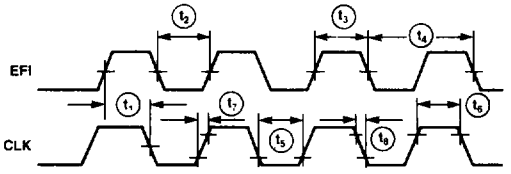
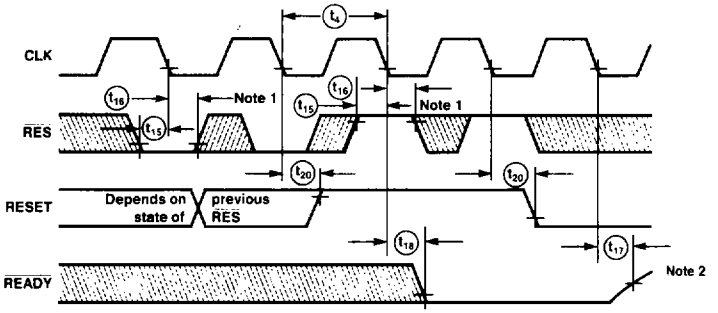
Waveforms

CLK as a Function of EFI



NOTE: The EFI input LOW and HIGH times as shown are required to guarentee the CLK LOW and HIGH times shown.

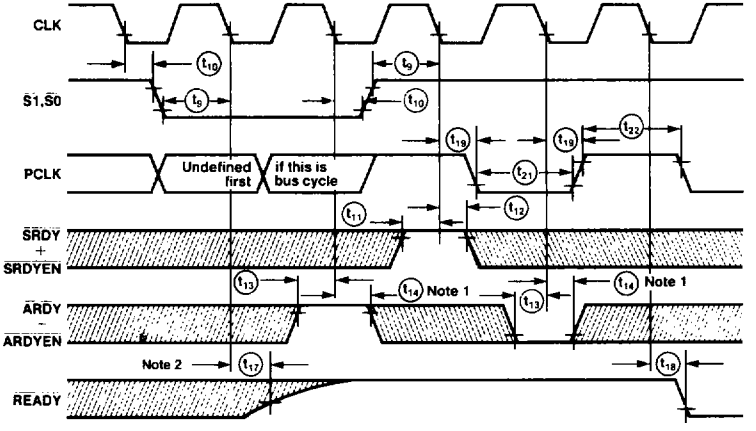
RESET and $\overline{\text{READY}}$ Timing as a Function of $\overline{\text{RES}}$ with $\overline{\text{S1}}$ and $\overline{\text{S0}}$ HIGH



NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

NOTE 2: Tie 910 ohm ±5% pullup resistor to the $\overline{\text{READY}}$ output

$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ HIGH



NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

NOTE 2: Tie 910 ohm ±5% pullup resistor to the $\overline{\text{READY}}$ output.

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