MCM6294

16K x 4 Bit Synchronous Static RAM
with Output Registers and Output Enable

The MCM6294 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MCM6294 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

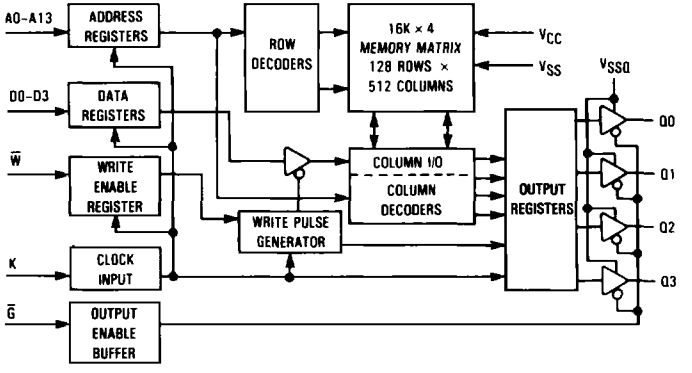
The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6294 is available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

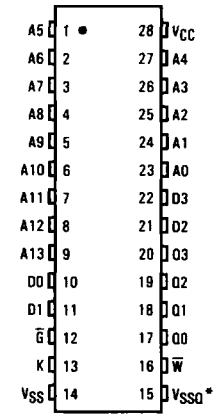
BLOCK DIAGRAM



P PACKAGE
300 MIL PLASTIC
CASE 710A

J PACKAGE
PLASTIC
CASE 810

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

PIN NAMES	
A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

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TRUTH TABLE

$\overline{W}$	Operation	Q0-Q3
L	Write	High Z
H	Read	D_{out}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, I_{out} = 0 mA, Cycle Time = t_{KHKH} min)	I_{CCA}	–	140	mA
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6294-20		MCM6294-25		MCM6294-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	5
Setup Times for: $\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	5
Hold Times for: $\overline{W}$	t_{KHWX}								
$\overline{G}$ High to Q High Z	t_{GHQZ}	–	10	–	10	–	13	ns	4, 6
$\overline{G}$ Low to Q Active	t_{GLQX}	0	–	0	–	0	–	ns	4, 6
$\overline{G}$ Low to Q Valid	t_{GLQV}	–	10	–	10	–	13	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device.

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AC TEST LOADS

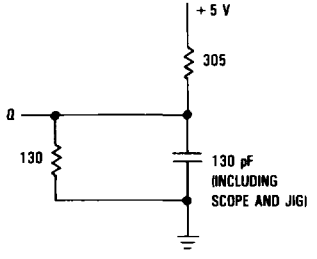


Figure 1A

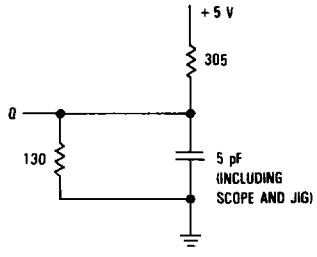
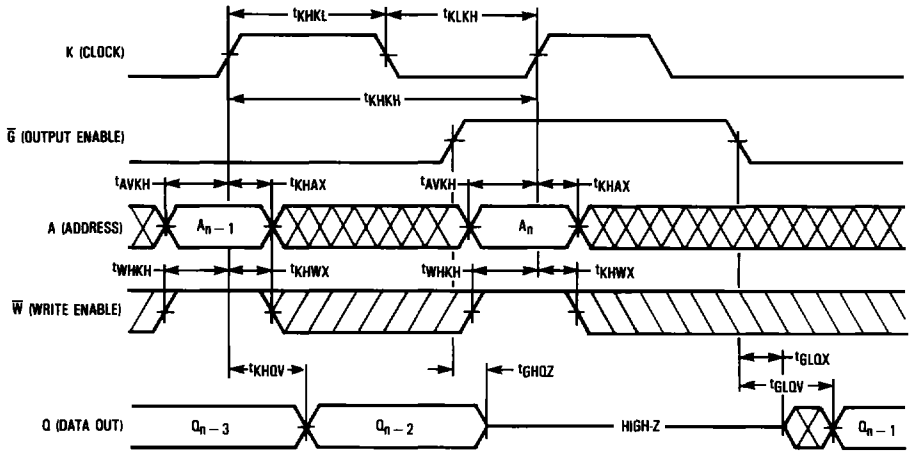
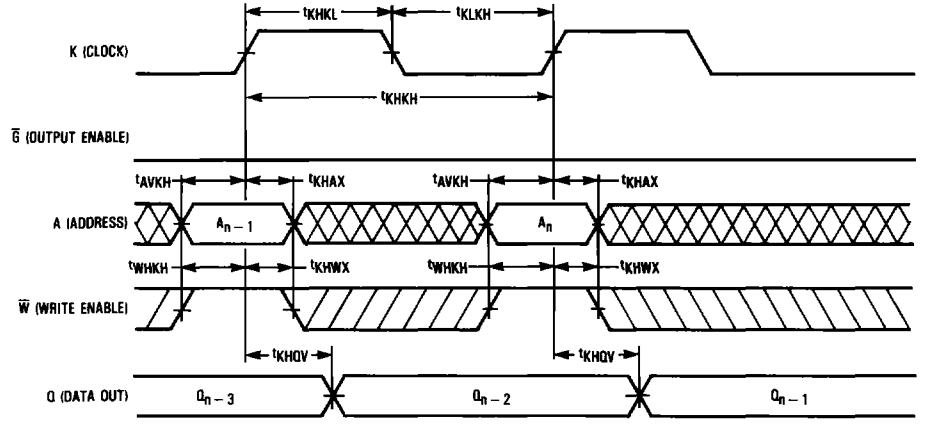


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



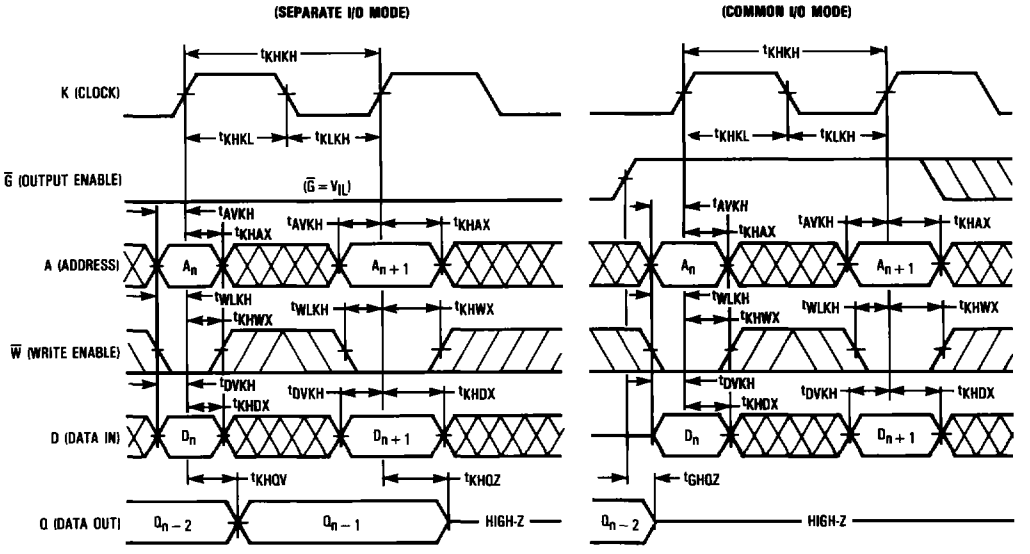
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles, where $\overline{W} = V_{IH}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6294-20		MCM6294-25		MCM6294-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	30	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	–	13	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	10	–	13	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	5
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	5
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6294 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 2 shows a typical system configuration using four MCM6294 chips. The system addresses are tied to the MCM6294s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6294. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

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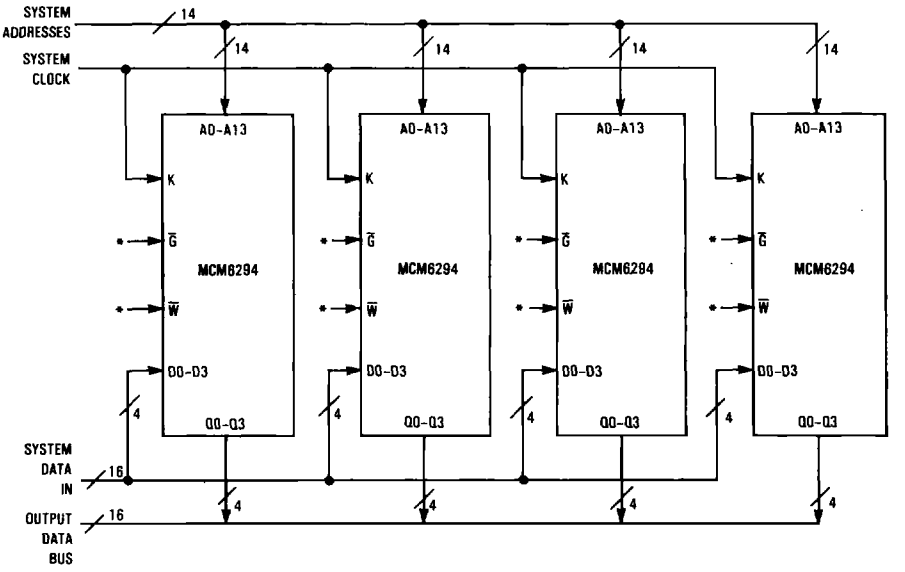
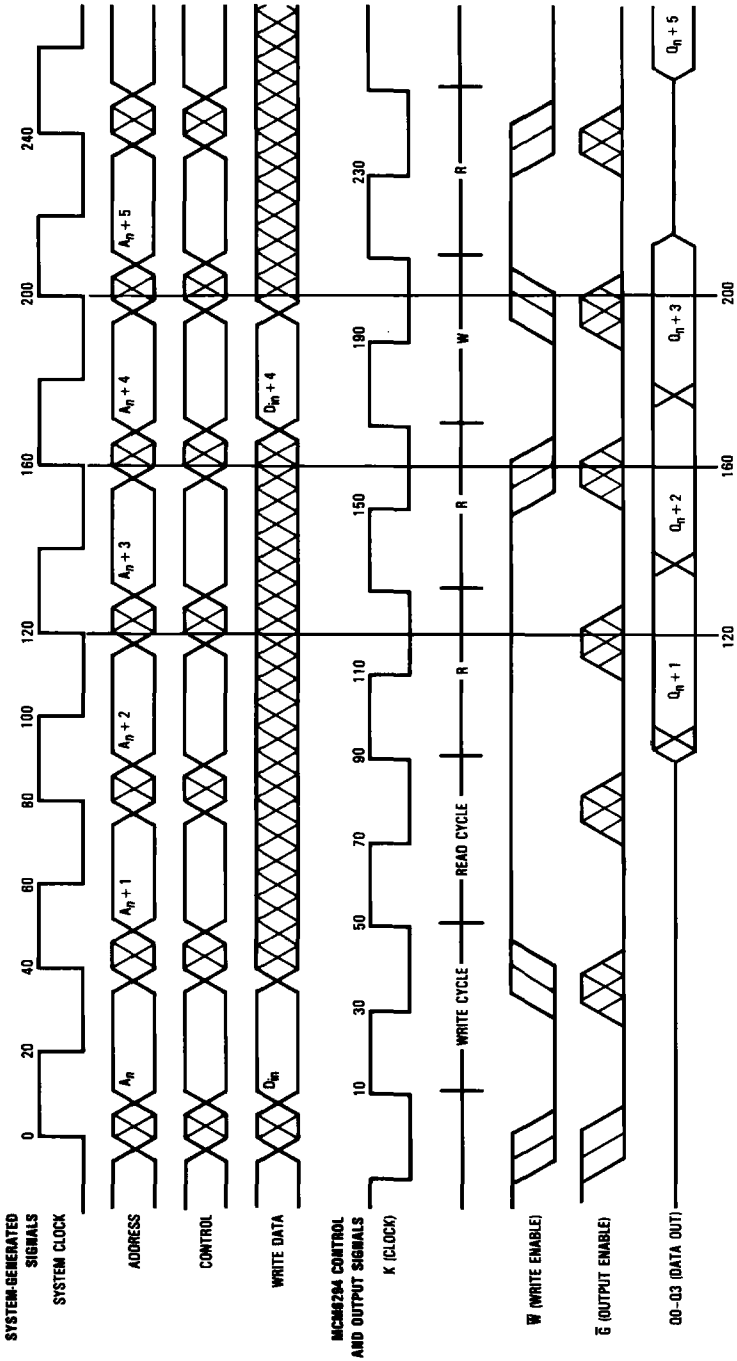


Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Pipeline System Timing

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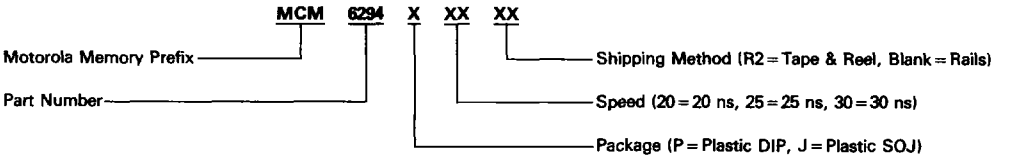
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6294P20	MCM6294J20	MCM6294J20R2
	MCM6294P25	MCM6294J25	MCM6294J25R2
	MCM6294P30	MCM6294J30	MCM6294J30R2

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