

**STD60NF06****N-CHANNEL 60V - 0.014Ω - 60A DPAK
STripFET™ II POWER MOSFET**

TYPE	V _{DSS}	R _{D(on)}	I _D
STD60NF06	60 V	< 0.016 Ω	60A

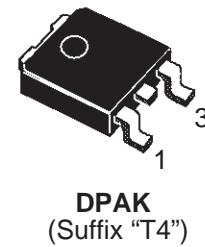
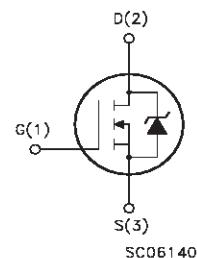
- TYPICAL R_{D(on)} = 0.014Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This Power Mosfet series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL
- AUTOMOTIVE

DPAK
(Suffix "T4")**INTERNAL SCHEMATIC DIAGRAM**

SC06140

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	60	A
I _D	Drain Current (continuous) at T _C = 100°C	42	A
I _{DM (1)}	Drain Current (pulsed)	240	A
P _{TOT}	Total Dissipation at T _C = 25°C	110	W
	Derating Factor	0.73	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	4	V/ns
T _{stg}	Storage Temperature	– 55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 60A, di/dt ≤ 200 A/μs, V_{DD} ≤ 24V, T_j ≤ T_{jMAX}

STD60NF06

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T _j	Maximum Lead Temperature For Soldering Purpose		275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	30	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 30 V)	350	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	60			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DSON}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 30 A		0.014	0.016	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 30 A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		1810		pF
C _{oss}	Output Capacitance			360		pF
C _{rss}	Reverse Transfer Capacitance			125		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30 \text{ V}$, $I_D = 30 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (see test circuit, Figure 3)		16		ns
t_r	Rise Time			108		ns
Q_g	Total Gate Charge	$V_{DD} = 48 \text{ V}$, $I_D = 60 \text{ A}$ $V_{GS} = 10 \text{ V}$		49	66	nC
Q_{gs}	Gate-Source Charge			18		nC
Q_{gd}	Gate-Drain Charge			14		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 30 \text{ V}$, $I_D = 30 \text{ A}$,		43		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (see test circuit, Figure 3)		20		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 48 \text{ V}$, $I_D = 60 \text{ A}$		40		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$		12		ns
t_c	Cross-over Time	(see test circuit, Figure 3)		21		ns

SOURCE DRAIN DIODE

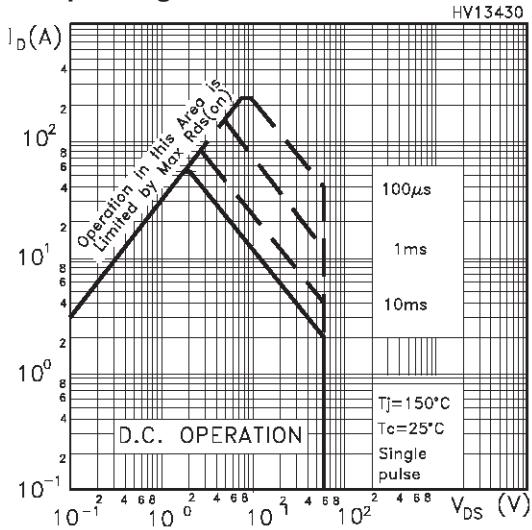
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				60	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				240	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 60 \text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 60 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,		73		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 25 \text{ V}$, $T_j = 150^\circ\text{C}$		182		nC
I_{IRRM}	Reverse Recovery Current	(see test circuit, Figure 5)		5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

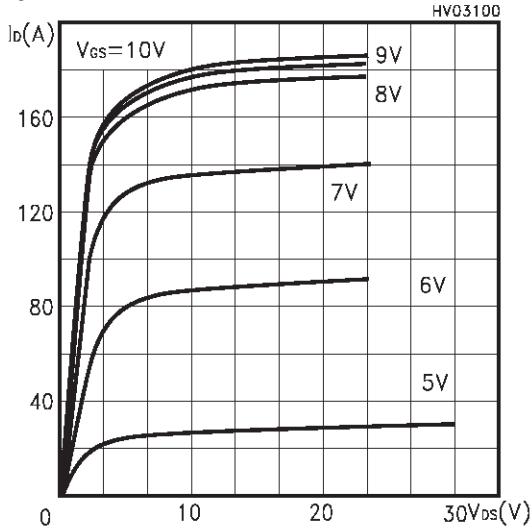
2. Pulse width limited by safe operating area.

STD60NF06

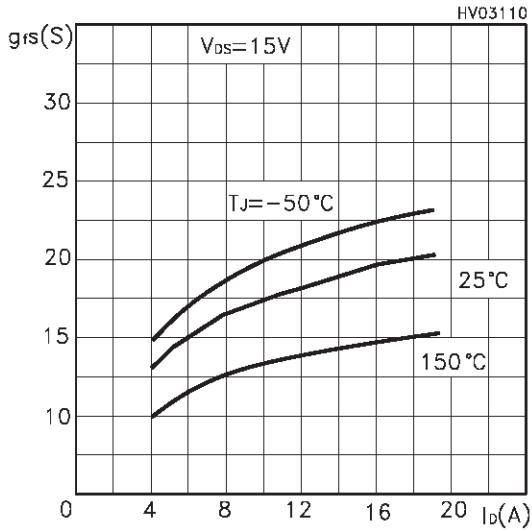
Safe Operating Area for DPAK



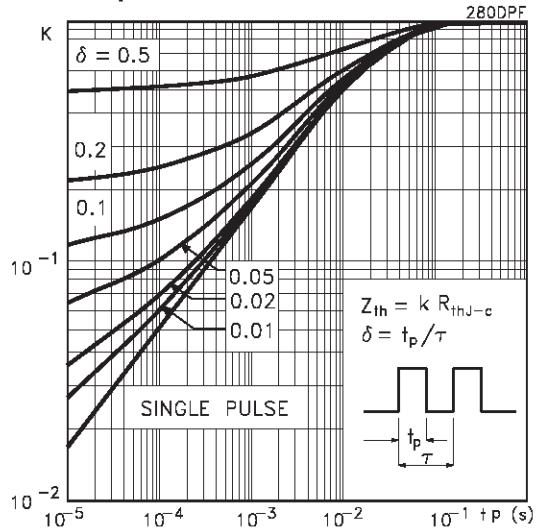
Output Characteristics



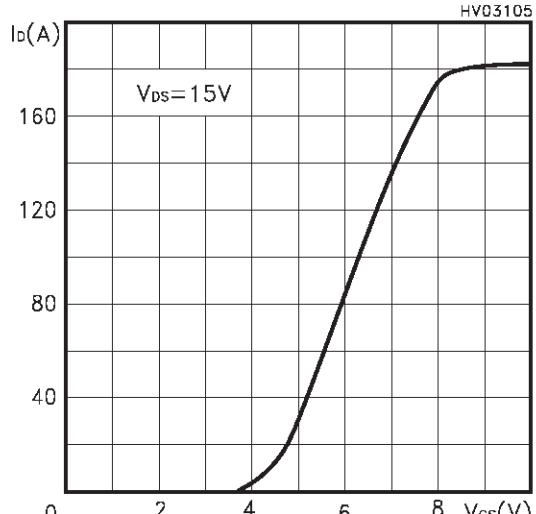
Transconductance



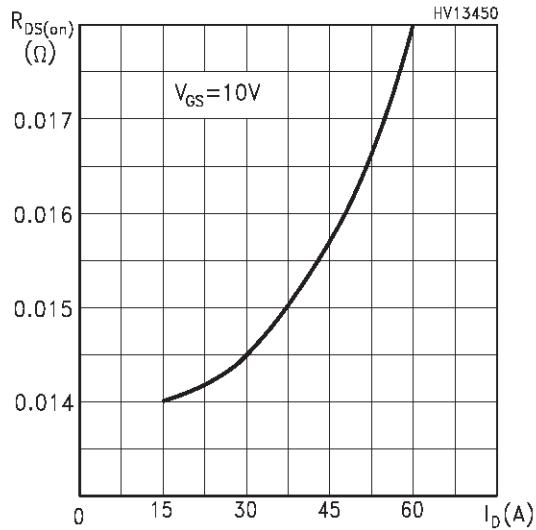
Thermal Impedance for DPAK

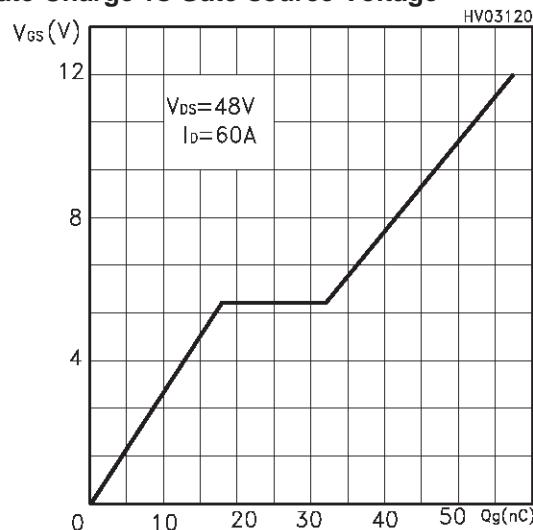
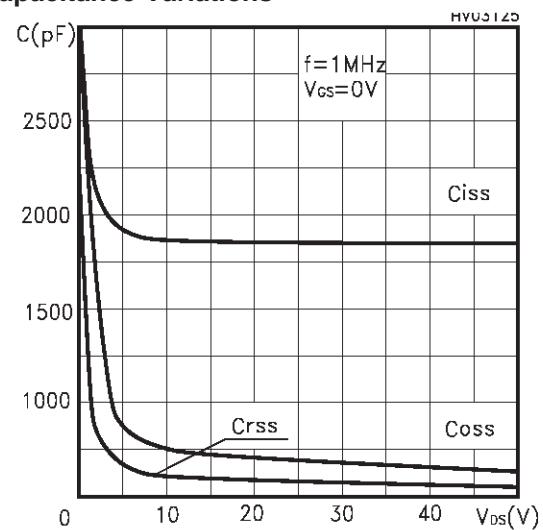
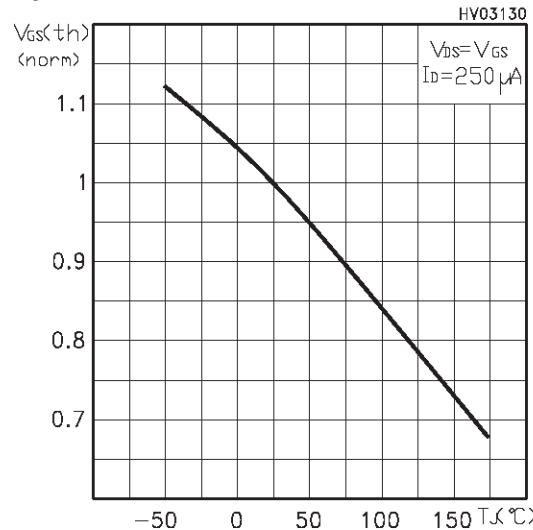
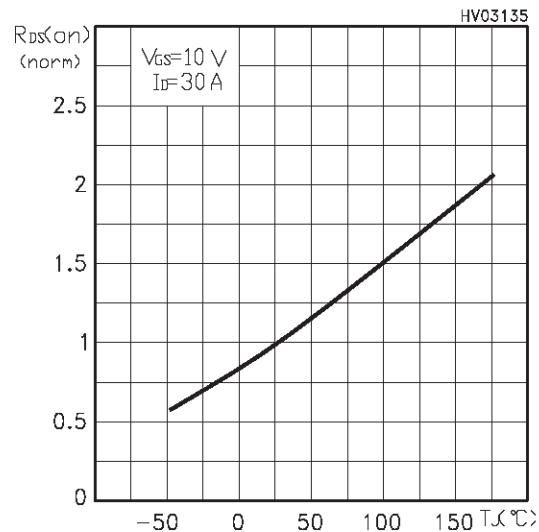
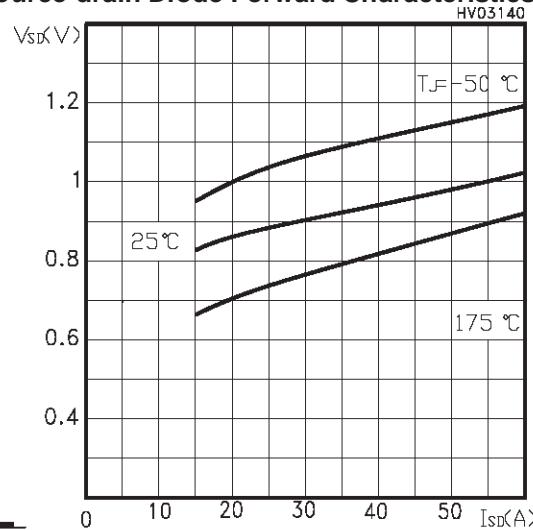


Transfer Characteristics



Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage**Capacitance Variations****Normalized Gate Threshold Voltage vs Temperature****Normalized On Resistance vs Temperature****Source-drain Diode Forward Characteristics**

STD60NF06

Fig. 1: Unclamped Inductive Load Test Circuit

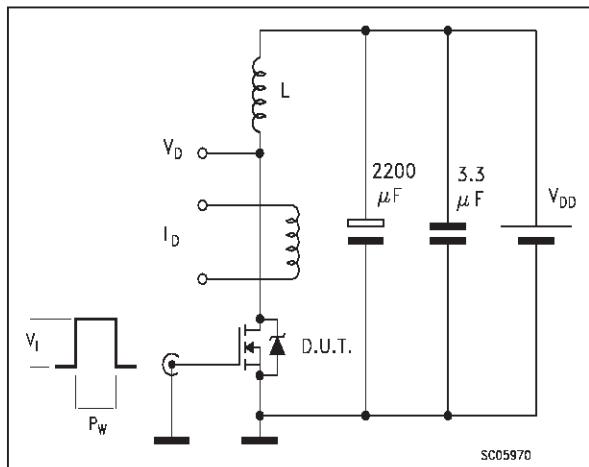


Fig. 2: Unclamped Inductive Waveform

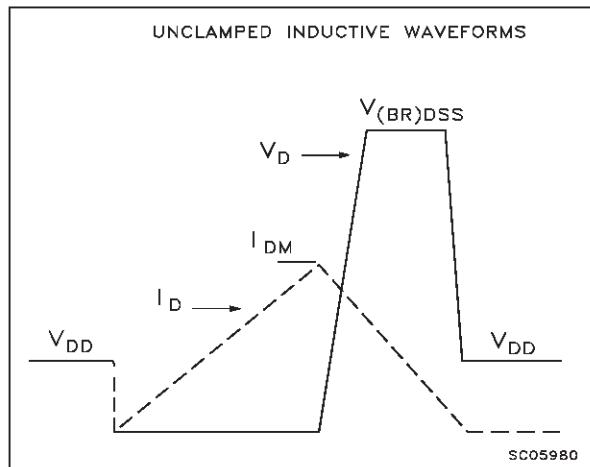


Fig. 3: Switching Times Test Circuit For Resistive Load

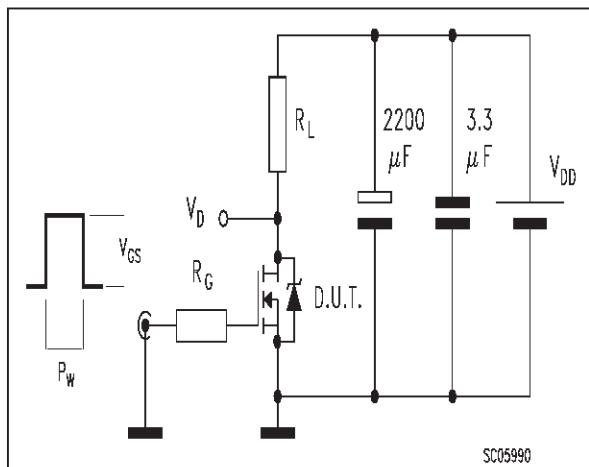


Fig. 4: Gate Charge test Circuit

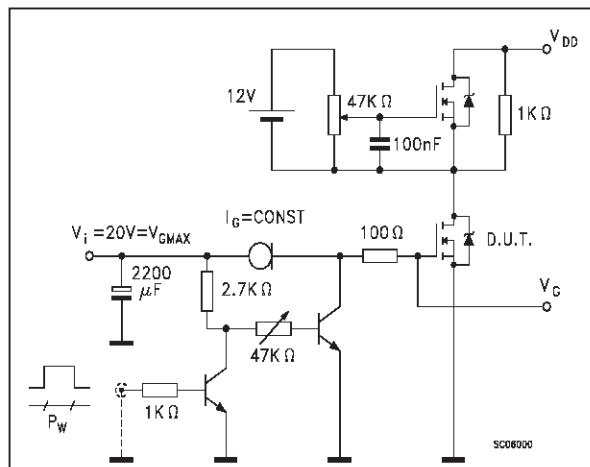
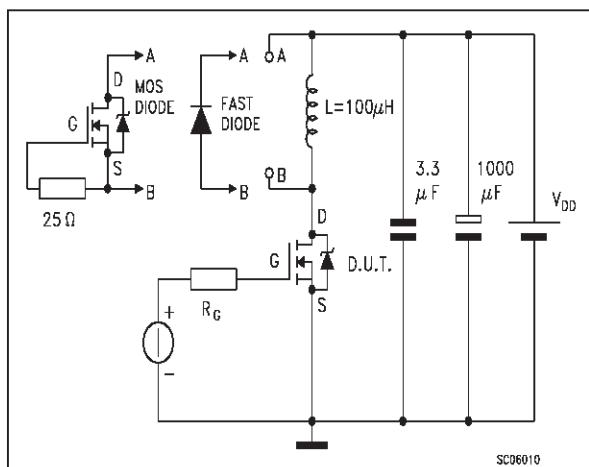
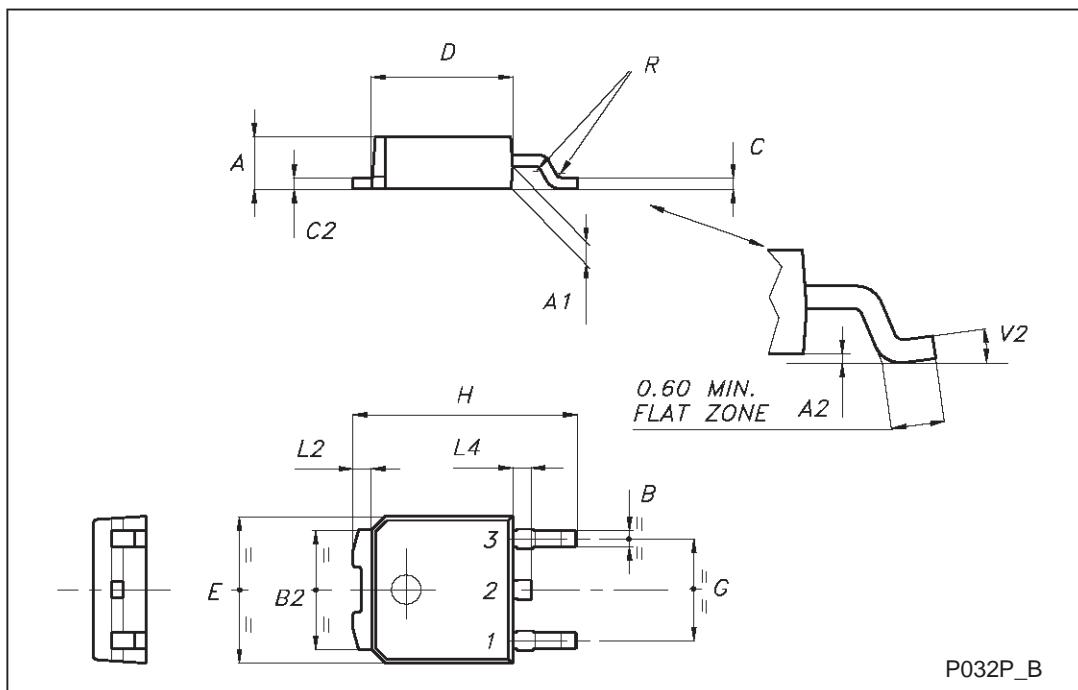


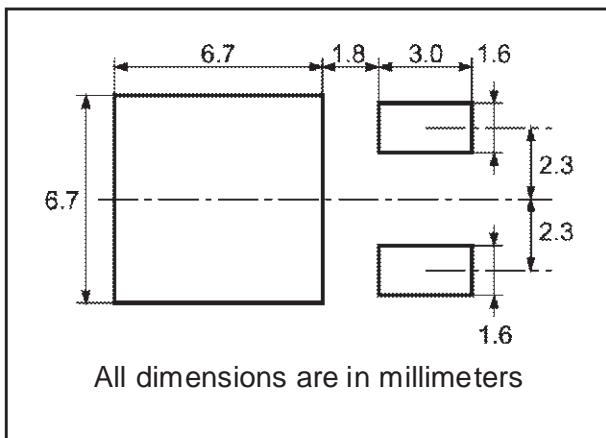
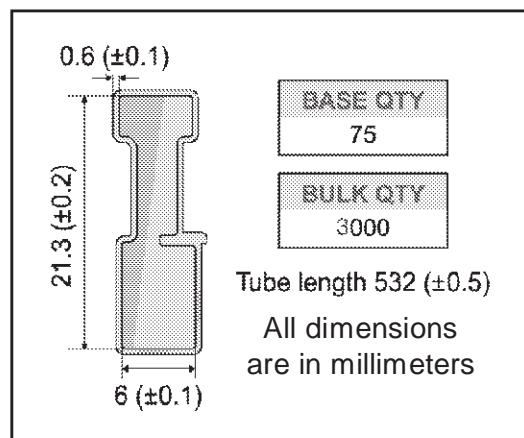
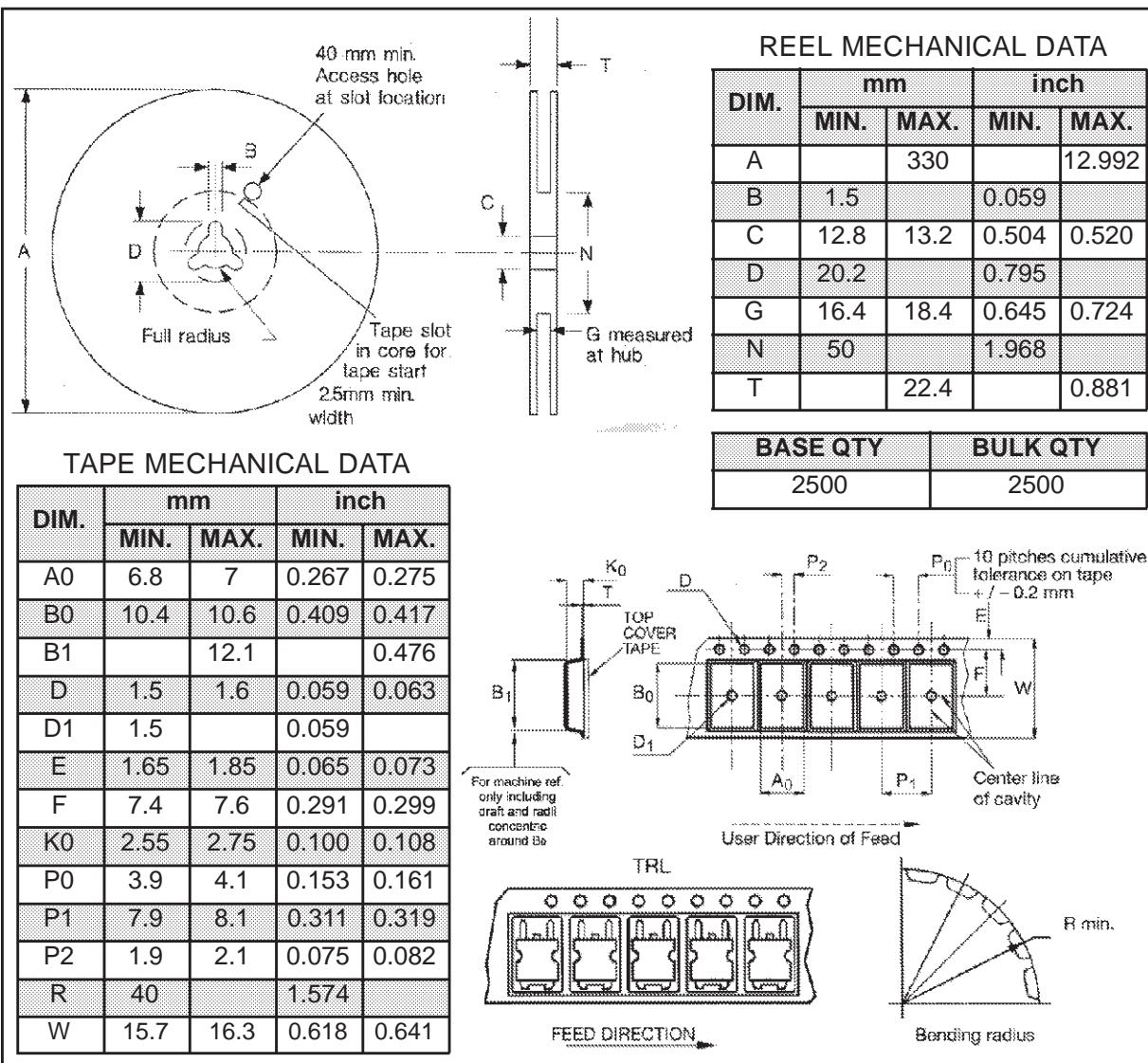
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



DPAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>