

1.1 Scope.

This specification covers the detail requirements for a complete monolithic 12-bit, 10 Msps A/D converter with an on-chip, high performance track-and-hold amplifier (THA) and voltage reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD872SD/883B
-2	AD872SE/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Side Brazed Ceramic DIP
E	E-44A	44-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

AV_{DD} to AGND	-0.5 V to +6.5 V
AV_{SS} to AGND	-6.5 V to +0.5 V
DV_{DD} , DRV_{DD} to DGND	-0.5 V to +6.5 V
AGND to DGND	-1 V to +1 V
AV_{DD} to DV_{DD}	-6.5 V to +6.5 V
Clock Input, OEN to DGND	-0.5 V to $DV_{DD} + 0.5$ V
Digital Outputs to DGND	-0.5 V to $DV_{DD} + 0.3$ V
REF IN to AV_{DD}	AV_{SS} to 0 V
REF IN to AV_{SS}	0 V to AV_{DD}
V_{INA} , V_{INB} , REF IN to AGND	-6.5 V to +6.5 V
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10 sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance: $\theta_{JC} = 25^\circ\text{C}/\text{W}$ for D-28
 $\theta_{JA} = 60^\circ\text{C}/\text{W}$ for D-28
 $\theta_{JC} = 42^\circ\text{C}/\text{W}$ for E-44A
 $\theta_{JA} = 70^\circ\text{C}/\text{W}$ for E-44A

AD872—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition	Units
Resolution	RES	-1	12	12	12		Bits
Differential Nonlinearity ¹	DNL	-1	12	12	12	All Codes Histogram	Bits
Zero Error	B _{POE}	-1	0.75	0.75			±% FSR max
Gain Error	A _E	-1	1.25	1.25			±% FSR max
Zero Error Drift	TCB _{POE}	-1			0.30	External 2.5 V Reference	±% FSR max
Gain Error Drift	TCA _{INT}	-1			1.75	Internal 2.5 V Reference	±% FSR max
Gain Error Drift	TCA _{EXT}	-1			0.5	External 2.5 V Reference	±% FSR max
Power Supply Rejection	PSR	-1	0.125	0.125	0.125	See Note 2	±% FSR max
Analog Input Range	V _{IN}	-1	1	1	1		±V max
Input Resistance	R _{IN}	-1	50				kΩ
Input Capacitance	C _{IN}	-1	10				pF
Internal Reference Output Voltage	V _{REF}	-1	2.46	2.46	2.46		V min
			2.54	2.54	2.54		V max
Power Dissipation	PD	-1	1.3	1.3	1.3		Watts max
Power Supply Current	I _{AVDD}	-1	88	88	88		mA max
	I _{AVSS}		150	150	150		
	I _{DVDD}		21	21	21		
	I _{DRVDD} ³		2	2	2		
Signal-to-Noise Distortion Ratio	S/(N+D)	-1	61	61	61	f _{IN} = 1 MHz; f _S = 10 MHz	dB min
		-2	60	60	60		
Total Harmonic Distortion	THD	-1	-62	-62	-62	f _{IN} = 1 MHz; f _S = 10 MHz	dB max
		-2	-60	-60	-60		
Logic Input High Voltage	V _{IH}	-1	2.0	2.0	2.0		V min
Logic Input Low Voltage	V _{IL}	-1	0.8	0.8	0.8		V max
Logic Input High Current (CLK, OEN ³)	I _{IH}	-1	10	10	10		±μA max
Logic Input Low Current (CLK, OEN ³)	I _{IL}	-1	10	10	10		±μA max
Logic Output High Voltage (MSB-Bit 12, OTR)	V _{OH}	-1	2.4	2.4	2.4	I _{SOURCE} = 500 μA	V min
Logic Output Low Voltage (MSB-Bit 12, OTR)	V _{OL}	-1	0.4	0.4	0.4	I _{SINK} = 1.6 mA	V min
Leakage ³	I _Z	-1	10	10	10	Three-State	±μA max
Clock Period	t _C	-1	100	100	100		ns min
Output Delay	t _{OD}	-1	10	10	10		ns min
Pipeline Delay	t _{PD}	-1	3				Clock Cycles max
Clock Pulse Width High	t _{CH}	-1	45				ns min
Clock Pulse Width Low	t _{CL}	-1	45				ns min
Clock Duty Cycle	D _{CYC}	-1	40				% min
			60				% max

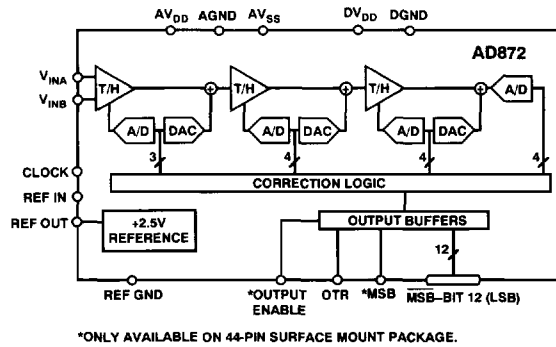
NOTES

¹Minimum resolution for which "no missing codes" is guaranteed.

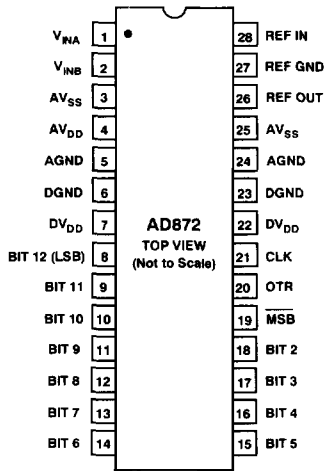
²Test conditions for PSR: 4.75 V ≤ AV_{DD} ≤ 5.25 V, -5.25 V ≤ AV_{SS} ≤ -4.75 V, 4.75 V ≤ DV_{DD} ≤ 5.25 V.

³E-44A package only.

3.2.1 Functional Block Diagram and Terminal Assignments.



D Package



E Package

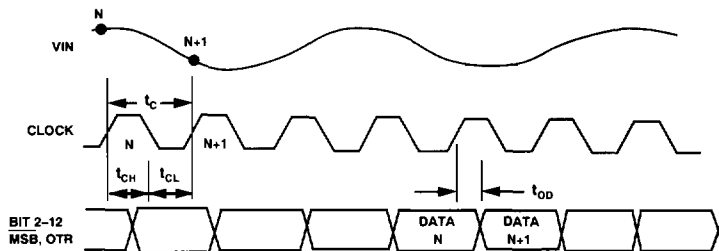
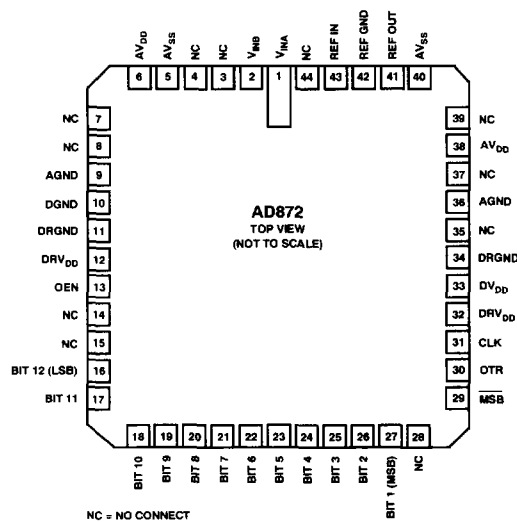


Figure 1. Timing Diagram

