Register Programmable Clock Generator

AK8141

Features

- **Input Frequency:**
  48MHz/24MHz/12MHz/27MHz (Selectable)
- **Output Frequency:**
  27MHz – 50MHz by 1MHz step,
  33.75MHz/40.5MHz/49.5MHz (Selectable)
- **Low Jitter Performance:**
  15 ps (Typ.) Period 1σ
- **Low Current Consumption:**
  3.5mA (Typ.) at 27MHz, 3.0V
  4.5mA (Typ.) at 50MHz, 3.0V
- **Output Load:**
  15pF(Max)
- **Supply Voltage:**
  2.7 – 3.6V
- **Operating Temperature Range:**
  -20 to +85℃
- **Package:**
  8-pin USON

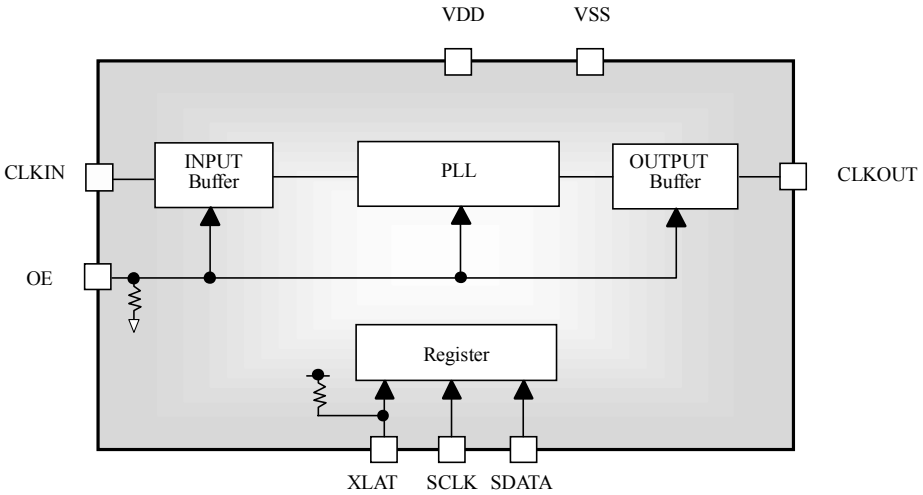
Description

The AK8141 is a single clock generator IC with an integrated PLL. It can generate a 27.0MHz – 50.0MHz by 1MHz step or 33.75MHz, 40.5MHz, 49.5MHz clock from a 48MHz, 24MHz, 12MHz and 27MHz master clock input frequency. The output can be enabled or disabled with pin and the frequency can be changed via three-line serial interface. The high performance PLL locks to the master clock input, generating a low jitter, highly accurate clock output without an external crystal.

Applications

- Digital Still Camera
- Digital Video Camera

Block Diagram



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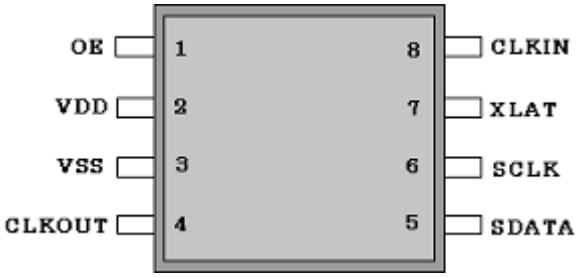
PIN DESCRIPTION



Package: 8-Pin USON (Top View)

Pin No.	Pin Name	Pin Type	Description	
1	OE	IN	CLKOUT output enable control "L": CLKOUT="L" and power down. "H": active	(1)
2	VDD	--	Power supply	
3	VSS	--	Ground	
4	CLKOUT	OUT	Clock output Output clock frequency is selectable to 27.0MHz or 50.0MHz by 1MHz step, or 33.75MHz, 40.5MHz, 49.5MHz through the three-line serial interface. In power down mode (OE = "L"), this pin is "L".	
5	SDATA	IN	Serial data input	
6	SCLK	IN	Serial clock input	
7	XLAT	IN	Serial write control 8-bits serial data is stored at the rising edge of this input. Set "H" except during serial write process	(1)
8	CLKIN	IN	Clock input Input frequency is selected from 48MHz, 24MHz, 12MHz or 27MHz via the serial interface. Place the AK8141 in power down (OE = "L") mode when an input clock is not supplied. Unstable input to the CLKIN causes the unstable CLKOUT signal. DC input to the CLKIN also causes the unstable CLKOUT signal.	

(1) Internal pull down 100kΩ (Typ.)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8141U	8141	Tape and Reel	8-pin USON	-20 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	Vin	VSS-0.3 to VDD+0.3	V
Input Current (any pins except supplies)	I_{IN}	±10	mA
Storage Temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature	Ta		-20		85	°C
Supply Voltage	VDD		2.7	3.0	3.6	V
Input Clock Frequency	Fin			48.0 24.0 12.0 27.0		MHz
Input Clock Duty Cycle				50		%
Output Load Capacitance	Cp1	Pin: CLKOUT			15	pF

DC Characteristics

All specifications at VDD: over 2.7 to 3.6V, Ta: -20 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}	Pin: CLKIN, OE, XLAT, SCLK, SDATA	0.7*VDD			V
Low level input voltage	V_{IL}	Same as above			0.3*VDD	V
Input leakage current 1	I_L1	Pin: CLKIN, SCLK, SDATA	-10		+10	μA
Input leakage current 2	I_L2	OE	-10		+75	μA
Input leakage current 3	I_L3	XLAT	-75		+10	μA
High level output voltage	V_{OH}	CLKOUT IOH= -4mA (VDD=3.0V, Ta=25°C)	0.8*VDD			V
Low level output voltage	V_{OL}	CLKOUT IOL = +4mA (VDD=3.0V, Ta=25°C)			0.2*VDD	V
Current Consumption1	$I_{DD}1$	No load CLKIN=48MHz CLKOUT=27MHz (VDD=3.0V, Ta=25℃)		3.5		mA
Current Consumption2	$I_{DD}2$	No load CLKIN=48MHz CLKOUT=50MHz (VDD=3.0V, Ta=25℃)		4.5		mA
Power down current	I_{pd}	OE="L" FSEL="L" or open		0	10	μA

AC Characteristics

All specifications at VDD: over 2.7 to 3.6V, Ta: -20 to +85℃, unless otherwise noted

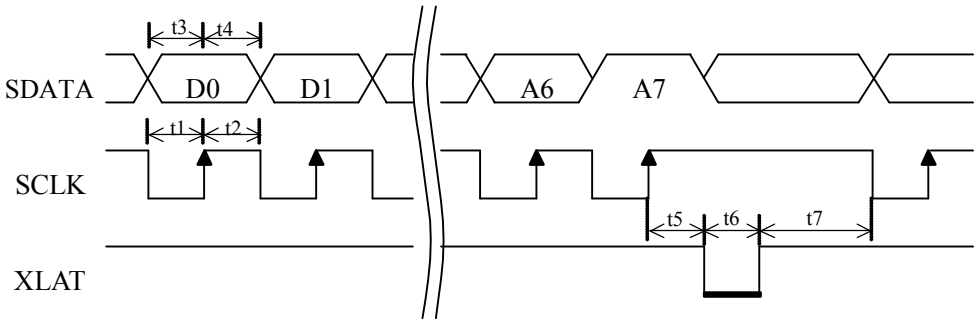
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Duty Cycle(2) (3)			45	50	55	%
Output Clock Rise Time(2) (3)	t_{rise}	0.2VDD to 0.8VDD			4.0	ns
Output Clock Fall Time(2) (3)	t_{fall}	0.2VDD to 0.8VDD			4.0	ns
Output Clock Jitter (2) (3)	Jit	Period, 1σ		15		ps
Output Lock Time(1)	t_{lock}	Power-up			1	ms

(1) The time that output reaches the target frequency within accuracy of ±0.1% from the point that the power supply reaches VDD

(2) With the load capacitance specified by the recommended operation conditions

(3) Design value

Serial Interface

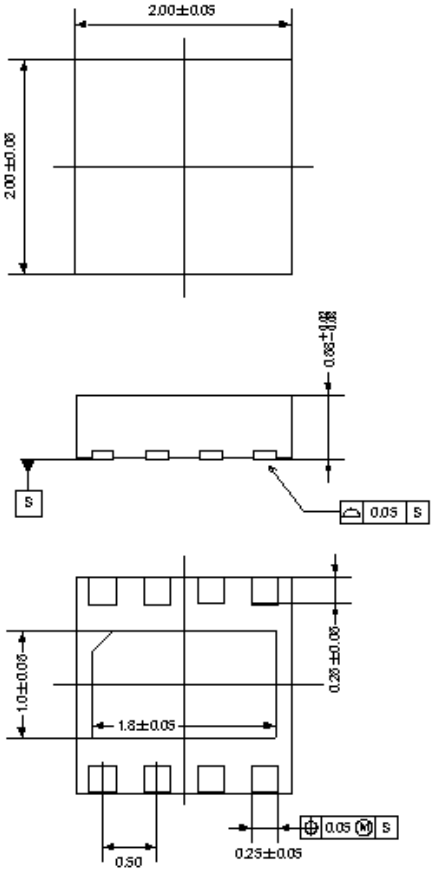


Note) It might cause a write access if SCLK rise while XLAT stay at "Low".

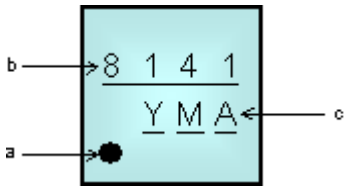
Symbol	Parameter	Min	Typ	Max	Unit
t1,t2	SCLK pulse width	50			ns
t3	SDATA setup time	50			ns
t4	SDATA hold time	50			ns
t5	SCLK rising edge to XLAT falling edge	50			ns
t6	XLAT pulse width	50			ns
t7	XLAT rising edge to SCLK falling edge	50			ns

Package Information

- **Mechanical data (Units:mm)**



- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (3 digits)

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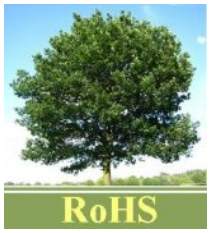
- **RoHS Compliance**



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(*) RoHS compliant products from AKEMD are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

Functional Description

Register map

AK8141 has one 8-bit register. The register map is shown below.

Address	Data							
A[7:0]	D7	D6	D5	D4	D3	D2	D1	D0
FFh	INFRQ1	INFRQ0	0	OUTFRQ4	OUTFRQ3	OUTFRQ2	OUTFRQ1	OUTFRQ0

Note) D5 should be set to "0".

Register setting

The data for the register is set via the serial interface such as SCLK pin, SDATA pin and XLAT pin.
It is recommended that the register access is executed while OE pin = "L".

Important

It must be set the appropriate data to the register as the procedure shown below after power up. The AK8141 does not have a reset function on the register.

<Register setting procedure after power up>

1) Power up with OE="L".
2) Set values to the register.
3) Set OE="H".

Register bit Function

INFRQ1-0 [Write] Input clock frequency is configured with these bits.

INFRQ1	INFRQ0	Input frequency
0	0	48MHz
0	1	24MHz
1	0	12MHz
1	1	27MHz

OUTFRQ4-0 [Write] Output clock frequency is configured with these bits.

OUTFRQ4	OUTFRQ3	OUTFRQ2	OUTFRQ1	OUTFRQ0	CLKOUT
0	0	0	0	0	27.00MHz
0	0	0	0	1	28.00MHz
0	0	0	1	0	29.00MHz
0	0	0	1	1	30.00MHz
0	0	1	0	0	31.00MHz
0	0	1	0	1	32.00MHz
0	0	1	1	0	33.00MHz
0	0	1	1	1	33.75MHz
0	1	0	0	0	34.00MHz
0	1	0	0	1	35.00MHz
0	1	0	1	0	36.00MHz
0	1	0	1	1	37.00MHz
0	1	1	0	0	38.00MHz
0	1	1	0	1	39.00MHz
0	1	1	1	0	40.00MHz
0	1	1	1	1	40.50MHz
1	0	0	0	0	41.00MHz
1	0	0	0	1	42.00MHz
1	0	0	1	0	43.00MHz
1	0	0	1	1	44.00MHz
1	0	1	0	0	45.00MHz
1	0	1	0	1	46.00MHz
1	0	1	1	0	47.00MHz
1	0	1	1	1	48.00MHz
1	1	0	0	0	49.00MHz
1	1	0	0	1	49.50MHz
1	1	0	1	0	50.00MHz
1	1	0	1	1	(*1)
1	1	1	0	0	(*1)
1	1	1	0	1	(*1)
1	1	1	1	0	(*1)
1	1	1	1	1	(*1)

(*1) 40.5MHz

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