ADVANCE INFORMATION

AMD

Am29BL16xC

16 Megabit (1 M x 16-Bit)
CMOS 3.0 Volt-only High Performance Burst Mode Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Choice of three architectures**
  - — Am29BL160C: 4 words sequential with wrap around (linear 4), bottom boot
  - — Am29BL161C: 4 words interleaved with wrap around (interleave 4), top boot
  - — Am29BL162C: 32 words sequential with wrap around (linear 32), bottom boot
  - — Sector sizes for all devices: One 8 Kword, two 4 Kword, one 112 Kword, and seven 128 Kword sectors
- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Read access times**
  - Burst access times as fast as 18 ns
  - Initial/random access times as fast as 65 ns
- **Alterable burst length via BAA# pin**
- **5 V-tolerant data, address, and control signals**
- **Sector Protection**
  - — Implemented using in-system or via programming equipment
  - — Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1 million write cycle guarantee per sector**
- **20-year data retention**
- **CFI (Common Flash Interface) compliant**
  - — Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
  - — Backward-compatible with AMD Am29LVxxx and Am29Fxxx flash memories
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device for reading array data
- **Package Options**
  - — 56-pin TSOP
  - — 56-pin SSOP

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GENERAL DESCRIPTION

The Am29BL16xC are 16 Mbit, 3.0 Volt-only burst mode Flash memory devices organized as 1,048,576 words. The device is offered in 56-pin TSOP and 56-pin SSOP packages. These devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply. A 12.0-volt V_{PP} or 5.0 V_{CC} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 65, 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Burst Mode Features

AMD Burst Flash devices require additional control pins for **burst operations**: Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The Am29BL16xC devices are offered in three different architectures. Each device is capable of providing a different mode of burst read operation:

Am29BL160C—Linear Burst: 4 word sequential burst with wrap around, bottom boot only

Am29BL161C—Interleaved Burst: 4 word interleaved burst with wrap around, top boot only

Am29BL162C—Linear Burst: 32 word sequential burst with wrap around, bottom boot only

AMD Flash Memory Features

Each device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. The I/O and control signals are 5V tolerant.

The Am29BL16xC is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

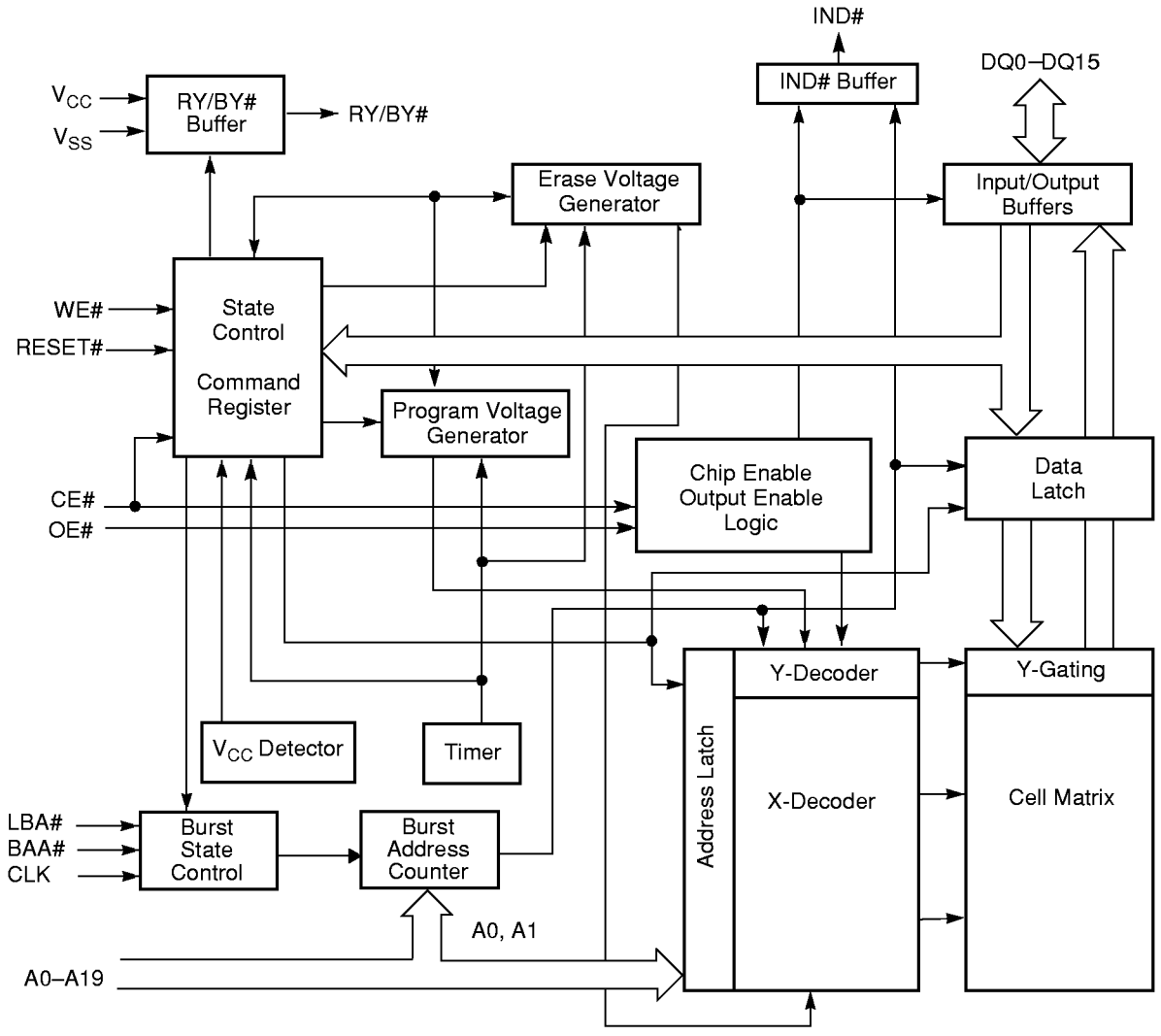
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number		Am29BL16xC				
Speed Option	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**65R**	**70R**			
	Full Voltage Range: V_{CC} = 2.7–3.6 V			**70**	**90**	**120**
Max access time, ns (t_{ACC})		65	70	70	90	120
Max CE# access time, ns (t_{CE})		65	70	70	90	120
Max OE# access time, ns (t_{OE})		18	20	20	25	28

BLOCK DIAGRAM FOR AM29BL160C/AM29BL162C



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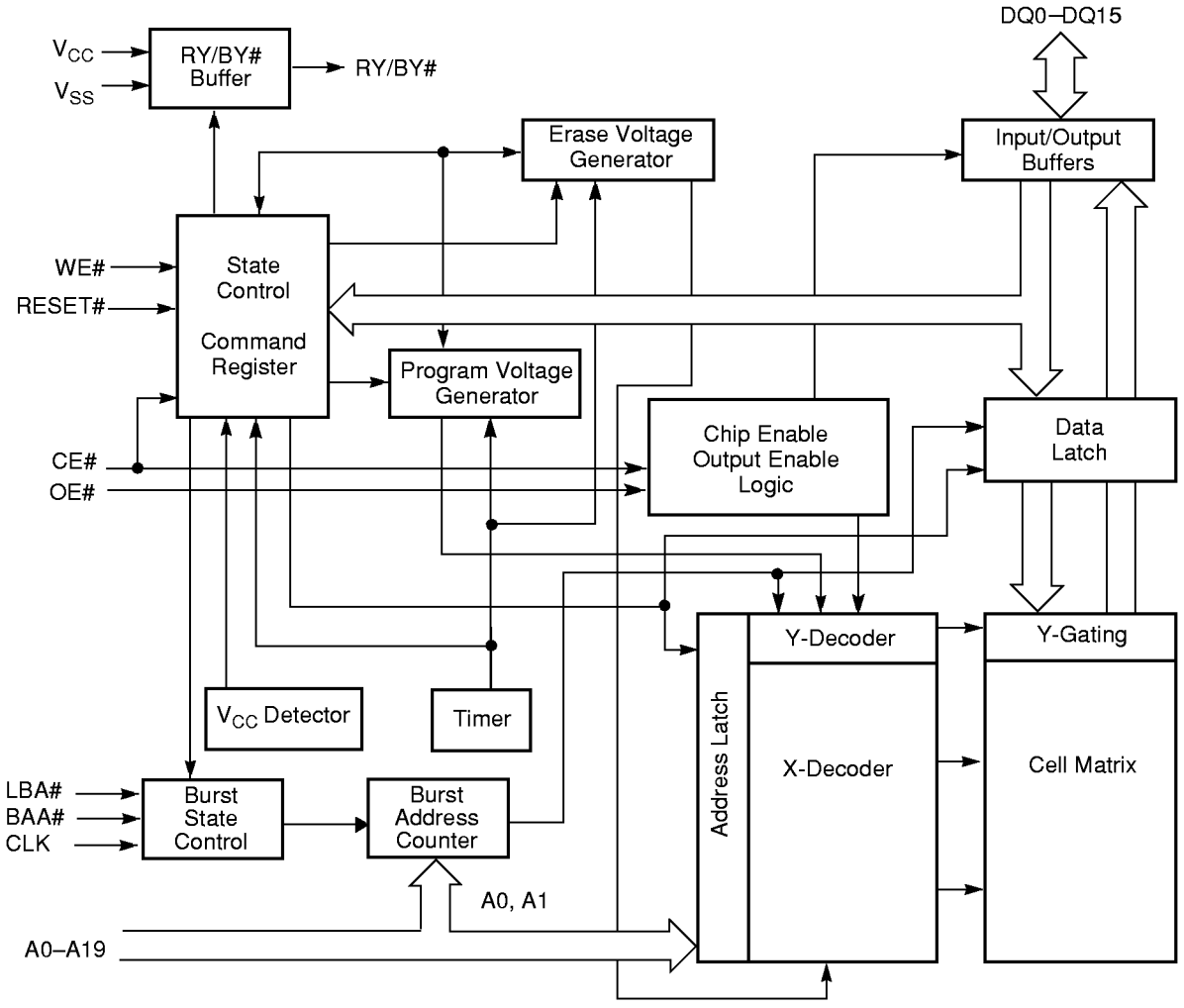
BLOCK DIAGRAM FOR AM29BL161C



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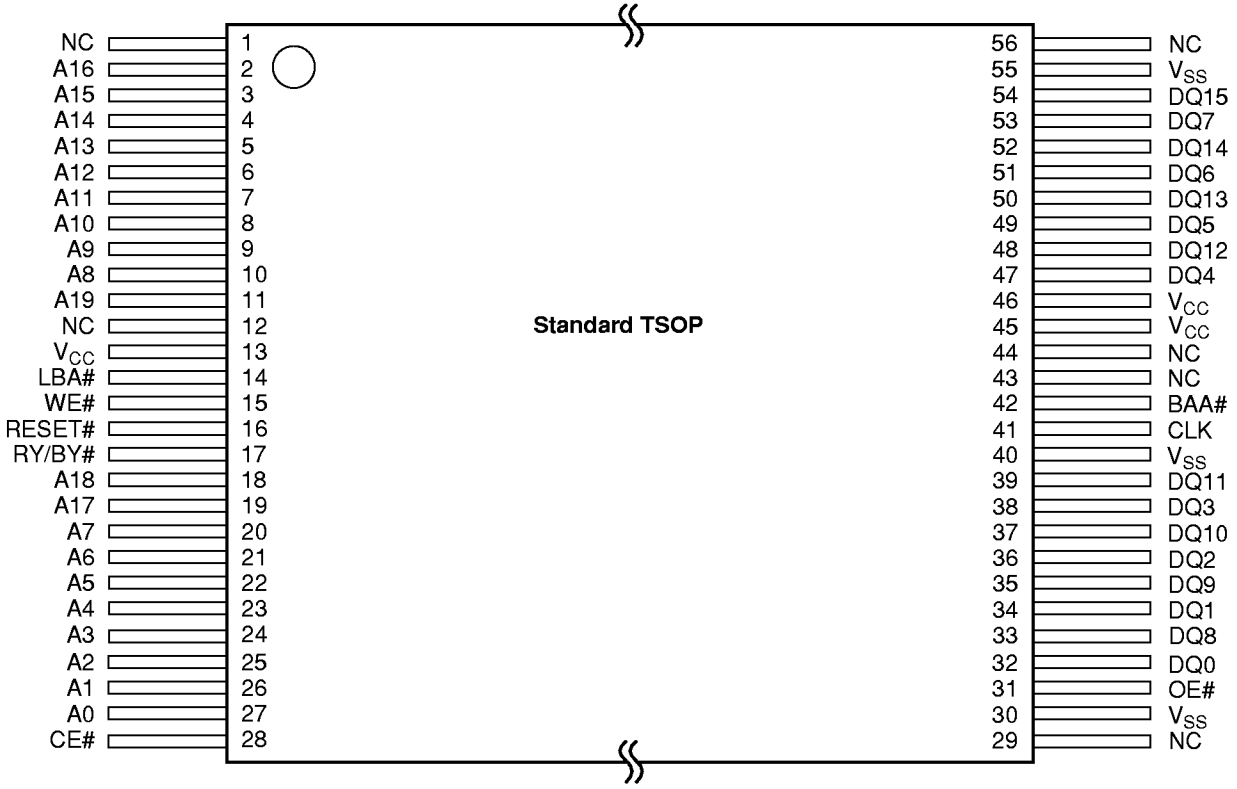
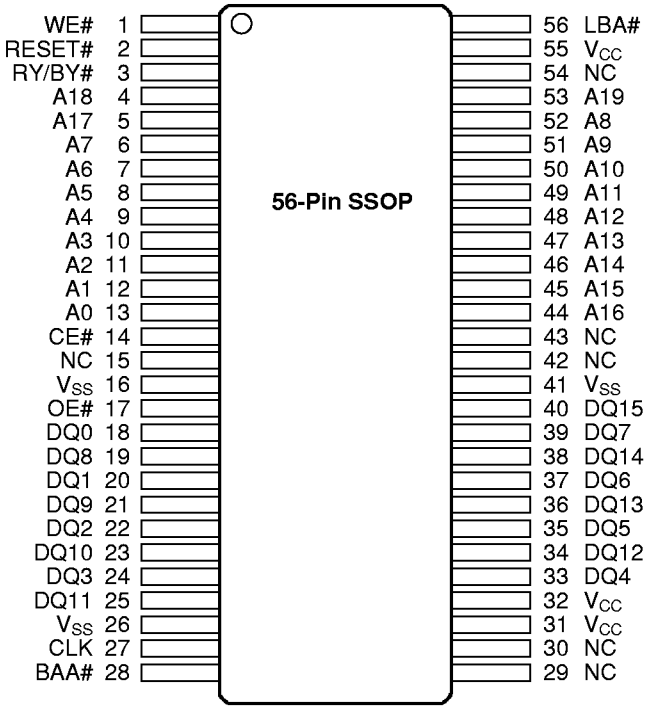
CONNECTION DIAGRAMS FOR Am29BL161C





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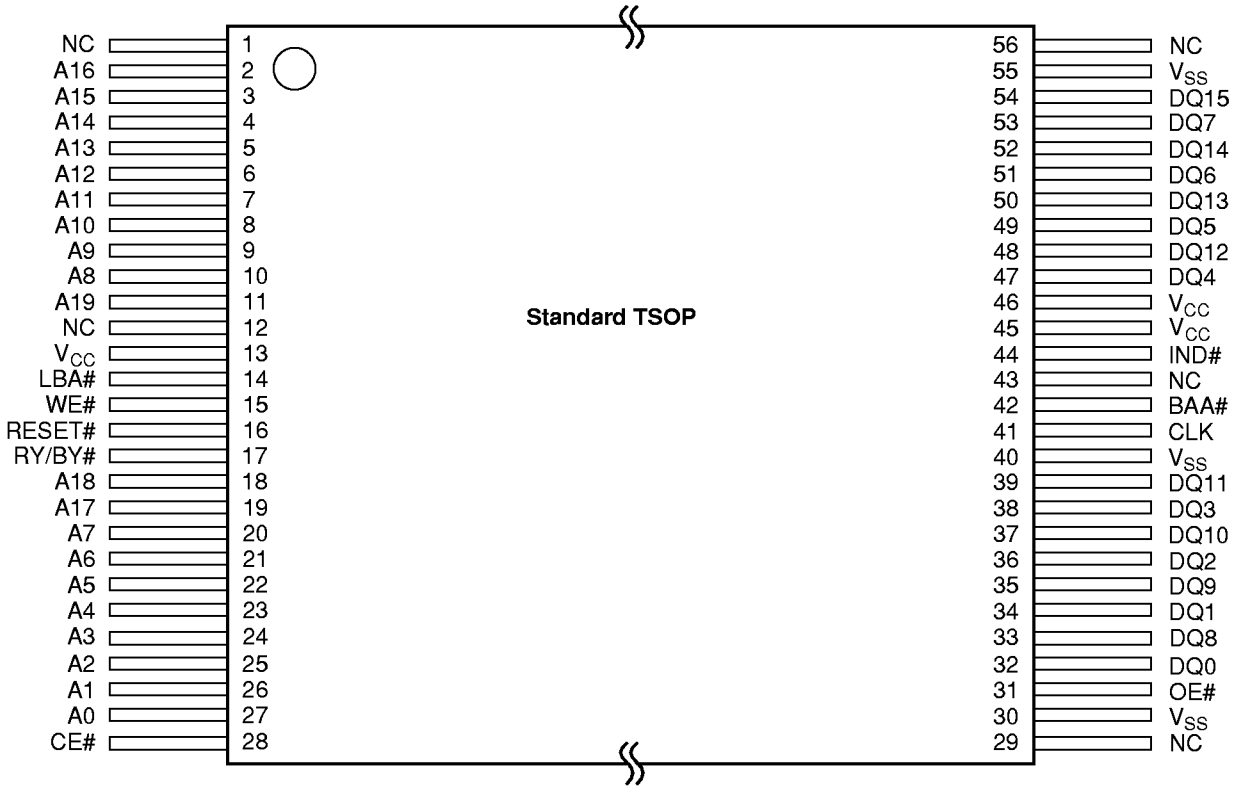
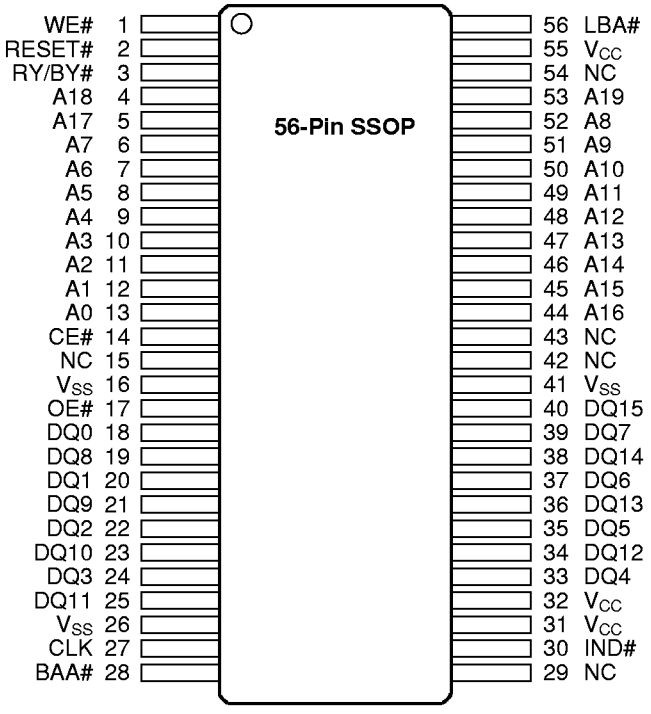
CONNECTION DIAGRAMS for Am29BL160C/Am29BL162C





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PIN CONFIGURATION

A0–A19 = 20 addresses

DQ0–DQ15 = 16 data inputs/outputs

CE# = Chip Enable Input. This signal shall be asynchronous relative to CLK for the burst mode.

OE# = Output Enable Input. This signal shall be asynchronous relative to CLK for the burst mode.

WE# = Write enable. This signal shall be asynchronous relative to CLK for the burst mode.

V_{SS} = Device ground

NC = No connect. Pin not connected internally

RY/BY# = Ready Busy output

CLK = Clock Input that can be tied to the system or microprocessor clock and provides the fundamental timing and internal operating frequency. CLK latches input addresses in conjunction with LBA# input and increments the burst address with the BAA# input.

LBA# = Load Burst Address input. Indicates that the valid address is present on the address inputs.

LBA# Low at the rising edge of the clock latches the address on the address inputs into the burst mode Flash device. Data becomes available t_{PACC} ns of initial access time after the rising edge of the same clock that latches the address.

LBA# High indicates that the address is not valid

BAA# = Burst Address Advance input. Increments the address during the burst mode operation

BAA# Low enables the burst mode Flash device to read from the next word when gated with the rising edge of the clock. Data becomes available t_{BACC} ns of burst access time after the rising edge of the clock

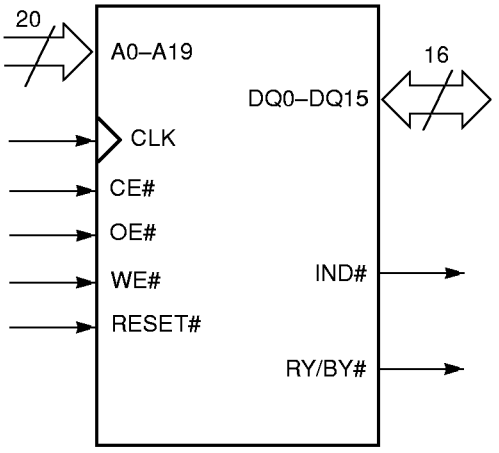
BAA # High prevents the rising edge of the clock from advancing the data to the next word output. The output data remains unchanged.

IND# = End of burst indicator. IND# is low when the last word in the burst sequence is at the data outputs.

RESET# = Hardware reset input

Note: *The address, data, and control signals (RY/BY#, LBA, BAA, IND, RESET, OE#, CE#, and WE#) are 5 V tolerant.*

LOGIC SYMBOL



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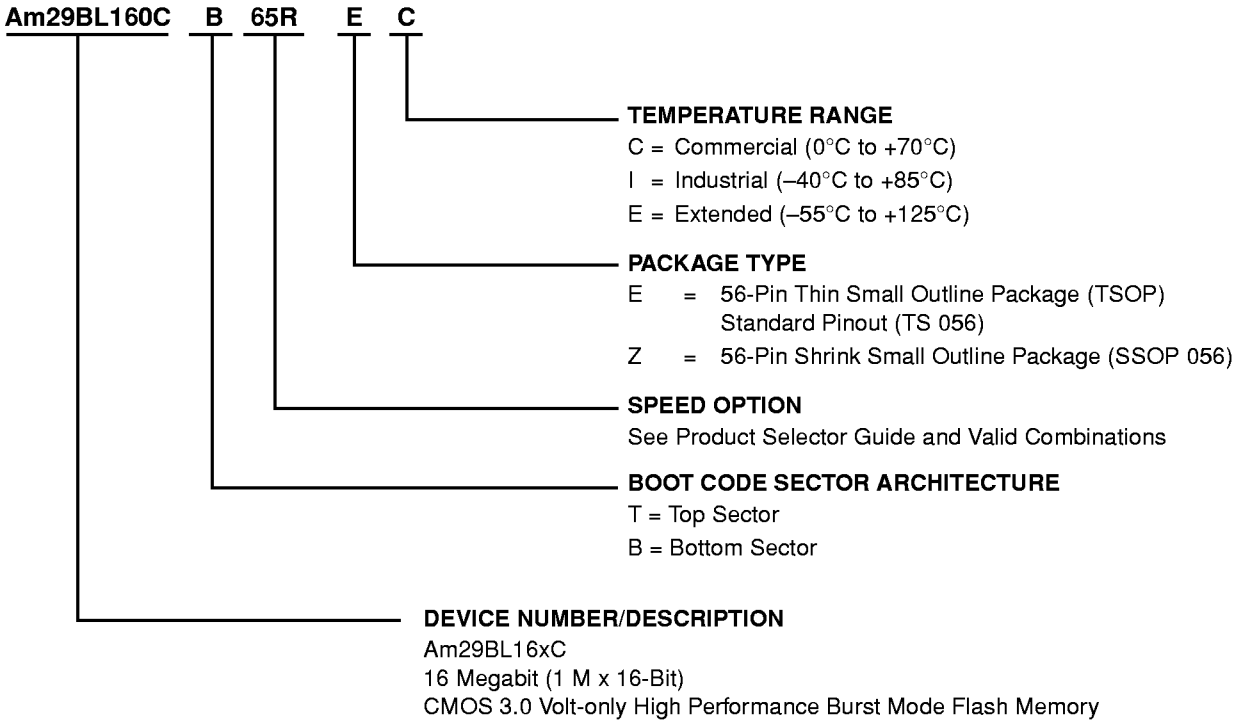
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29BL160CB65R Am29BL161CT65R Am29BL162CB65R	EC, ZC, EI, ZI, EE, ZE
Am29BL160CB70R Am29BL161CT70R Am29BL162CB70R	
Am29BL160CB70 Am29BL161CT70 Am29BL162CB70	
Am29BL160CB90 Am29BL161CT90 Am29BL162CB90	
Am29BL160CB120 Am29BL161CT120 Am29BL162CB120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

SECTOR ARCHITECTURE

Table 1. Am29BL160C/Am29BL162C Sector Address Table

Sector	Sector Size	Address Range
SA0	8 Kwords	00000h–01FFFh
SA1	4 Kwords	02000h–02FFFh
SA2	4 Kwords	03000h–03FFFh
SA3	112 Kwords	04000h–1FFFFh
SA4	128 Kwords	20000h–3FFFFh
SA5	128 Kwords	40000h–5FFFFh
SA6	128 Kwords	60000h–7FFFFh
SA7	128 Kwords	80000h–9FFFFh
SA8	128 Kwords	A0000h–BFFFFh
SA9	128 Kwords	C0000h–DFFFFh
SA10	128 Kwords	E0000h–FFFFFh

Table 2. Am29BL161C Sector Address Table

Sector	Sector Size	Address Range
SA0	128 Kwords	00000h–1FFFFh
SA1	128 Kwords	20000h–3FFFFh
SA2	128 Kwords	40000h–5FFFFh
SA3	128 Kwords	60000h–7FFFFh
SA4	128 Kwords	80000h–9FFFFh
SA5	128 Kwords	A0000h–BFFFFh
SA6	128 Kwords	C0000h–DFFFFh
SA7	112 Kwords	E0000h–FBFFFh
SA8	4 Kwords	FC000h–FCFFFh
SA9	4 Kwords	FD000h–FDFFFh
SA10	8 Kwords	FE000h–FFFFFh