Am90CL255

Low-Power 256K x 1 CMOS Nibble Mode DRAM

OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{CC5}	V_{CC} Supply Current CMOS Standby	$\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at V_{IH}, all other inputs and outputs $\geq V_{SS}$	Am90CL255		0.1	mA

The Am90CL255-15 is screened for I_{CC1} = 55 mA, I_{CC3} = 50 mA, and I_{CC4} = 16 mA.

AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following pages.

FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where t_{RC} = Refresh Cycle Time

and t_{RI} = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.

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SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL255-15 Min.	Am90CL255-15 Max.	Units
READ/WRITE/READ-MODIFY-WRITE CYCLE					
1	t_{RAC}	Access Time from $\overline{RAS}$ (Note 10)		150	ns
2	t_{CAC}	Access Time from $\overline{CAS}$ (Note 10)		60	ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	85		ns
4	t_{RC}	R/W Cycle Time (Note 3)	245		ns
5	t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	ns
6	t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	ns
7	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	0		ns
8	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 4)	30	90	ns
9	t_{RSH}	$\overline{RAS}$ Hold Time	60		ns
10	t_{CSH}	$\overline{CAS}$ Hold Time	150		ns
11	t_{ASR}	Row Address Setup Time	0		ns
12	t_{RAH}	Row Address Hold Time	20		ns
13	t_{ASC}	Column Address Setup Time	0		ns
14	t_{CAH}	Column Address Hold Time	25		ns
15	t_{AR}	Column Address Hold Time to $\overline{RAS}$ (Note 12)			ns
16	t_T	Transition Time	3	50	ns
17	t_{OFF}	Output Disable Time	0	30	ns
18	t_{REF}	Time Between Refresh		4	ms
READ CYCLE					
19	t_{RCS}	Read Command Setup Time	0		ns
20	t_{RCH}	Read Command Hold to $\overline{CAS}$	0		ns
21	t_{RRH}	Read Command Hold to $\overline{RAS}$	20		ns
WRITE CYCLE					
22	t_{WCS}	Write Command Setup	0		ns
23	t_{WCH}	Write Command Hold Time	25		ns
24	t_{WP}	Write Command Pulse Width	25		ns
25	t_{RWL}	Write Command to $\overline{RAS}$	30		ns
26	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	30		ns
27	t_{DS}	Data-In Setup Time	0		ns
28	t_{DH}	Data-In Hold Time	25		ns
READ-MODIFY-WRITE CYCLE					
29	t_{RWC}	RMW Cycle Time (Note 5)	245		ns
30	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	25		ns
31	t_{RRW}	RMW $\overline{RAS}$ Pulse Width (Note 6)	150	10,000	ns
32	t_{CRW}	RMW $\overline{CAS}$ Pulse Width (Note 7)	60		ns
NIBBLE MODE READ CYCLE					
33	t_{NC}	Nibble R/W Cycle Time (Note 8)	60		ns
34	t_{NCAC}	Nibble $\overline{CAS}$ Access Time	30		ns
35	t_{NCAS}	Nibble $\overline{CAS}$ Pulse Width	30		ns
36	t_{NCP}	Nibble $\overline{CAS}$ Precharge Time	20		ns
37	t_{NRSH}	Nibble $\overline{RAS}$ Hold Time	30		ns

Notes: See next page for notes.

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL255-15 Min.	Am90CL255-15 Max.	Units
NIBBLE MODE WRITE CYCLE					
38	t_{NCWL}	Nibble Mode Write-to-$\overline{CAS}$ Lead Time	30		ns
39	t_{NCWD}	Nibble $\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 11)	0		ns
40	t_{NCRW}	Nibble Mode RMW $\overline{CAS}$ Pulse Width	30		ns
41	t_{NWRH}	Nibble $\overline{RAS}$ Hold Time	40		ns
42	t_{NRWC}	Nibble RMW Cycle Time (Note 9)	65		ns

Notes:
1. An initial pause of 100 µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
2. Switching characteristics assume t_T = 5 ns. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. $t_{RC} = t_{RAS} + t_T + t_{RP} + t_T$.
4. $t_{RCD} = t_{RAH} + t_T + t_{ASC} + t_T$.
5. $t_{RWC} = t_{RRW} + t_{RP} + t_T + t_T$.
6. $t_{RRW} = t_{RCD}(Max) + t_{CWD} + t_T + t_{RWL}$.
7. $t_{CRW} = t_{CWD} + t_T + t_{CWL}$.
8. $t_{NC} = t_{NCAS} + t_T + t_{NCP} + t_T$.
9. $t_{NRWC} = t_{NCWD} + t_T + t_{NCWL} + t_T + t_{NCP} + t_T$.
10. All switching characteristic parameters are measured with a load equivalent of two TTL loads and 100 pF.
11. If the first Nibble Cycle is a Read-Modify-Write, the same cycle can be performed on the next three bits if $\overline{WE}$ stays LOW, or Read Cycle if $\overline{WE}$ is pulled HIGH prior to start of Nibble Cycle.
12. Timing requirements referenced to $\overline{RAS}$ are non-restrictive and are deleted from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. The hold times of the Column Address, D_{IN} and $\overline{WE}$, as well as t_{CWD} ($\overline{CAS}$-to-$\overline{WE}$ delay) are not restricted by t_{RCD}.

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