

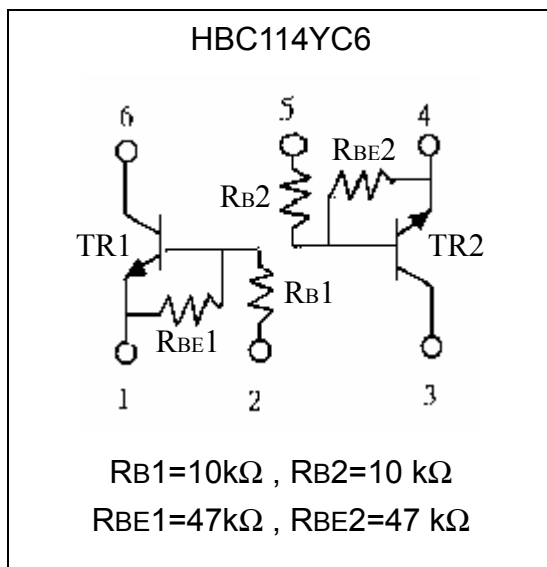
Dual NPN Digital Transistors

HBC114YC6

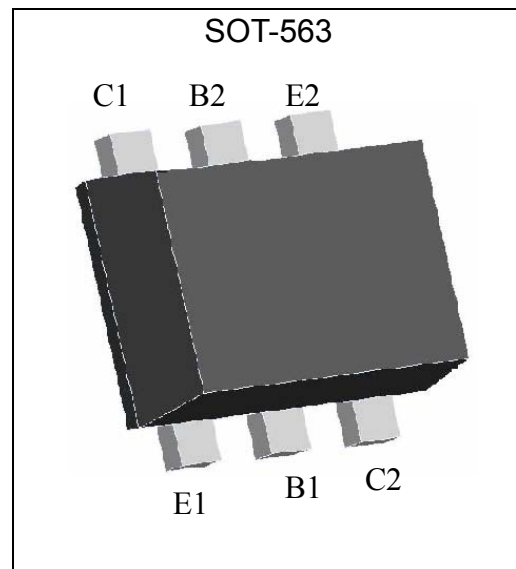
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Two DTC114Y chips in a SOT-563 package.
- Mounting by SOT-523 automatic mounting machines is possible.
- Mounting cost and area can be cut in half.
- Complements the HBA114YC6
- Pb-free package.

Equivalent Circuit



Outline



**Absolute Maximum Ratings** (Each Transistor, Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	V _{CC}	50	V
Input Voltage	V _{IN}	-6~+40	V
Output Current	I _O	70	mA
	I _{O(max.)}	100	mA
Power Dissipation	P _d	150 (Note)	mW
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note: 120mW per element must not be exceeded.**Electrical Characteristics** (Each Transistor, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V _{I(off)}	-	-	0.3	V	V _{CC} =5V, I _O =100μA
	V _{I(on)}	3	-	-	V	V _O =0.3V, I _O =1mA
Output Voltage	V _{O(on)}	-	0.1	0.3	V	I _O /I _I =5mA/0.25mA
Input Current	I _I	-	-	0.88	mA	V _I =5V
Output Current	I _{O(off)}	-	-	0.5	μA	V _{CC} =50V, V _I =0V
DC Current Gain	G _I	68	-	-	-	V _O =5V, I _O =5mA
Input Resistance	R ₁	7	10	13	kΩ	-
Resistance Ratio	R ₂ /R ₁	3.7	4.7	5.7	-	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =10V, I _C =5mA, f=100MHz *

* Transition frequency of the device

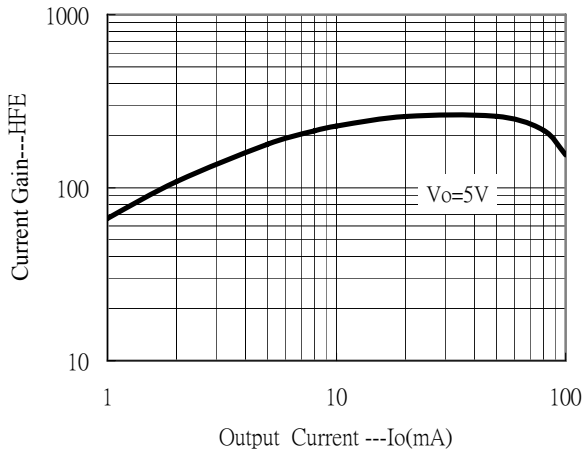
Ordering Information

Device	Package	Shipping	Marking
HBC114YC6	SOT-563 (Pb-free and halogen-free package)	3000 pcs / Tape & Reel	8D

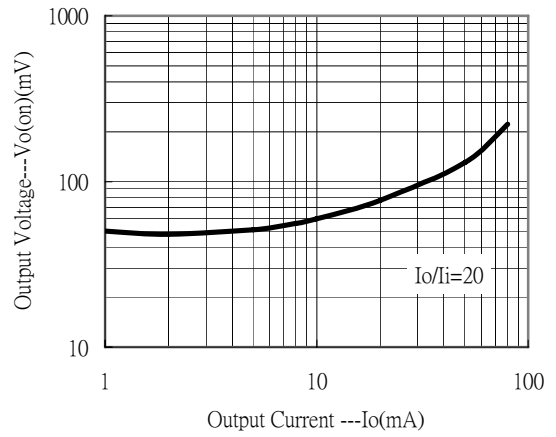


Typical Characteristics

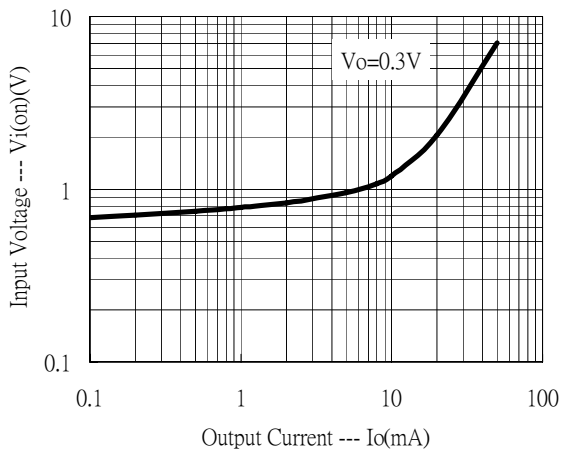
DC Current Gain vs Output Current



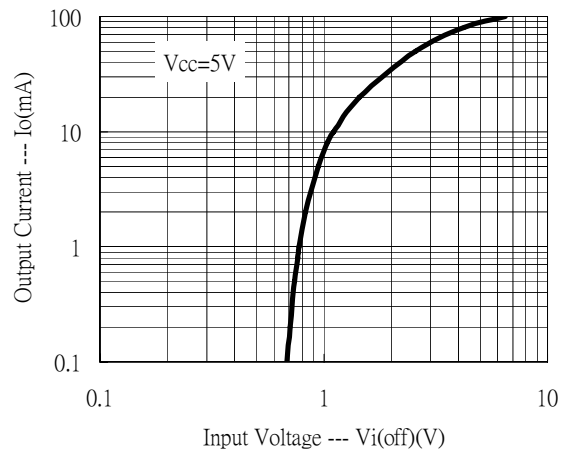
Output Voltage vs Output Current



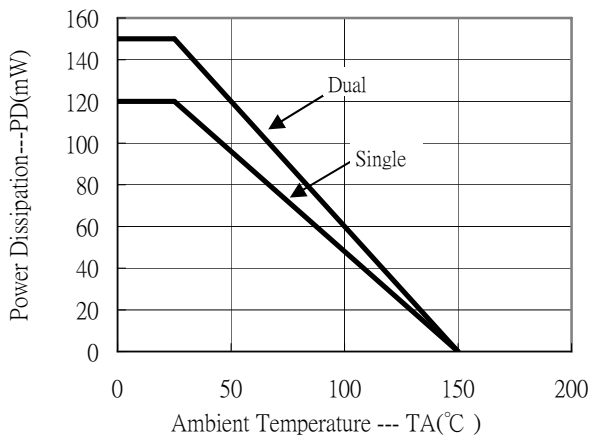
Input Voltage vs Output Current (ON Characteristics)



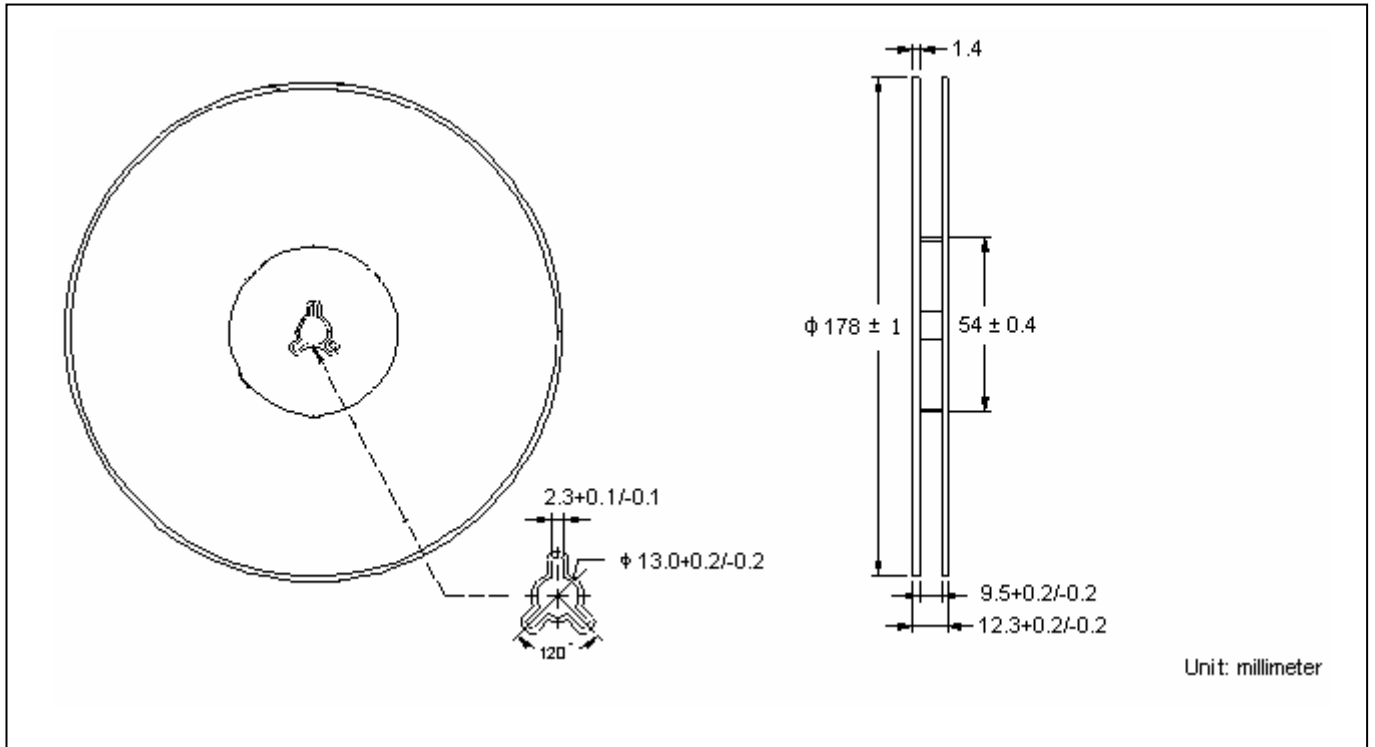
Output Current vs Input Voltage (OFF Characteristics)



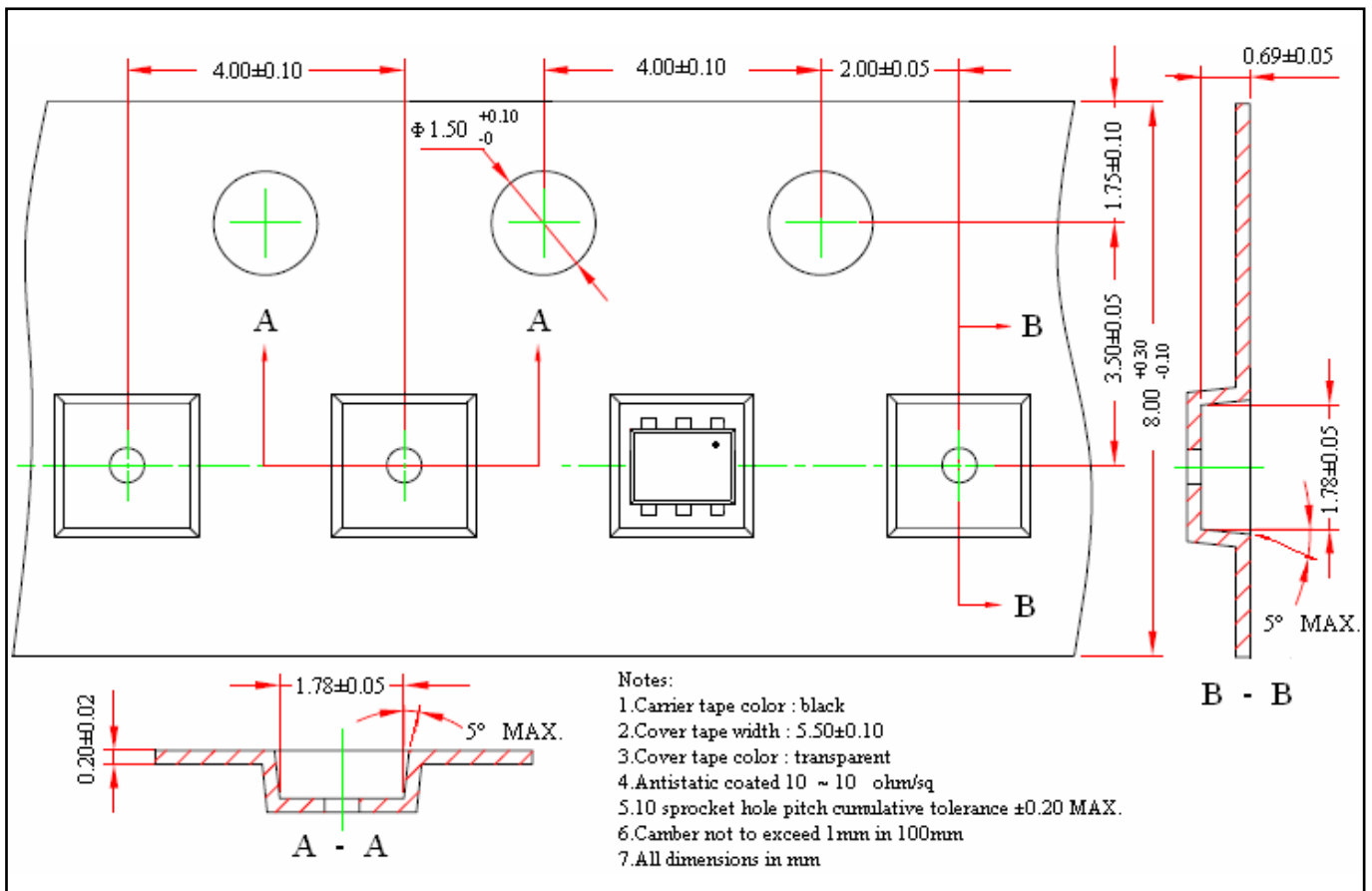
Power Derating Curves



Reel Dimension



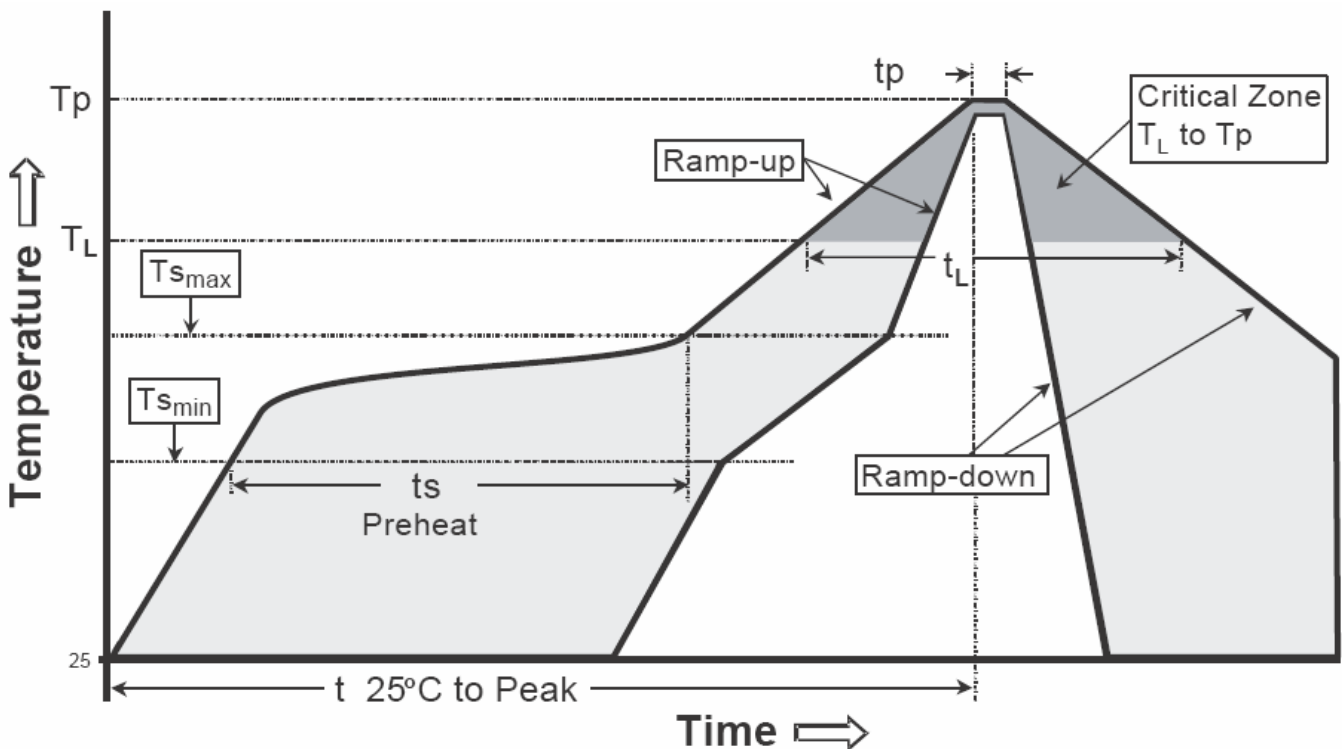
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

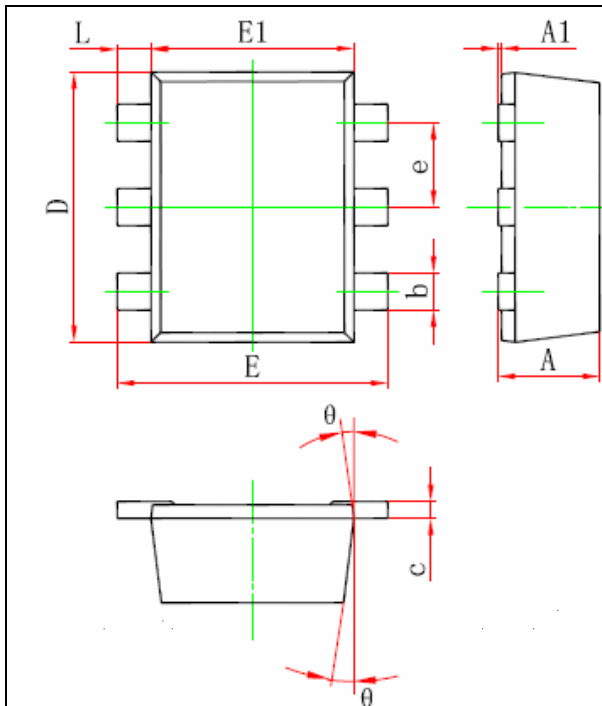
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

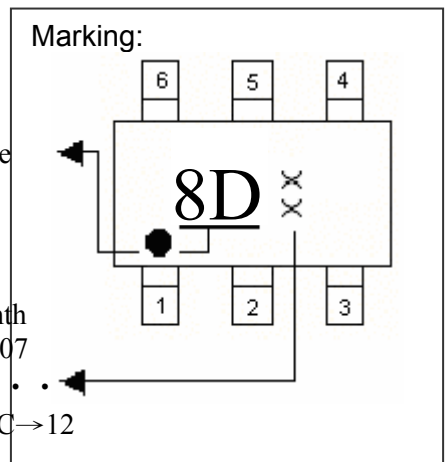
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-563 Dimension



The diagram shows three views of the SOT-563 package: a top view with dimensions L, E1, E, D, e, b, and θ ; a side view with dimensions A1 and A; and a perspective view of the lead with dimension c and θ .

Marking:



The marking diagram shows a top-down view of the package with pins numbered 1 to 6. The marking includes '8D', 'XX', and a 'Product Code' area.

Date Code: Year+Month
 Year: 6→2006, 7→2007
 Month: 1→1, 2→2, . . .
 9→9, A→10, B→11, C→12

Style:
 Pin 1. Emitter1 (E1)
 Pin 2. Base1 (B1)
 Pin 3. Collector2 (C2)
 Pin 4. Emitter2 (E2)
 Pin 5. Base2 (B2)
 Pin 6. Collector1 (C1)

**6-Lead SOT-563 Plastic Surface Mounted Package
 CYStek Package Code: C6**

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.021	0.024	0.525	0.600	b	0.007	0.011	0.170	0.270
A1	0.000	0.002	0.000	0.050	E1	0.043	0.051	1.100	1.300
e	0.018	0.022	0.450	0.550	E	0.059	0.067	1.500	1.700
c	0.004	0.006	0.090	0.160	L	0.004	0.012	0.100	0.300
D	0.059	0.067	1.500	1.700	θ	7° REF		7° REF	

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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