KTMicro

Stereo FM Receiver Radio-on-a-Chip™

KT0830EG

▪ Features

Fully compatible with KT0830E
Excellent radio reception with short antenna
32.768KHz and 38KHz crystal support
Variable reference clock support including 32.768 KHz/7.6MHz/12MHz/24MHz
Excellent tuning experience with built in SNR meter and RSSI

Low-cost true single-chip FM radio solution
- Single-Chip Low IF FM Receiver
- Direct band, volume, frequency selection
- Digital FM Demodulator
- Digital Stereo Processor
- Low-noise PLL with integrated VCO

Extended FM band support (64-109MHz)
Integrated Class AB headphone driver
High Fidelity
- SNR: 64dB
- THD: <0.3%

High Sensitivity: -106dBm
Low supply current
- 19mA (operating), 1uA (power-down)

High Driving capability
- Drive up to 16 ohm load (single-sided)

Automatic Frequency Control (AFC)
Automatic gain control (AGC)
Anti-pop circuit
16-pin SOP package

▪ Applications

Single chip FM radio used in PMP, boom box, sporting devices, medical devices and etc

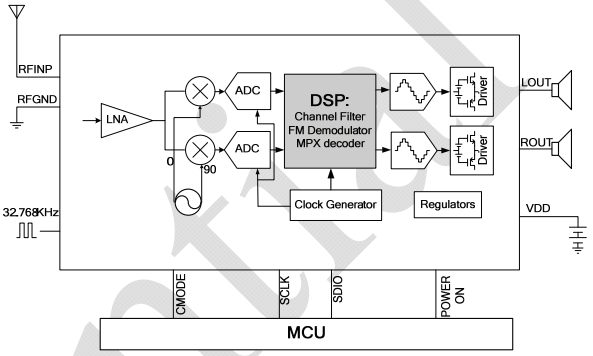

Figure 1: System Diagram

▪ Description

The KT0830EG is a high-quality Monolithic Digital FM Receiver designed to playback high-fidelity FM broadcasting signals under various conditions.

The KT0830EG offers a true single-chip FM radio solution. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture, a fully-integrated LNA, automatic gain control (AGC), high-performance ADCs, high-quality analog and digital filters, and an on-chip low-noise self-tuning VCO. The on-chip high-fidelity Class-AB driver further eliminates the need for any external audio amplifiers and can drive stereo headphones directly.

The on-chip LDO regulator allows the chip to operate with power supply ranging from 2.0V to 3.6V consuming merely 19mA in full operation mode and less than 10uA when standby – greatly extending the battery life.

The small footprint, high integration level and great flexibility make KT0830EG for any standalone FM radio applications.

Rev. 1.2

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1 *Electrical specification*

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Power Supply	VDD	Relative to Vss	2.0	3.3	3.6	V
Operating Temp	Tj	Junction Temperature	-20	50	110	°C

Table 2: DC Characteristics

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	I_A		-	19	-	mA
Standby Current	I_{APD}			6	10	μA
Power-down Current	I_{PD}			1	3	μA

Table 3: FM Receiver Characteristics

(Unless otherwise noted Tj = -20~110 °C, VDD =2.0V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
FM Frequency Range	F_{rx}		64		109	MHz
Sensitivity[1,2,3]	Sen	(S+N)/N=26dB		2.2	3.5	uVemf
Input referred 3rd Order Intermodulation Production[4,5]	IIP3			87		dBuVEMF
Adjacent Channel Selectivity		±200KHz	40		51	dB
Alternate Channel Selectivity		±400KHz	50		70	dB
Image Rejection Radio				35		dB
AM suppression				50		dB
RCLK frequency			32	32.768	26000	KHz
RCLK frequency Range[8]			-100		100	ppm
Audio Output Voltage[1,2,3,4]		32ohm load	68	70	72	mV_{RMS}
Audio Band Limits[1,2,4]		±3dB	30		15k	Hz
Audio Stereo Separation [1,4,6]			35			dB
Audio Stereo S/N[1,4,6,7]				64		dB
Audio THD[1,2,4,6]				0.3		%
Audio Common Mode Voltage				0.7		V
Audio Output Load Resistance	R_L	Single-ended	16			Ω
Seek/Tune Time (effective channel)					50	ms/ch
Power-up Time					380	ms

Notes:
1. FMOD=1kHz, 75us de-emphasis
2. MONO=1
3. △F=22.5kHz
4. V_{EMF}=1mV, Frx=70MHz~110MHz
5. AGCD=1
6. △F=75kHz
7. VOLUME<3:0>=1111
8. The supported RCLK frequency is not continuous. Please refer to application notes.

2 Pin List

A 16-pin SOP package is used. The chip IO pin-out is listed in Table 4.

Table 4 Pin-Out

Pin Index	Name	I/O Type	Function
1	VDD	Power	2.0V – 3.6V Power supply
2	GND	Ground	Ground
3	GND	Ground	Ground
4	SCLK	Digital Input	I2C clock input.
5	SDIO	Digital IO	I2C data input/output
6	LOUT	Analog output	Left channel output with 16 ohm driving capability.
7	ROUT	Analog output	Right channel output with 16 ohm driving capability.
8	GND	Ground	Ground
9	VDD	Power	2.0V – 3.6V power supply.
10	XI/RCLK	Analog IO	32.768KHz crystal input or 32.768KHz external reference clock input.
11	XO	Analog IO	32.768KHz crystal input
12	POWER_ON	Digital Input	High for normal operating mode and low for standby mode.
13	N.C.	N.C.	No Connection
14	GND	Ground	Ground
15	RFINP	Analog Input	RF signal input. External AC coupling cap is not required
16	GND	Ground	Ground

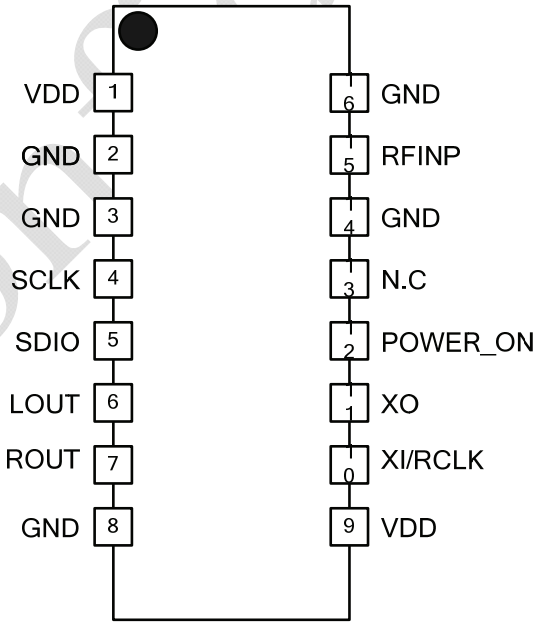
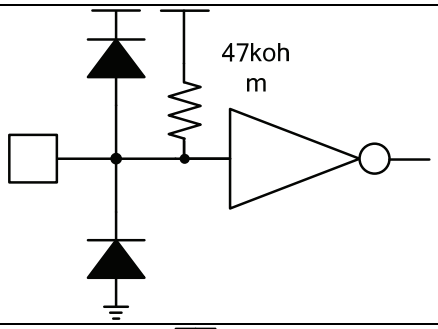
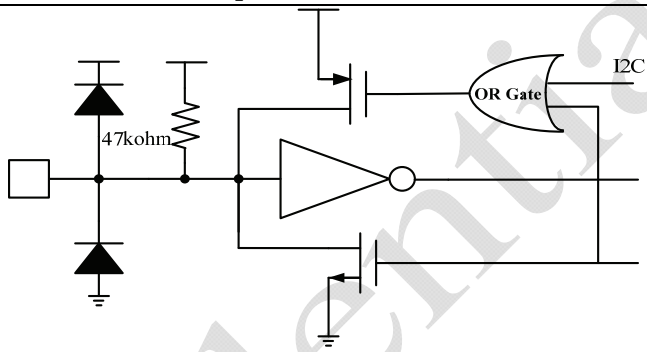
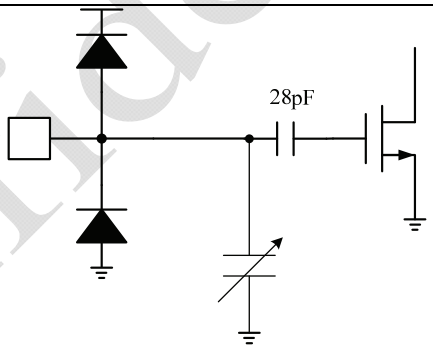
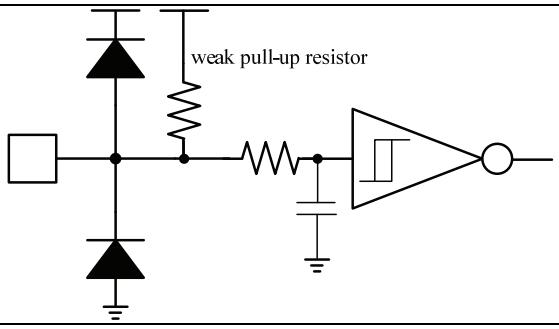


Figure 2: Pin out

Table 5: I/O Pin Configuration

PAD	Schematic
SCLK	
SDIO	
RFINP	
POWERON	

3 Functional Description

3.1 Overview

The KT0830EG offers a true single-chip FM radio solution by virtually eliminating all the external components. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture, a fully-integrated LNA, automatic gain control (AGC), high-performance ADCs, high-quality analog and digital filters, and an on-chip low-noise self-tuning VCO. The on-chip high-fidelity Class-AB driver further eliminates the need for any external audio amplifiers and can drive stereo headphones directly.

3.2 FM Receiver

A high performance digital-IF structure receiver is used in KT0830EG to convert RF signal to IF signal. The received IF signal is digitized by a high resolution analog to digital converter (ADC) and all of the following signal processing including channel filtering, FM demodulation and stereo decoding is performed digitally. In order to improve the dynamic range of the RF signal, an automatic gain control (AGC) loop is used together with the low noise amplifier (LNA).

3.3 Digital Signal Processing

3.3.1 Stereo Decoder

The digitized IF signal is fed to the FM demodulator which demodulates the signal and outputs a digital multiplexed (MPX) signal consisting of L+R audio, L-R audio, 19kHz pilot tone. The left channel signal and the right channel signal can be extracted from the MPX signal by simply adding and subtracting the L+R signal and L-R signal. The spectrum diagram is shown in Figure 3.

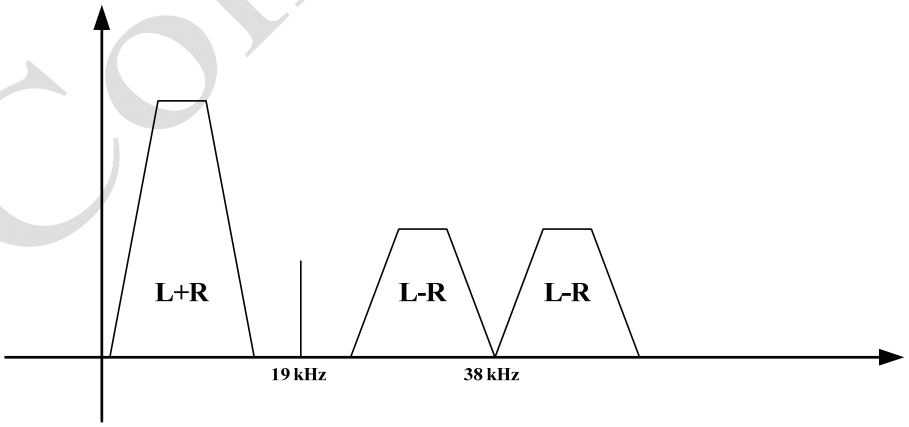


Figure 3: Spectrum diagram of the MPX signal

3.3.2 Mute

KT0830EG can be hard muted by setting VOLUME to 0 and the output of the audio signal is set to the common mode voltage.

There is also a Soft Mute feature that is enabled by setting SMUTE_B to 0. In this mode, the audio volume is gradually attenuated when the signal reception is bad (i.e. when the RSSI or SNR, which is determined by reg SMMD, is below a certain level as defined by SMTH<2:0>.) The reg VOLUMET<3:0> sets the lowest volume that the internal state machine can reach. The attenuation attack rate and depth can be configured through SMUTER<1:0> and SMUTEA<1:0>, respectively.

3.3.3 Stereo / Mono Blending

In order to provide a comfortable listening experience, KT0830EG blends the stereo signal with mono signal gradually when in weak reception. The signal level range over which the blending occurs is set by BLNDADJ<1:0>. The blending is disabled when DBLND is set to 1. MONO playback mode can also be forced by setting the MONO to 1.

3.3.4 Bass Boosting

KT0830EG provides a digital audio enhancement feature, bass boosting. The gain of the bass boost can be programmed through BASS<1:0> (Reg0x04<9:8>). With BASS<1:0>=00, this feature is disabled.

3.4 Stereo DAC, Audio Filter and Driver

Two high-quality single-bit ΔΣ audio digital to analog converters (DAC) are integrated along with high-fidelity analog audio filters and class AB drivers. Headphones or speakers with impedance as low as 16ohms can be directly driven without external audio drivers. An integrated anti-pop circuit eliminates the click-and-pop sound during power up and power down.

3.5 SEEK/TUNE

The fully integrated LO synthesizer supports wide band operation from 64MHz to 110MHz. The chip begins to directly TUNE to a channel when the register TUNE is set to 1. The channel frequency can be programmed and tuned by setting CHAN<9:0> which is defined as

$$\text{Freq(MHz)} = 50\ \text{kHz} \times \text{CHAN<9:0>} + 64\ \text{MHz}$$

The Seeking process is started by setting SEEK to “1”. Two built-in seek methods are available, which are distinguished by setting SEEK_SEL. Seeking direction is determined by SEEKDIR. The band edges are determined by BAND<1:0> and the seek step is set by SPACE<1:0>. KT0830EG automatically seeks and tunes to the first satisfying station. If no qualified channel is found, the FM receiver returns to the original channel and SF/BL bit is set to “1”. when SEEKMD is set to 0. Alternatively, if SEEKMD is set to 1 and no qualified channel is found, the chip stops at the band edge while setting SF/BL bit to 1. When AUTOTUNE bit is set to 1, the chip will automatically tune to the found channel, otherwise, the chip will remain mute after

seek is completed. During the seeking, the current channel can be read out from READCH<9:0> bits. Refer to application notes for more information.

3.6 Power on Sequence

KT0830EG is powered up by pulling the POWER_ON pin to high. or leaving this pin not connection. No external power-on reset circuit is required. One needs to wait for 400ms before he/she can configure the chip through the serial interface.

3.7 Reference Clock

The KT0810G support variable reference clock frequencies, such as 32.768KHz, 7.6MHz, 12MHz, 13MHz, 24MHz, 26MHz and etc. The built-in crystal oscillator also supports 32.768KHz and 38KHz crystal. Please refer to application notes for more information about setting different reference clock.

4 Control Interface- I2C

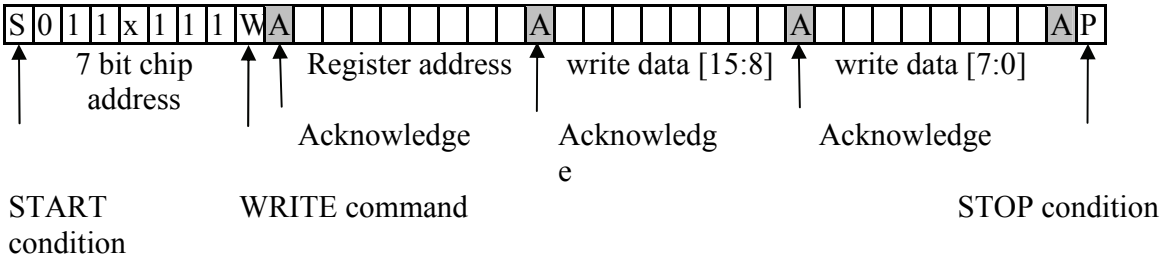
I2C bus mode uses SCLK and SDIO to transfer data. The device always drives data to SDIO at the falling edge of SCLK and captures data from SDIO at the rising edge of SCLK. The device acknowledges the external controller by driving SDIO low at the falling edge of SCLK. Data transfer always begins with START condition and ends with STOP condition. The external controller can read/write one 16-bits data at the specified address or read/write desired number of registers data continuously from the specified address till when STOP condition is occurred.

For write operations, external controller should send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> write data n [15:8] -> write data n [7:0] -> write data n+1 [15:8] -> write data n+1 [7:0] -> …… -> STOP condition.

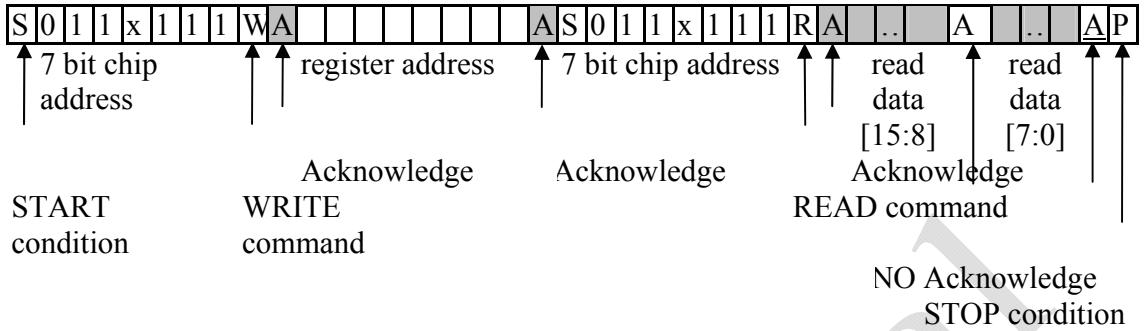
For read operations, external controller should send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> 7 bit chip address and Read command (“1”) , then device will send read data n [15:8] -> read data n [7:0] -> read data n+1 [15:8] -> read data n+1 [7:0] -> …… till STOP condition.

Table 6 : I2C Interface Protocol

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



Note: The data bits in gray color are sent by KT0830EG

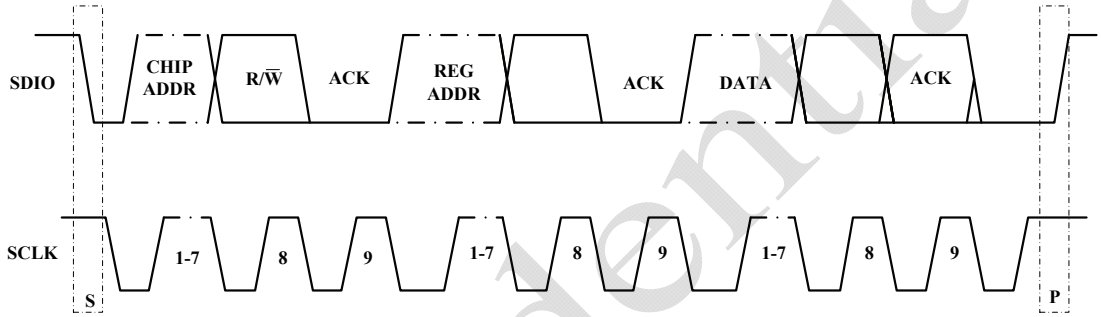
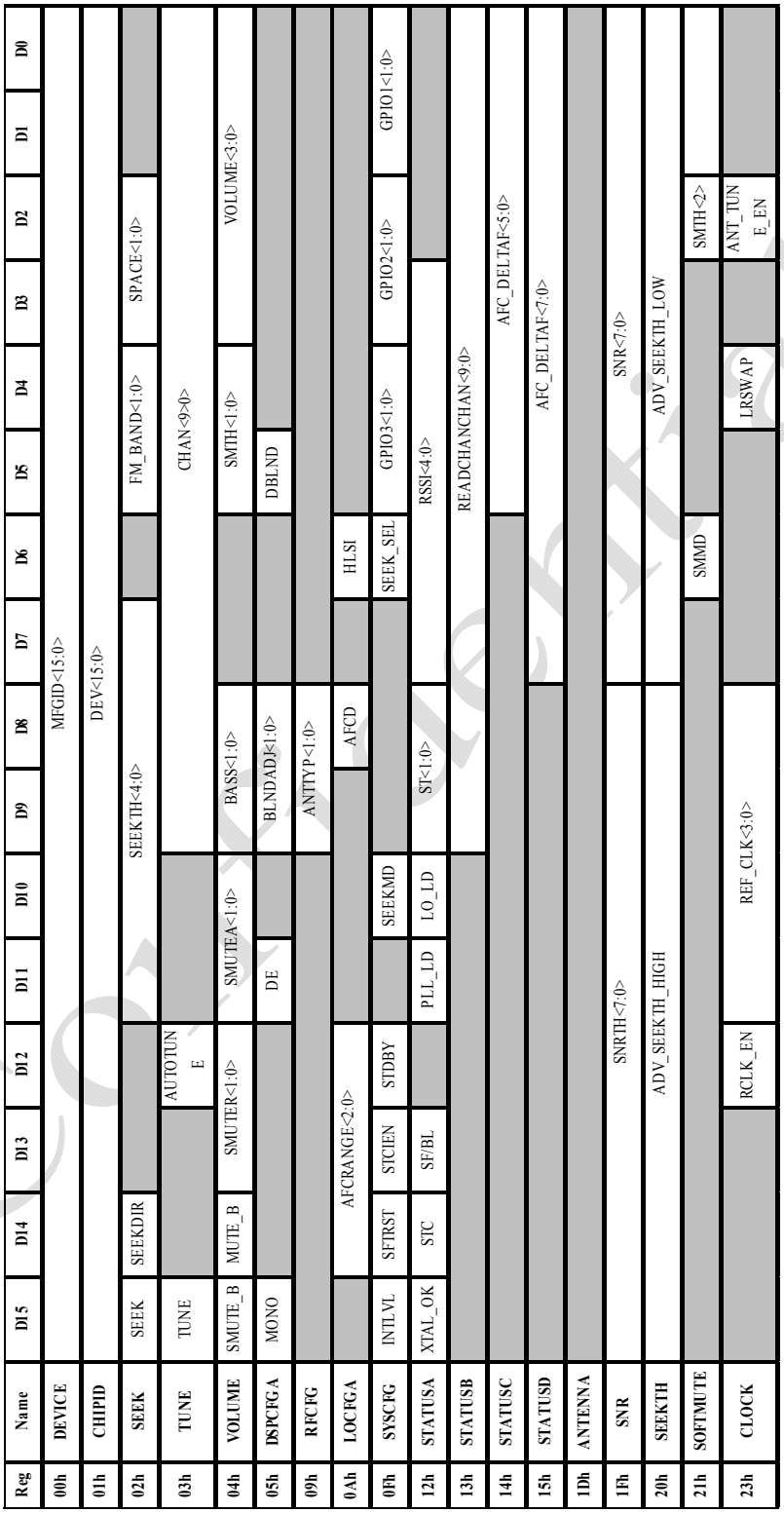


Figure 4: I2C interface timing diagram

5 Register Map



Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	DEVICE	MFGID<15:0>															
01h	CHIPID	DEV<15:0>															
02h	SEEK	SEEK	SEEKDIR					SEEKTH<4:0>				FM_BAND<1:0>		SPACE<1:0>			
03h	TUNE	TUNE			AUTOTUNE			CHAN<9:0>									
04h	VOLUME	SMUTE_B	MUTE_B	SMUTER<1:0>		SMUTEA<1:0>		BASS<1:0>				SMTH<1:0>		VOLUME<3:0>			
05h	DSPCFGA	MONO				DE		BLNDADJ<1:0>				DBLND					
09h	RFCFG							ANTTYP<1:0>									
0Ah	LOCFGA		AFCRANGE<2:0>						AFCD		HLSI						
0Fh	SYSCFG	INTLVL	SFTRST	STCIEN	STDBY		SEEKMD				SEEK_SEL	GPIO3<1:0>		GPIO2<1:0>		GPIO1<1:0>	
12h	STATUSA	XTAL_OK	STC	SF/BL		PLL_LD	LO_LD		ST<1:0>			RSSI<4:0>					
13h	STATUSB	READCHANCHAN<9:0>															
14h	STATUSC	AFC_DELTAF<5:0>															
15h	STATUSD	AFC_DELTAF<7:0>															
1Dh	ANTENNA																
1Fh	SNR	SNR<7:0>															
20h	SEEKTH	ADV_SEEKTH_LOW															
21h	SOFTMUTE										SMMD				SMTH<2>		
23h	CLOCK	REF_CLK<3:0>			RCLK_EN								LRSWAP			ANT_TUNE_EN	

The register bank stores channel frequency codes, calibration parameters, operation status, mode and power controls, which can be accessed by the internal digital controller, state machines and external micro controllers through the serial interface.
All registers are 16 bits wide. Control logics are active high unless specifically noted. **All the registers are automatically set to default values after the chip is powered-on or reset.**

5.1 Device ID Register (Reg 0x00)

Bit	Symbol	Access	Default	Functional Description
15:0	MFGID<15:0>	R	0xb002	**Manufacturer ID**

5.2 CHIP ID (Reg 0x01)

Bit	Symbol	Access	Default	Functional Description
15:0	DEV<15:0>	R	0x0440	**Part Number** 0x0440=FM Receiver

5.3 Seek Configuration (Reg 0x02)

Bit	Symbol	Access	Default	Functional Description
15	SEEK	RW	0	**Seek enable** 0 = Disable 1 = Enable
14	SEEKDIR	RW	0	**Seek direction** 0 = Seek down 1 = Seek up
13:12	Reserved	RW	10	**Reserved**
11:7	SEEKTH<4:0>	RW	00110	**Seek Threshold** 00000 = most sensitive 11111 = least sensitive
6	Reserved		0	Reserved
5:4	FM_Band<1:0>	RW	00	**Band Selection** 00 = 87-108MHz (USA, Europe) 01 = 76-108MHz (Japan wide band) 10 = 76-90MHz (Japan). 11 = reserved
3:2	SPACE<1:0>	RW	00	Channel spacing 00 = 200KHz (US, Europe) 01 = 100KHz (Europe, Japan) 10 = 50KHz
1:0	Reserved		11	Reserved

5.4 TUNE Register (Reg 0x03)

Bit	Symbol	Access	Default	Functional Description

15	Tune	RW	0	**Tune Enable** 0 = Disable 1 = Enable
14:13	Reserved	RW	00	
12	AUTOTUNE	RW	1	**Automatic tune control** 0 = Will NOT tune after a successful seek until a separated Tune command is received from the control interface 1 = Automatically starts Tune process after Seek
11:10	Reserved	RW	10	
9:0	Chan<9:0>	RW	1CC	Tune Channel Value

5.5 VOLUME Control Register (Reg 0x04)

Bit	Symbol	Access	Default	Functional Description
15	SMUTE_B	RW	1	**Softmute Disable** 0 = Softmute enable 1 = Softmute disable
14	MUTE_B	RW	0	**Hard Mute Disable** 0 = Mute enable 1 = Mute disable
13:12	SMUTER<1:0>	RW	00	**Softmute Attack/Recover Rate** 0 = Slowest 01 = Fastest (RSSI mode only) 10 = Fast 11 = Slow
11:10	SMUTEA<1:0>	RW	00	**Softmute Attenuation** 00 = Strong 01 = Strongest 10 = Weak 11 = Weakest
9:8	BASS<1:0>	RW	00	**Bass boost effect mode selection** 00 = Disable 01 = Low 10 = Med 11 = High
7:6	Reserved		00	
5:4	SMTH<1:0>	RW	10	**Soft mute start level together with SMTH<2> in reg0x21** 000 = Lowest …… 111 = Highest

3:0	VOLUME<3:0>	RW	0111	**Volume Control** 0000 = mute 0001 = -42dBFS 0010 = -39dBFS …… ……. 1110 = -3dBFS 1111 = FS

5.6 DSP Configuration Register A (Reg 0x05)

Bit	Symbol	Access	Default	Functional Description
15	MONO	RW	0	**Mono Select** 0 = Stereo 1 = Force mono
14:12	Reserved	RW	101	Reserved
11	DE	RW	0	**De-emphasis** 0 = 75us. Used in USA. 1 = 50us. Used in Europe, Australia, Japan.
10	Reserved	RW	0	
9:8	BLNDADJ<1:0>	RW	00	**Stereo/Mono Blend Start Level** 00 = High 01 = Highest 10 = Lowest 11 = Low Note: Write 00 explicitly even if 00 is the default value.
7:6	Reserved	RW	00	**Reserved**
5	DBLND	RW	0	**Blend disable** 0 = blend enable 1 = blend disable
4:0	Reserved		00000	**Reserved**

5.7 LO Synthesizer Configuration A (Reg 0x0A)

Bit	Symbol	Access	Default	Functional Description
15	**Reserved**	**RW**	**0**	
14:12	AFCRANGE<2:0>	RW	000	AFC correction range 000 = 12KHz 001 = 15KHz 010 = 14KHz 011 = 17KHz 100 = 16KHz 101 = 19KHz 110 = 22KHz 111 = 25KHz
11:9	Reserved	RW	000	

8	AFCD	RW	1	**AFC disable control bit** 0 = AFC enable 1 = AFC disable
7	Reserved	RW	0	
6	HLSI	RW	0	**High side or low side injection** 1 = high side injection 0 = low side injection
5:0	Reserved	R	000000	**Reserved**

5.8 System Configuration Register (Reg 0x0F)

Bit	Symbol	Access	Default	Functional Description
15	INTLVL	RW	1	**Interrupt level control (GPIO2)** 0 = low level interrupt 1 = high level interrupt
14	SFTRST	RW	0	**Soft reset bit** 0 = normal operation 1 = soft reset
13	STCIEN	RW	0	**Seek/Tune Complete Interrupt Enable** 0 = Disable Interrupt 1 = Enable Interrupt
12	STDBY	RW	0	**Standby mode (See version notes)** 0 = disable 1 = enable
11	Reserved	RW	1	**Reserved**
10	SEEKMD	RW	0	**Seek mode selection** 0 = cycling seek 1 = stop at the band edge.
9:7	Reserved	RW	100	
6	SEEK_SEL	RW	0	SEEK Method Selection 0 = Traditional method 1 = Advanced method
5:4	GPIO3<1:0>	RW	00	**General Purpose I/O 3** 00 = high impedance 01 = Mono/Stereo indicator (ST). GPIO3 = High for Stereo GPIO3 = Low for Mono 10 = low 11 = high
3:2	GPIO2<1:0>	RW	00	**General purpose I/O 2** 00 = high impedance 01 = STC interrupt/RDS group synchronization interrupt/ 10 = low 11 = high

				Setting STCIEN=1 will generate a high level interrupt on GPIO2 when the STC bit is set. Setting RDSIEN=1 will generate a high level interrupt on GPIO2 when RDS is synchronized.
1:0	GPIO1<1:0>	RW	00	**General purpose I/O 1** 00 = high impedance 01 = reserved 10 = low 11 = high

5.9 Status Register A (Reg 0x12)

Bit	Symbol	Access	Default	Functional Description
15	XTAL_OK	R	0	**Crystal ready indictor** 0 = not ready 1= crystal is ok
14	STC	RW	0	**Seek/Tune Complete** 0 = Not Complete 1 = Complete The status can be cleared manually
13	SF/BL	RW	0	**Seek Fail or Band Limit** 0 = Seek successful 1 = Seek failure
12	Reserved	R	0	
11	PLL_LOCK	R	1	**System PLL ready indicator** 0 = not ready 1 = System PLL ready
10	LO_LOCK	R	1	**LO Synthesizer ready indicator** 0 = not ready 1 = ready
9:8	ST<1:0>	R	00	**Stereo indicator** 11 = Stereo Other= Mono
7:3	RSSI<4:0>	R	00000	**RSSI value indicator** RSSI indication range is from -100dBm to -7dBm with 3dB resolution, where 00000 means minimum level and 11111 means maximum level.
2:0	Reserved	R	000	**Reserved**

5.10 Status Register B (Reg 0x13)

Bit	Symbol	Access	Default	Functional Description
15:10	Reserved	R	000000	Reserved
9:0	READCHAN<9:0>	R	0	**The current Channel** READCHAN<9:0> provides the

				current channel during seek or after a seek or tune operation is completed

5.11 . Status Register C (Reg 0x14)

Bit	Symbol	Access	Default	Functional Description
15:6	Reserved	R	0000000000	Reserved
5:0	AFC_DELTAF_5767<5:0>	R	000000	Frequency difference between CHAN and received signal, calculated by AFC block in two's complement format. Range is -31 to +31. Unit is KHz. This register is valid when STC=1

5.12 Status Register D (Reg 0x15)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	R	00000000	Reserved
7:0	AFC_DELTAF<7:0>	R	00000000	Frequency difference between CHAN and received signal, calculated by AFC block in two's complement format. Range is -127 to +127. Unit is KHz. This register is valid when STC=1

5.13 Antenna Register (Reg 0x1D)

Bit	Symbol	Access	Default	Functional Description
15:0	Reserved			

5.14 SNR Register (Reg 0x1F)

Bit	Symbol	Access	Default	Functional Description
15:8	SNRTH<7:0>	RW	0x00	SNR threshold for traditional seek mode
7:0	SNR<7:0>	R	0x00	SNR value of current channel 0x00 = Worst …… 0xFF = Best

5.15 SEEKTH Register (Reg 0x20)

Bit	Symbol	Access	Default	Functional Description
15:8	ADV_SEEKTH_HIGH	RW	0x14	High threshold for advanced seek mode
7:0	ADV_SEEKTH_LOW	RW	0x19	Low threshold for advanced seek mode

5.16 Softmute Register (Reg 0x21)

Bit	Symbol	Access	Default	Functional Description

15:7	Reserved	RW	000100000	Reserved
6	SMMD	RW	0	Softmute Mode Selection 0 = RSSI 1 = SNR
5:4	Reserved	RW	01	Reserved
3	SMTH<2>	RW	0	Softmute threshold MSB, together with SMTH<1:0> in Reg0x04 000 = Lowest 001 = … 111 = Highest
2:0	Reserved	RW	010	Reserved

5.17 Clock Register (Reg 0x23)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	000	Reserved
12	RCLK_EN	RW	0	Reference Clock Enable 0 = crystal 1 = reference clock
11:8	REF_CLK<3:0>	RW	0000	**Reference clock selection** 0000 = 32.768KHz 0001 = 6.5MHz 0010 = 7.6MHz 0011 = 12MHz 0100 = 13MHz 0101 = 15.2MHz 0110 = 19.2MHz 0111 = 24MHz 1000 = 26MHz
7:5	Reserved	RW	000	**Reserved**
4	LRSWAP	RW	0	**Swap Left and Right audio channels** 0 = don't swap 1 = swap
3:0	Reserved	RW	0	**Reserved**

6 Application circuit

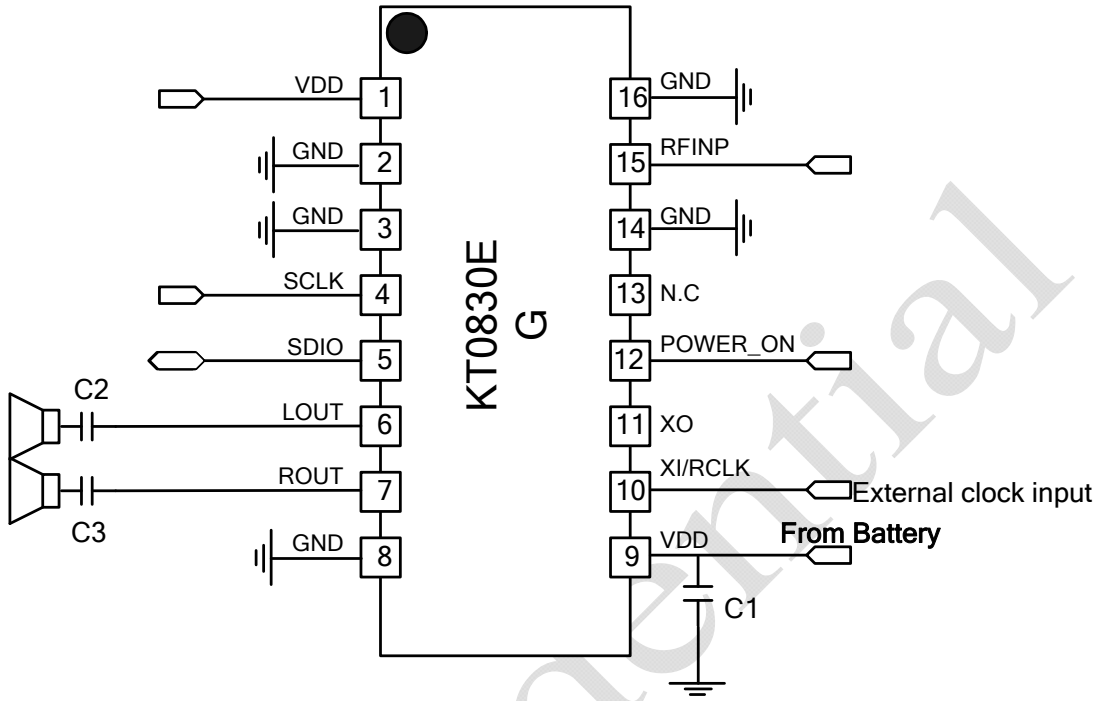


Figure 5: Typical application circuit (Reference Clock)

Note：The decoupling C1 should be close to Pin 8 and Pin 9。

Table 7: Bill of Material

Components	Value/Description	Suppliers
C1	Supply decoupling capacitor, 0.1uF	
C2,C3	AC decoupling capacitor, 100uF	

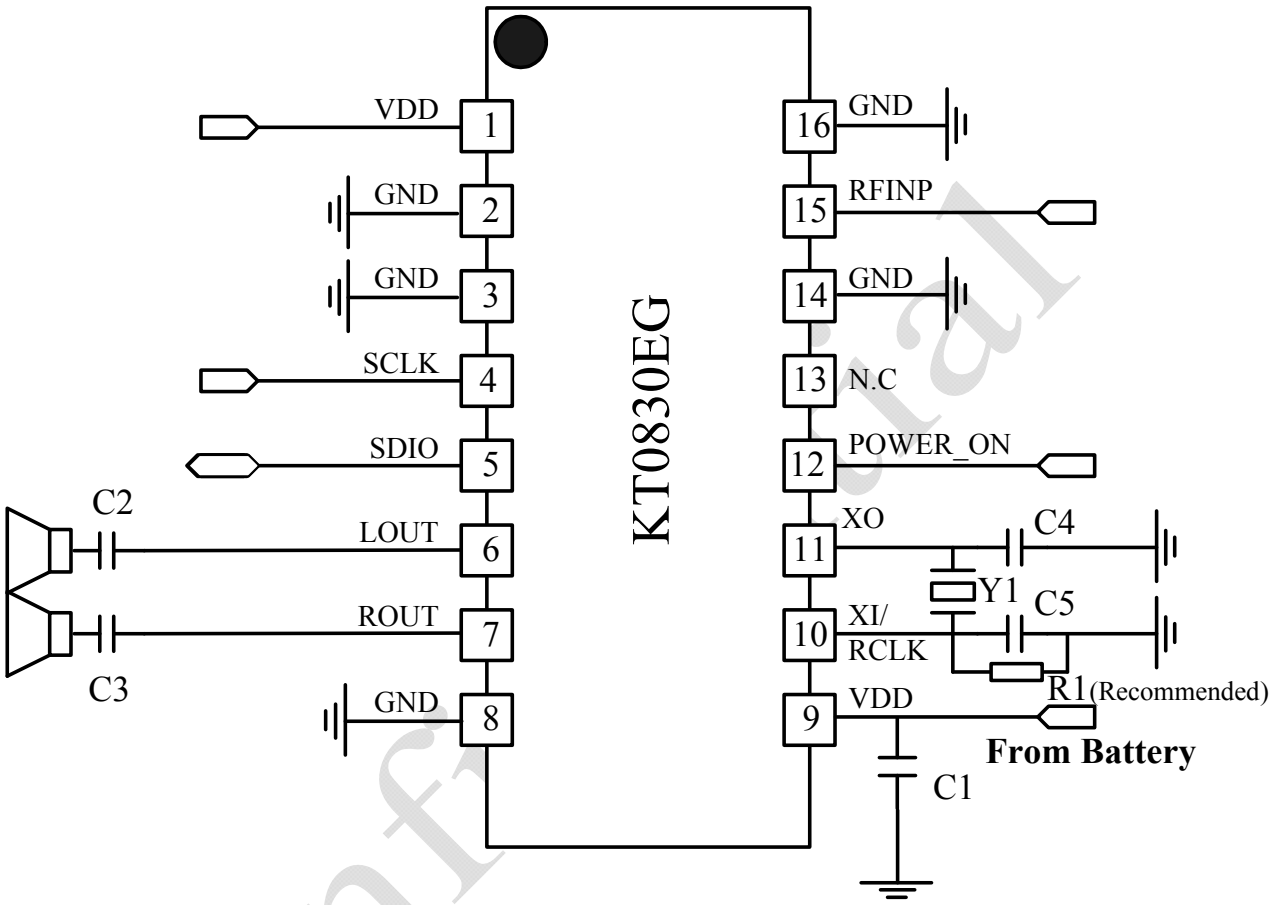


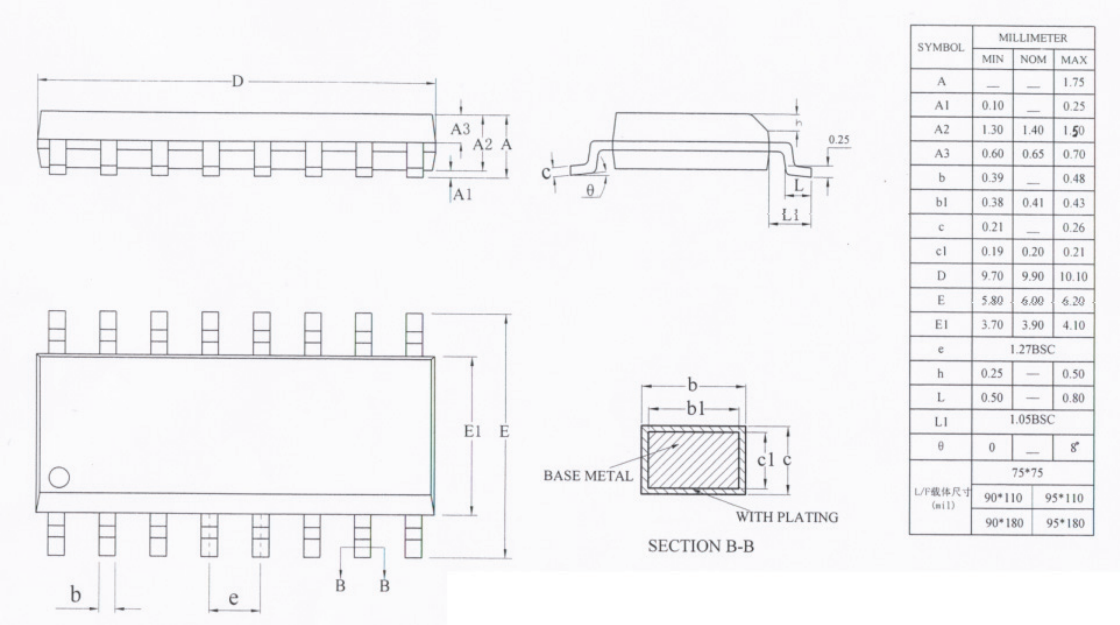
Figure 6: Typical application circuit (Crystal)

Note：The decoupling C1 should be close to Pin 8 and Pin 9。

Table 8: Bill of Material

Components	Value/Description	Suppliers
C1	Supply decoupling capacitor, 0.1uF	
C2,C3	AC decoupling capacitor, 100uF	
C4,C5	Capacitor, 24pF	
Y1	Crystal, 32.768KHz	
R1	Resistor, 10Mohm	

7 Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	75*75		
	90*110		95*110
	90*180		95*180

8 Order Information

Part Number	Description	Package	MOQ
KT0830EG	2nd gen Single-chip stereo FM receiver	SOP-16	5000

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9 Revision History

V1.0 Official Release
V1.1 Pin 14 and Pin 2
V1.2 Added Figure 7 and Table 9