

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

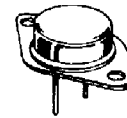
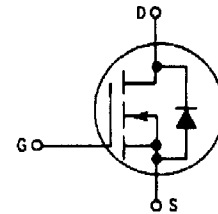
This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM25N10

TMOS POWER FET
25 AMPERES
 $R_{DS(on)} = 0.075 \text{ OHM}$
100 VOLTS



TO-204AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 105	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS — ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

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ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}$, $I_D = 12.5 \text{ Adc}$)	$R_{DS(on)}$	—	0.075	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 25 \text{ Adc}$) ($I_D = 12.5 \text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— —	2.25 1.8	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ V}$, $I_D = 12.5 \text{ A}$)	g_{FS}	5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$) See Figure 11	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DD} = 25 \text{ V}$, $I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms}$) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10 \text{ V}$) See Figure 12	Q_g	29 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	23 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	($I_S = \text{Rated } I_D$ $V_{GS} = 0$)	V_{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	