SIEMENS

SAB 179X Floppy Disk Formatter/ Controller Family

FEATURES	SAB 1791	SAB 1793	SAB 1795	SAB 1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

- Two VFO Control Signals -RG & VFOE
- Soft Sector Format Compatibility
- Automatic Track Seek with Verification
- Accomodates Single and Double Density Formats
  IBM 3740 Single Density (FM)
  IBM System 34 Double Density (MFM)
- Read Mode
  Single/Multiple Sector Read with Automatic Search or Entire Track Read
  Selectable 128 Byte or Variable length Sector
- Write Mode
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- System Compatibility
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-Chip Track and Sector Registers/Comprehensive Status Information
- Programmable Controls
  Selectable Track to Track Stepping Time
  Side Select Compare
- Write Precompensation
- Window Extension
- Incorprorates Encoding/Decoding and Address Mark Circuitry
- For 8" and 5¼"
  Floppy Disks
- Compatible with Industry Standard 179X

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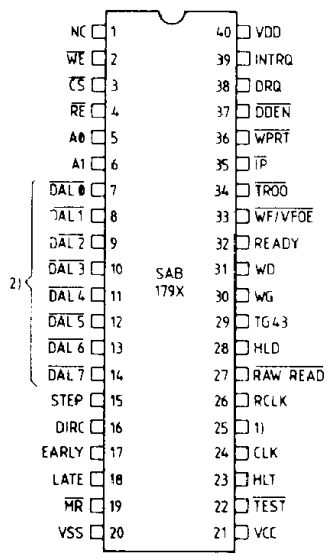
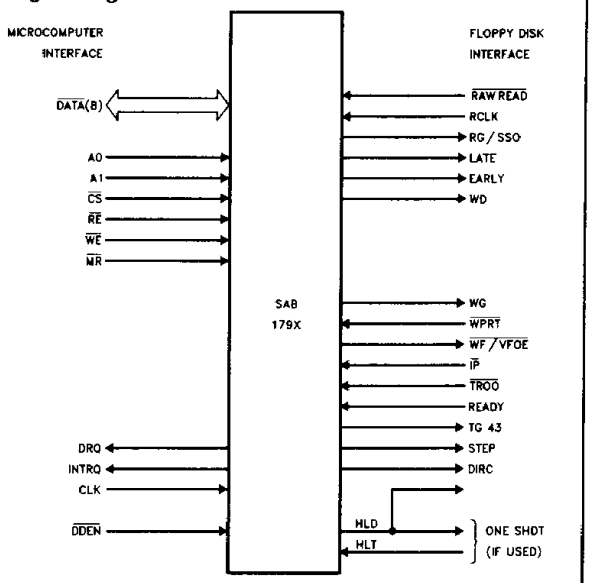
Pin Connections



1) SAB 1791/1793 = RG, SAB 1795/7 = SSO
2) SAB 1793/SAB 1797 = True Bus

Logic Diagram



SAB 179X is a floppy disk controller family of N-channel MOS LSI components designed to interface with SAB 8080/8085/8086/8051 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems.

October 1984

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
NC	1	–	NO CONNECTION – Pin 1 is internally connected to a back bias generator and must be left open by the user.
$\overline{MR}$	19	I	$\overline{MASTER\ RESET}$ – A logic low (50μs min.) on this input resets the device and loads HEX Ø3 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX Ø1 is loaded into sector register.
$\overline{WE}$	2	I	$\overline{WRITE\ ENABLE}$ – A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
$\overline{CS}$	3	I	$\overline{CHIP\ SELECT}$ - A logic low on this input selects the chip and enables computer communication with the device.
$\overline{RE}$	4	I	$\overline{READ\ ENABLE}$ – A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
A Ø, A 1	5,6	I	REGISTER SELECT LINES – These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A 1 A Ø $\overline{RE}$ $\overline{WE}$ Ø Ø Ø Status Reg Command Reg Ø Ø 1 Track Reg Track Reg Ø 1 Ø Sector Reg Sector Reg Ø 1 1 Data Reg Data Reg
$\overline{DAL Ø}$ to $\overline{DAL7}$	7 to 14	I/O	$\overline{DATA\ ACCESS\ LINES}$ – Eight bit inverted (SAB 1791/5) or true (SAB 1793/7) bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by $\overline{RE}$. Drive capability is 1 TTL Load
CLK	24	I	CLOCK – This input requires a free-running square wave clock for internal timing reference. 2 MHz ± 1% with 50% duty cycle. 1 MHz ± 1% for mini-floppies.
DRQ	38	O	DATA REQUEST – This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5V.
INTRQ	39	O	INTERRUPT REQUEST – This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5V.
STEP	15	O	STEP – The step output contains a pulse for each step.
DIRC	16	O	DIRECTION – Direction Output is active high when stepping in, active low when stepping out.
EARLY	17	O	EARLY – Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
LATE	18	O	LATE – Indicates that the write data pulse occuring while Late is active (high) should be shifted late for write precompensation.

Symbol	Number	Input (I) Output (O)	Function
$\overline{\text{TEST}}$	22	I	$\overline{\text{TEST}}$ – This input is used for testing purposes only and should be tied to + 5V or left open by the user unless interfacing to voice coil actuated motors.
HLT	23	I	HEAD LOAD TIMING – When a logic high is found on the HLT input the head is assumed to be engaged.
RG	25	O	READ GATE (SAB 1791/3) – A high level on this output indicates to the data separator circuitry that 2 bytes of zeros in single density, or 4 bytes of either zeros or ones in double density have been encountered, and is used for synchronization.
SSO	25	O	SIDE SELECT OUTPUT (SAB 1795/1797) – The logic level of the Side Select Output is directly controlled by the ‚S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = Ø, SSO is set to a logic Ø. The SSO is compared with side information in the sector ID field. If they do not compare, status bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic Ø upon a MASTER RESET condition.
RCLK	26	I	READ CLOCK – A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i. e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
$\overline{\text{RAW READ}}$	27	I	$\overline{\text{RAW READ}}$ – The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
HLD	28	O	HEAD LOAD – The HLD output controls the loading of the Read-Write head against the media.
TG43	29	O	TRACK GREATER THAN 43 – This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
WG	30	O	WRITE GATE – This output is made valid before writing is to be performed on the diskette.
WD	31	O	WRITE DATA – A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
READY	32	I	READY – This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.

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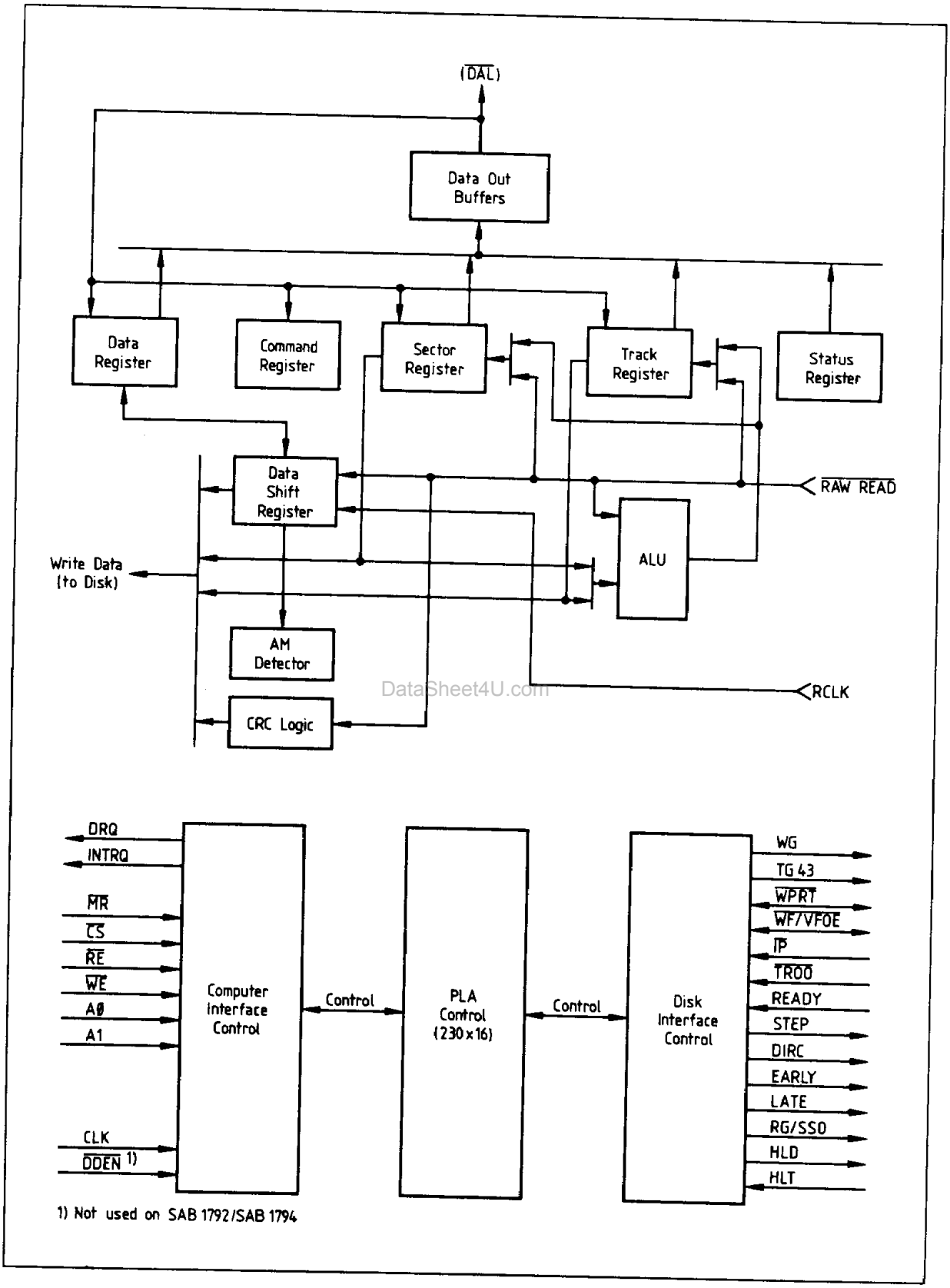
Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{WF/VFOE}$	33	I/O	$\overline{WRITE\ FAULT\ VFO\ ENABLE}$ – This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = Ø, any write command will immediately be terminated. When WG = Ø, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the SAB 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the SAB1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100 kOhm pull-up resistor.
TRØØ	34	I	$\overline{TRACK\ ØØ}$ – This input informs the SAB 179X that the Read/Write head is positioned over Track ØØ.
IP	35	I	$\overline{INDEX\ PULSE}$ – This input informs the SAB 179X when the index hole is encountered on the diskette
WPRT	36	I	$\overline{WRITE\ PROTECT}$ – This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
$\overline{DDEN}$	37	I	$\overline{DOUBLE\ DENSITY}$ – This pin selects either single or double density operation. When $\overline{DDEN}$ = Ø, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
VCC	21	–	POWER SUPPLY (+5 V).
VDD	40	–	POWER SUPPLY (+12 V).
VSS	20	–	GROUND (0 V)



1) Not used on SAB 1792/SAB 1794

General Description

The SAB 179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The SAB 179X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.
The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The SAB 179X is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The SAB 1793 is identical to the SAB 1791 except the DAL lines are TRUE for systems that utilize true data busses.
The SAB 1795/7 has a side select output for controlling double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on previous page. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register – This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operation information is transferred in parallel from the Data Register to the Data Shift Register.
When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track Ø). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed.This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control – All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.
The SAB 179X has two different modes of operation according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}} = Ø$ double density (MFM) is assumed. When $\overline{\text{DDEN}} = 1$, single density (FM) is assumed.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the SAB 179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and AØ, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-AØ	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
ØØ	Status Register	Command Register
Ø1	Track Register	Track Register
1Ø	Sector Register	Sector Register
11	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the SAB 179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd.[1] FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit Ø)	12 µs	6 µs
Write to Command Reg.	Read Status Bits 1-7	28 µs	14 µs
Write Any Register	Read From Diff. Register	Ø	Ø

[1] Times double for CLK = 1MHz (Minifloppies)

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Floppy Disk Interface

The SAB 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

Head Positioning

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and Ø of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock.If $\overline{TEST}$ = Ø, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.
The rates can be applied to a Step-Direction Motor through the device interface.

Step – A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.
Direction (DIRC) – The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The SAB 179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

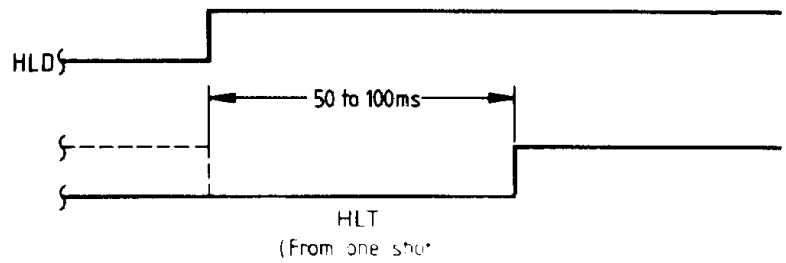
Stepping Rates

CLK $\overline{DDEN}$ R1 RØ	2 MHz Ø $\overline{TEST}$=1	2 MHz 1 $\overline{TEST}$=1	1 MHz Ø $\overline{TEST}$=1	1 MHz 1 $\overline{TEST}$=1	2 MHz x $\overline{TEST}$=Ø	1 MHz x $\overline{TEST}$=Ø
R1 Ø Ø Ø 1 1 Ø 1 1	3 ms 6 ms 10 ms 15 ms	3 ms 6 ms 10 ms 15 ms	6 ms 12 ms 20 ms 30 ms	6 ms 12 ms 20 ms 30 ms	184 μs 190 μs 198 μs 208 μs	368 μs 380 μs 396 μs 416 μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = Ø and V = Ø); or if the SAB 179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the SAB 179X which is used for the head engage time. When HLT = 1, the SAB 179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the SAB 179X.

Head Load Timing



When both HLD and HLT are true, the SAB 179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.
In summary for the Type I commands: if h = Ø and V = Ø, HLD is reset. If h = 1 and V = Ø, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = Ø and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the SAB 179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 179X then waits for HLT to occur.
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

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General Disk Read Operations

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "Ø." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*)

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
ØØ	128
Ø1	256
Ø2	512
Ø3	1024

*) SAB 1795/97 may vary – see command summary.

The number of sectors per track as far as the SAB 179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the SAB 179X is concerned is from Ø to 255 tracks.
For read operations in 8" double density the SAB 179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase locked loop, one shots, or counter techniques. In addition a Read Gate Signal is provided as an output (Pin 25) on SAB 1791 93 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The SAB 179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the SAB 179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "ØØ" or "FF" are detected. The SAB 179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.
During read operations (WG = Ø), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will got active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The SAB 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, this pin may be left open, as it has an internal pull-up resistor.

General Disk Write Operations

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 179X before the Write Gate signal can be activated.
Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{Write\ Fault}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the SAB 179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the SAB 179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = Ø) Write Data provides the unique address marks in both formats.
Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the SAB 179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Ready

Whenever a Read or Write command (Type II or III) is received the SAB 179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

Command Description

The SAB 179X accepts eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit Ø). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types.
Commands and types are summarized on next page.

Status Register

Upon receipt of any command, except, the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

(Bits)							
7	6	5	4	3	2	1	Ø
S7	S6	S5	S4	S3	S2	S1	SØ

Status varies according to the type of command executed.

Command Summary

Commands for SAB 1791, SAB 1793										Commands for SAB 1795, SAB 1797								
		Bits								Bits								
Type	Command	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a_0	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0	1	1	0	1	I_3	I_2	I_1	I_0

Flag Summary

Command Type	Bit No(s)	Description
I	0, 1	r_1 r_0 = Stepping Motor Rate
I	2	V = Track Number Verify Flag V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 ms Delay E = 0, No 15 ms delay E = 1, 15 ms delay
II	3	S = Side Compare Flag S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag L = 1 (implicit) for SAB 1791/3

	LSB's Sector Length in ID Field			
	00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

II	4	m = Multiple Record Flag m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_1 = 0 Terminate With No Interrupt (INTRQ)

Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	Ø	Ø	Ø	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	Ø	RECORD TYPE	Ø	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	Ø	RNF	Ø
S3	CRC ERROR	CRC ERROR	CRC ERROR	Ø	CRC ERROR	Ø
S2	TRACK Ø	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
SØ	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to Ø when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK ØØ	When set, indicates Read/Write head is positioned to Track Ø. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
SØ	BUSY	When set command is in progress. When reset no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ored" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. Ø = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
SØ	BUSY	When set, command is under execution. When reset, no command is under execution.

5

Formatting the Disk

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bis is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the SAB 179X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F 7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

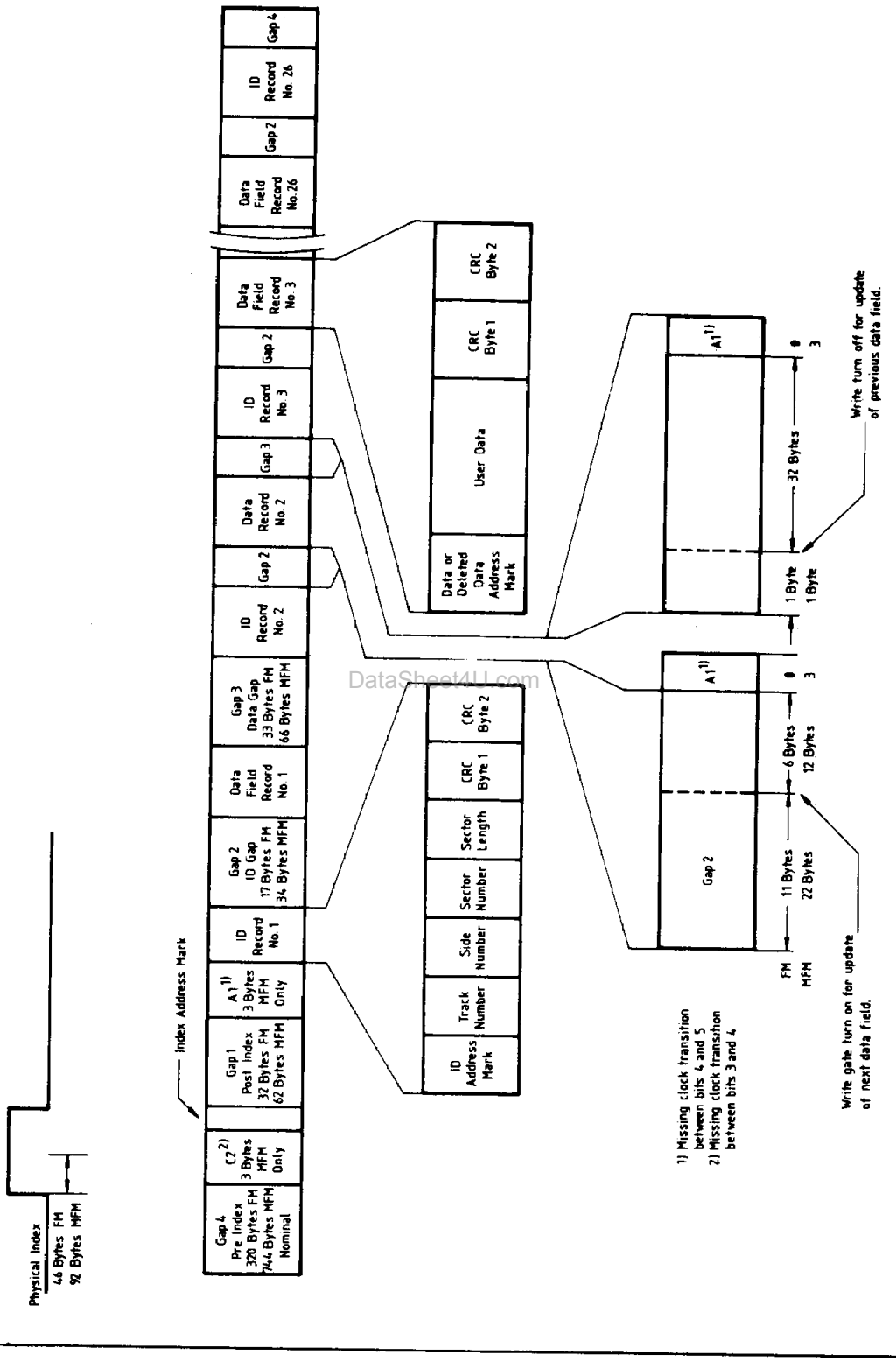
IBM 3740 Format – 128 Bytes/Sector (8")

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or ØØ)[3]
6	ØØ
1	FC (Index Mark)
26	FF (or ØØ)
[1] 6	ØØ
1	FE (ID Address Mark)
1	Track Number
1	Side Number (ØØ or Ø1)
1	Sector Number (1 thru 1A)
1	ØØ
1	F7 (2 CRC's written)
11	FF (or ØØ)
6	ØØ
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or ØØ)
247[2]	FF (or ØØ)

[1] Write bracketed field 26 times
[2] Continue writing until SAB 179X interrupts out. Approx. 247 bytes.
[3] Optional 'ØØ' on SAB 1795/7 only.

IBM Track Format



IBM System 34 Format 256 Bytes/Sector (8")

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex value of Byte written
80	4E
12	00
3	F6 (writes C2)
1	FC (Index Mark)
[1] 50	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (Data Adress Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598[2]	4E

[1] Write bracketed field 26 times
[2] Continue writing until SAB179X interrupts out. Approx. 598 bytes.

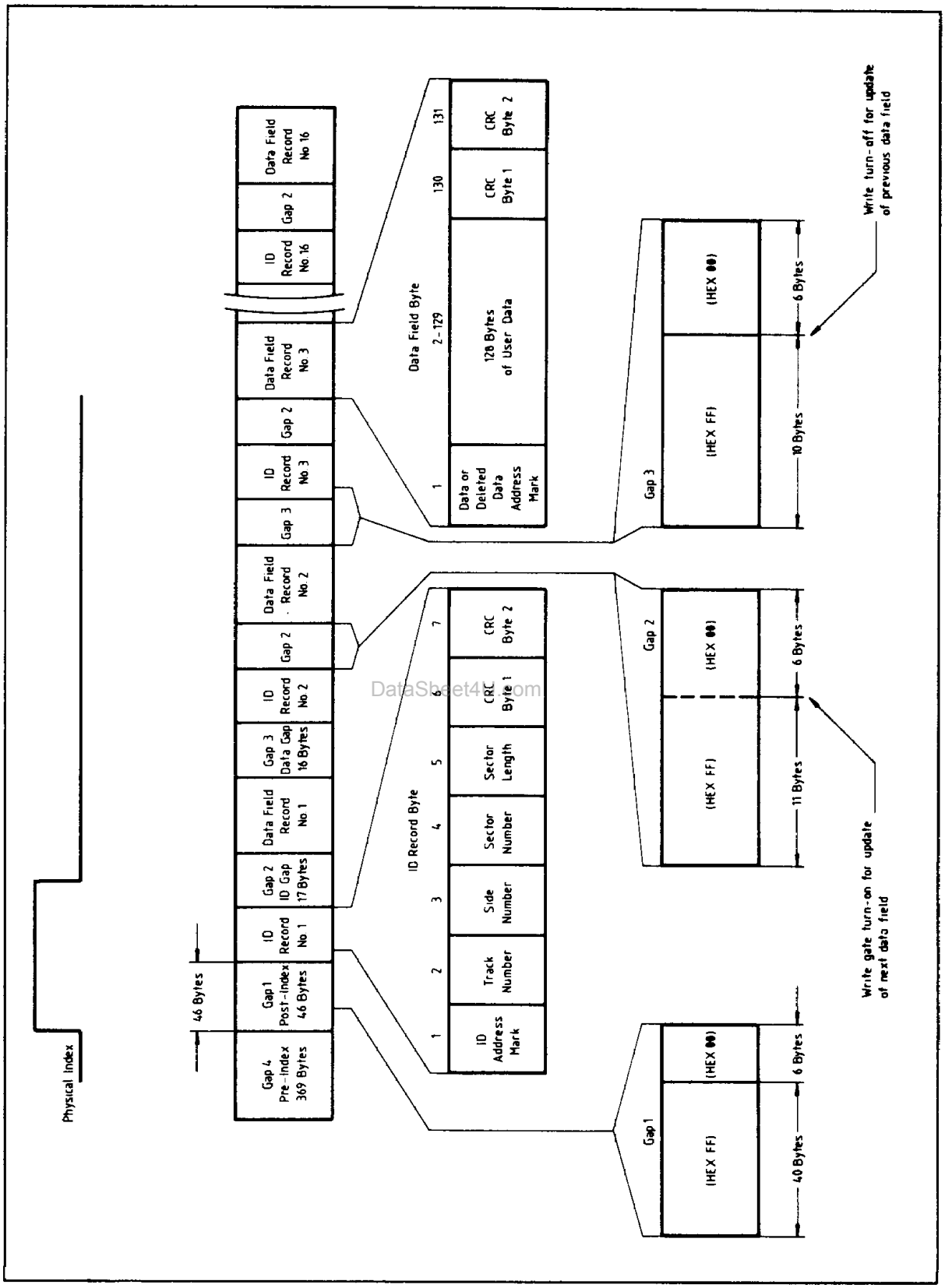
Recommended — 128 Bytes/Sector (Mini-Diskette)

Shown below is the Recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
[1] 40	FF (or 00)[3]
6	00
1	FE (ID Address Mark)
1	Track Numer
1	Side Number (00 or 01)
1	Sector Number (1 through 1A)
1	00 (Sector length)
1	F7 (2 CRC's written)
11	FF (or 00)[3]
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)[3]
369[2]	FF (or 00)[3]

[1] Write bracketed field 16 times
[2] Continue writing until SAB 179X interrupts out. Approx 369 bytes.
[3] Optional '00' on SAB 1795/7 only.

Recommended Single Density Format (Mini-Diskette)



256 Bytes/Sector (Mini-Diskette)

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex value of Byte written
60	4E
[1] 12	ØØ
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (Ø through 4C)
1	Side Number (Ø or 1)
1	Sector Number (1 through 1A)
1	Ø1 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	ØØ
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
24	4E
718[2]	4E

[1] Write bracketed field 26 times
[2] Continue writing until SAB 179X interrupts out. Approx. 718 bytes.

Non-standards Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the SAB 179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 179X operation, however PPL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
[3]	6 bytes ØØ	12 bytes ØØ
		3 bytes A1
Gap III	10 bytes FF	24 bytes 4E
[4]	4 bytes ØØ	8 bytes ØØ
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

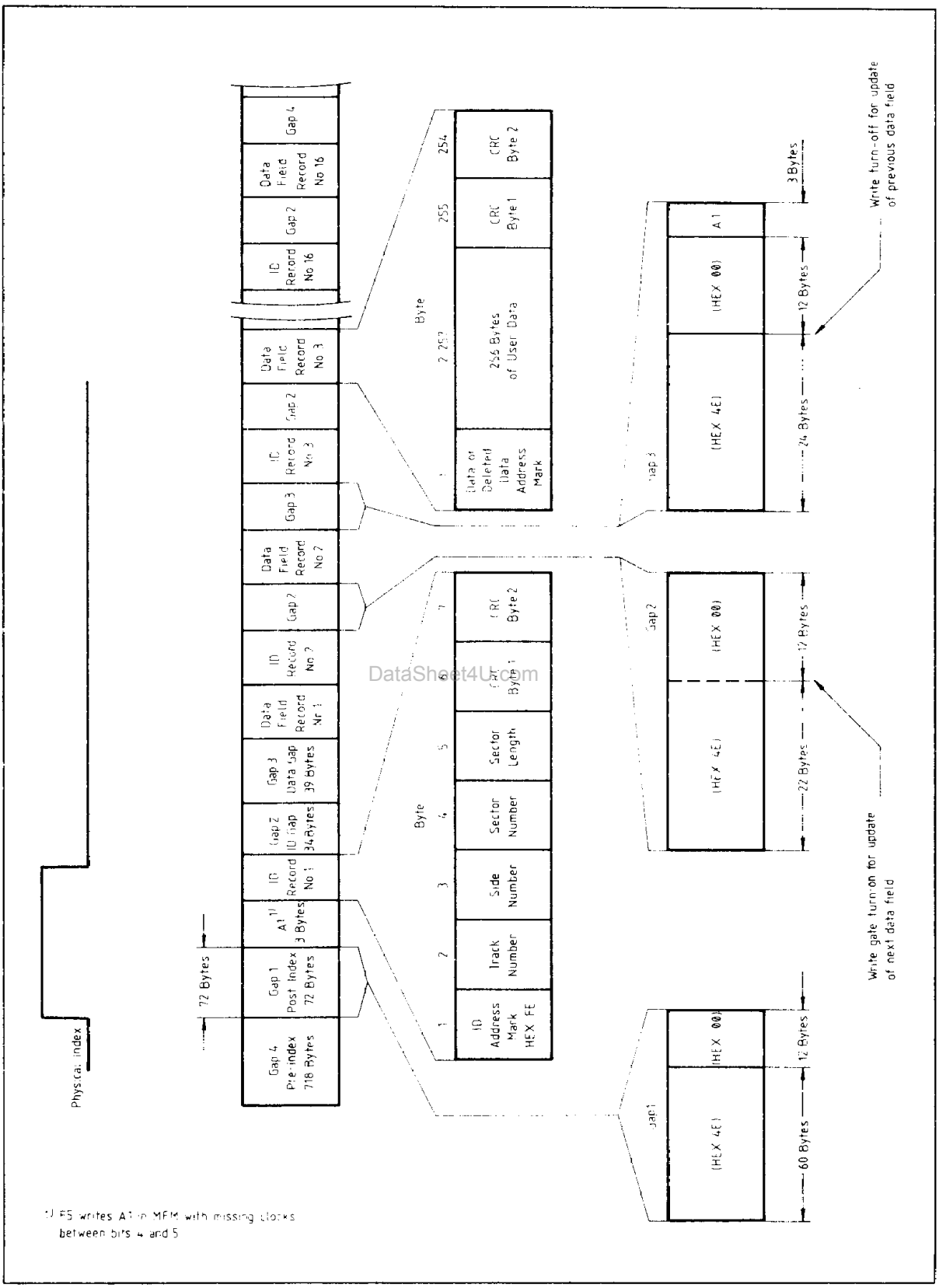
[3] Byte counts must be exact.
[4] Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.

Control Bytes for Initialization

Data Pattern in DR (Hex.)	SAB 179X Interpretation in FM (DDEN = 1)	SAB 179X Interpretation in MFM (DDEN = Ø)
ØØ through F4	Write ØØ through F4 with CLK = FF	Write ØØ through F4, in MFM
F5	Not Allowed	Write A1[1] in MFM, Preset CRC
F6	Not Allowed	Write C2[2] in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 through FB	Write F8 through FB, Clk = C7, Preset CRC	Write F8 through FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Present CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

[1] Missing clock transition between bits 4 and 5
[2] Missing clock transition between bits 3 and 4

Recommended Double Density Format (Mini-Diskette)



Absolute maximum ratings[1)]

Operating Temperature	0 to 70°C
Storage Temperature	−65 to +150°C
VDD with Respect to Vss (Ground)	+15 to −0.3 V
Max. Voltage to any Input with Respect to VSS	+15 to −0.3 V

D. C. Characteristics

TA = 0 to 70° C; VDD = +12 V ± 5%; VCC = +5V ± 5%; VSS = OV

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
IIL	Input Leakage	–	–	10	μA	VIN = VDD
IOL	Output Leakage					VOUT = VDD
VIH	Input High Voltage	2.6	–	–	V	–
VIL	Input Low Voltage	–		0.8		
VOH	Output High Voltage	2.8		–		IO = −100 μA
VOL	Output Low Voltage	–		0.45		IO = 1.6mA
ICC	Power Supply Current		35	60	mA	–
IDD	Power Supply Current		10	15		
PD	Power Dissipation		–	0.6	W	

Capacitance[3)]

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	15	pF	Unmeasured pins returned to GND
COUT	Output Capacitance			

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2)] Leakage conditions are for input pins without internal pull-up resistors.

[3)] This parameter is periodically sampled and not 100% tested.

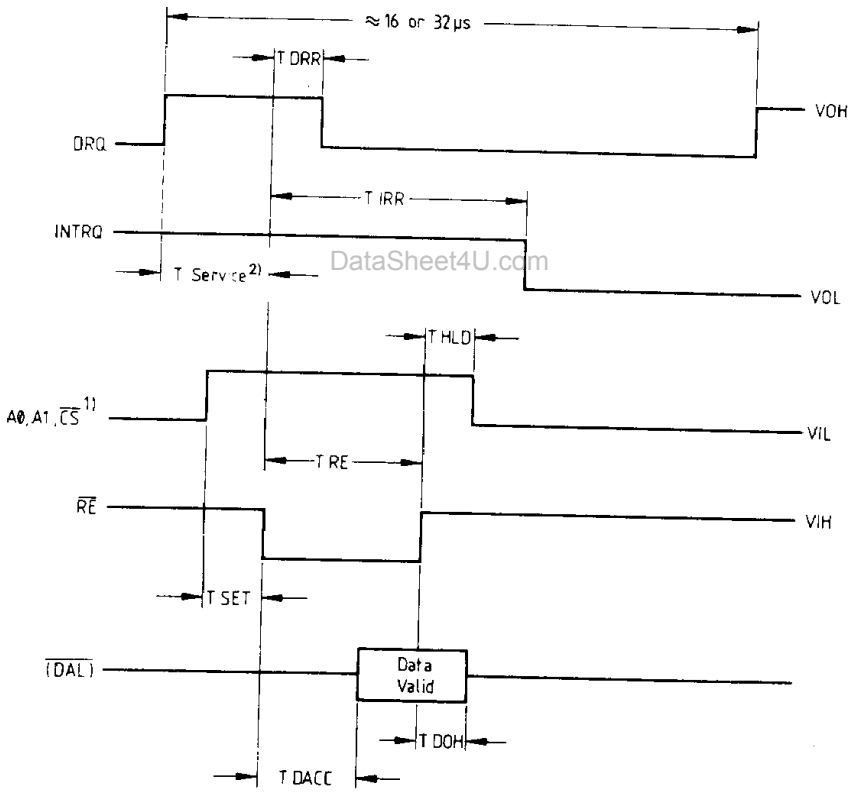
A.C. Characteristics

TA = 0 to 70° C, VDD = +12 V ± 5%; VSS = 0V, VCC = +5V ± 5%

All timing readings at VOL = 0.8 V and VOH = 2.0 V.

Read Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{RE}$	50	–	–	ns	–
THLD	Hold ADDR & CS from $\overline{RE}$	10				
TRE	$\overline{RE}$ Pulse Width	400				CL = 50pf
TDRR	DRQ Reset from $\overline{RE}$	–	400	500		–
TIRR	INTRQ Reset from $\overline{RE}$		500	3000		
TDACC	Data Access from $\overline{RE}$		–	350		CL = 50pf
TDOH	Data Hold from $\overline{RE}$	50		150		



DRQ rising edge: Indicates that the data register has assembled data.
DRQ falling edge: Indicates that the data register was read.
INTRQ rising edge: Occurs at end of command.
INTRQ falling edge: Indicates that the status register was read.

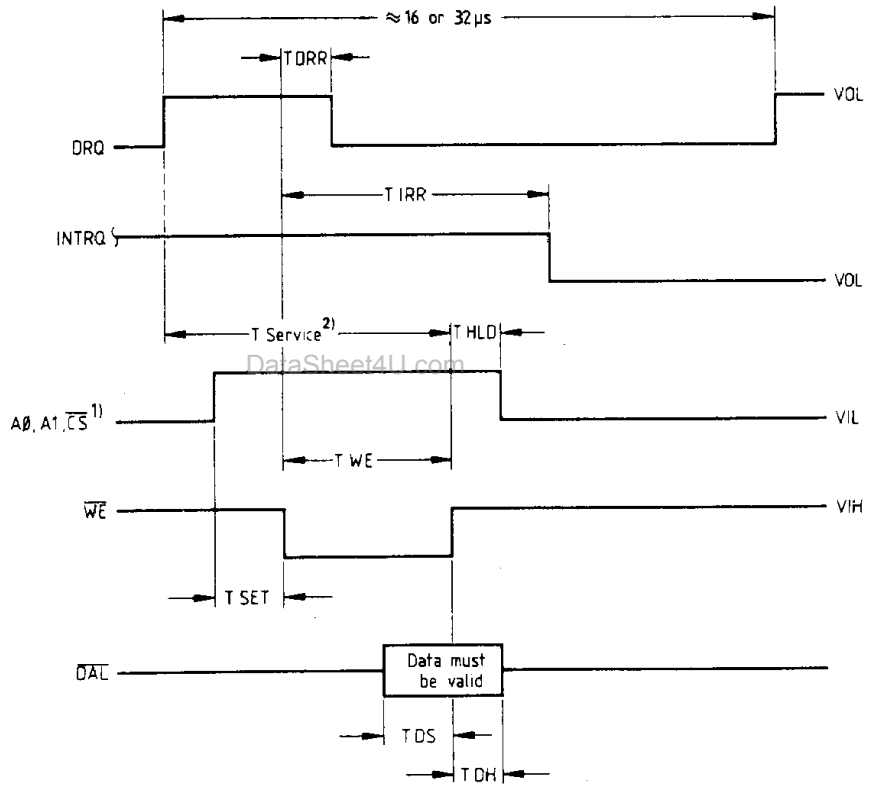
1) $\overline{CS}$ may be permanently tied LOW if desired.

2) T Service (worst case)
- FM = 27.5 µs
- MFM = 13.5 µs

3) Times double when CLK = 1MHz

Write Enable Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{WE}$	50	–	–	ns	–
THLD	Hold ADDR & CS from $\overline{WE}$	10				
TWE	$\overline{WE}$ Pulse Width	350				
TDRR	DRQ Reset from $\overline{WE}$	–	400	500		
TIRR	INTRQ Reset from $\overline{WE}$		500	3000		
TDS	Data Setup to $\overline{WE}$	250	–	–		
TDH	Data Hold from $\overline{WE}$	70				



DRQ rising edge: Indicates that the data register is empty.
DRQ falling edge: Indicates that the data register is loaded.
INTRQ rising edge: Indicate the end of a command.
INTRQ falling edge: Indicates that the command register is written to.

[1] CS may be permanently tied LOW if desired. When writing Data into Sector Track or Data Register User cannot read this Register until at least 4µs in MFM after the rising edge of WE when writing into the command Register Status is not valid until some 28µs in FM, 14 µs in MFM later.

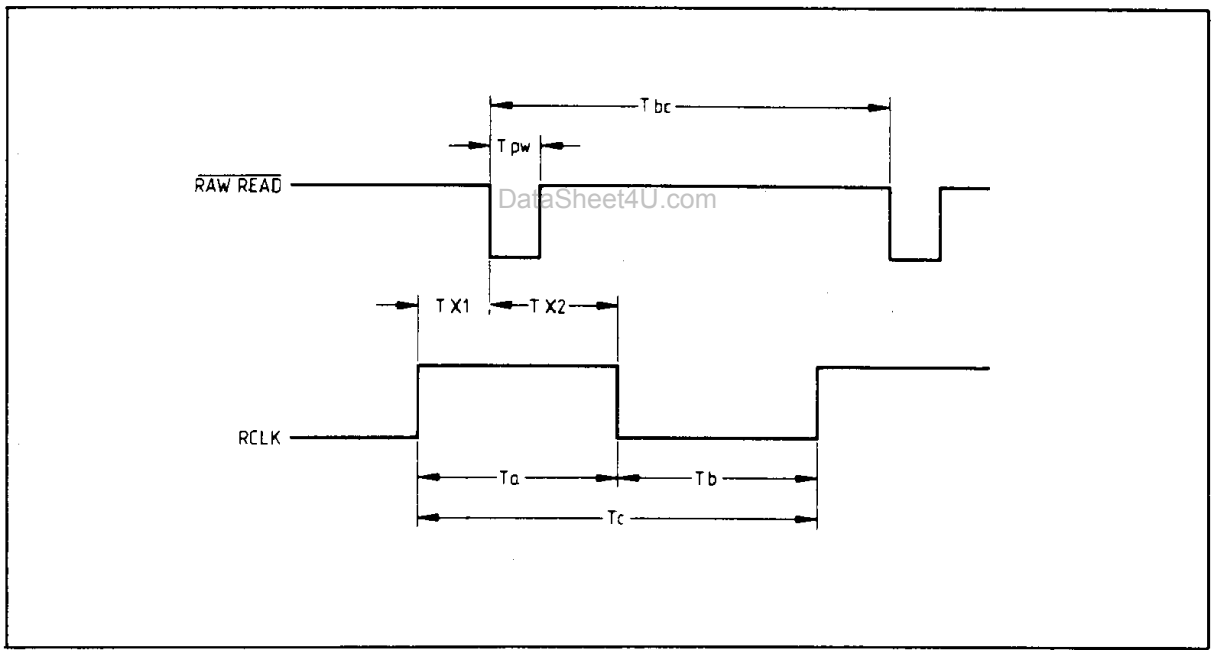
[2] T Service (worst case); FM = 23.5 µs; MFM = 11.5 µs

[3] Times double when CLK=1MHz

Input Data Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
Tpw	$\overline{\text{RAW READ}}$ Pulse Width	100	200	–	ns	1)
Tbc	$\overline{\text{RAW READ}}$ Cycle Time[2]	1500	2000			1800 ns @ 70°C
Tc	RCLK Cycle Time[3]					
Tx1	RCLK hold to $\overline{\text{RAW READ}}$	40	–			1)
Tx2	$\overline{\text{RAW READ}}$ hold to RCLK					1)

[1] Pulse width on RAW READ (Pin 27) is normally 100 – 300ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300ns for MFM at CLK = 2MHz and 600ns for FM at 2MHz. Times double for 1MHz.
[2] tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
[3] RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).

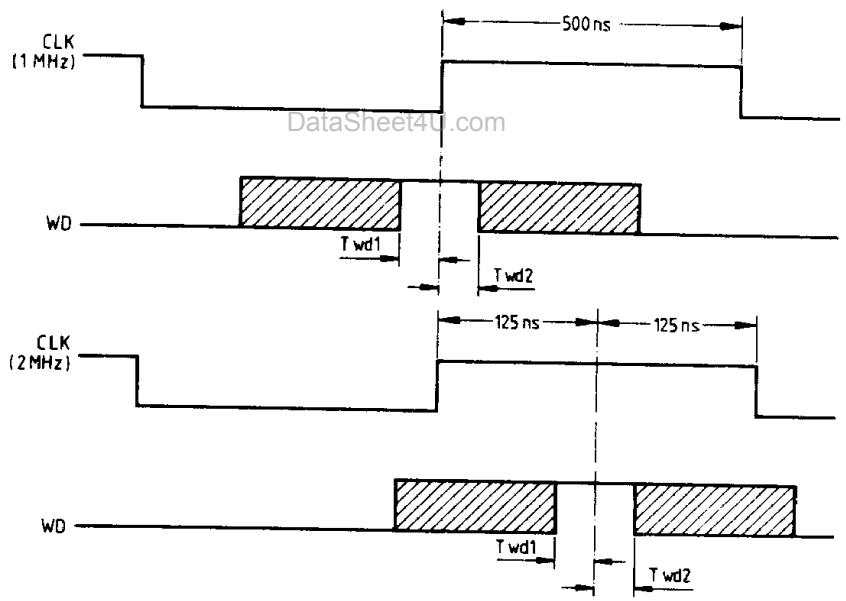


				Nominal		
Diskette	Mode	$\overline{\text{DDEN}}$	CLK	Ta	Tb	Tc
8"	MFM	Ø	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2 μs	4 μs
5"	MFM	Ø	1 MHz	2 μs	2 μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

A PPL Data Separator is recommended for 8" MFM

Write Data Timing (All Times Double when CLK = 1 MHz)

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
Twp	Write Data Pulse Width	450 150	500 200	550 250	ns	FM MFM
Twg	Write Gate to Write Data	–	2 1	–	µs	FM MFM
Tbc	Write data cycle Time		2,3 or 4			± CLK Error
Ts	Early (Late) to Write Data	125			ns	MFM
Th	Early (Late) from Write Data					
Twf	Write Gate off from WD	–	2 1		µs	FM MFM
Twd1	WD Valid to CLK	100 50	–		ns	CLK = 1MHz CLK = 2MHz
Twd2	WD Valid after CLK	100 30				CLK = 1MHz CLK = 2MHz

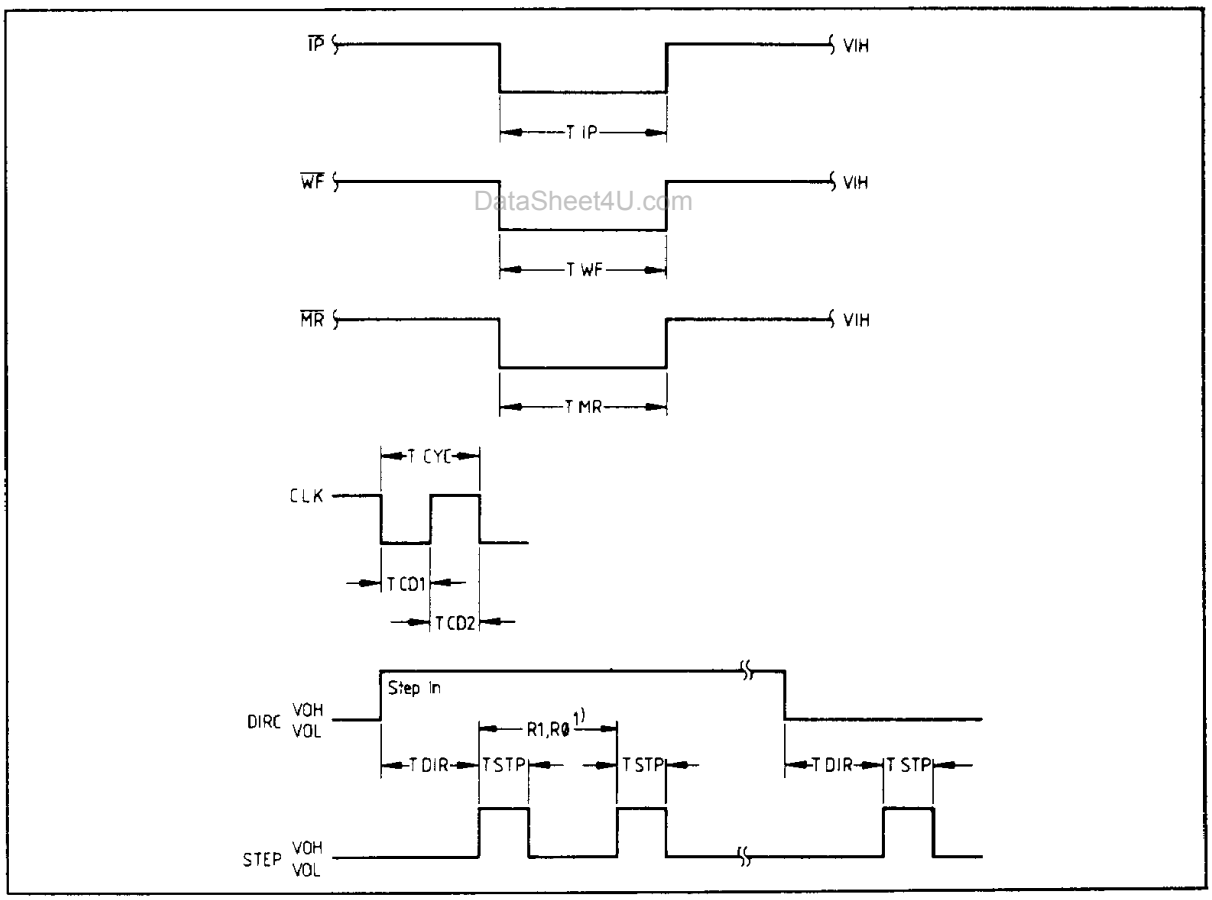


Write Data/Clock Relationship ($\overline{DDEN}$ = Ø)

WD must have rising edge in first shaded area and trailing edge in second shaded area

Miscellaneous Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TCD1	Clock Duty (LOW)	230		20000	ns	2)
TCD2	Clock Duty (HIGH)	200				
TSTP	Step Pulse Output	2 or 4	–	–	µs	± CLK Error
TDIR	Dir Setup to Step	–	12			
TMR	Master Reset Pulse Width	50				
TIP	Index Pulse Width	10	–			2)
TWF	Write Fault Pulse Width	20				



1) From step rate table.
2) Times double when CLK=1MHz

Ordering Information

Type	Description
SAB 1791-02-P	Floppy-Disk-Controller (P-DIP 40); Inverted Data Bus, single-sided operation
SAB 1793-02-P	Floppy-Disk-Controller (P-DIP 40); True Data Bus, single-sided operation
SAB 1795-02-P	Floppy-Disk-Controller (P-DIP 40); Inverted Data Bus, double-sided operation
SAB 1797-02-P	Floppy-Disk-Controller (P-DIP 40); True Data Bus, double-sided operation