

# 4GB DDR2 – SDRAM SO-DIMM

## 200 Pin SO-DIMM

SEN04G64D2BC2MT-xx[W]R

4GByte in FBGA Technology

RoHS compliant

### Options:

Data Rate / Latency	Marking
DDR2 667 MT/s CL5	-30
DDR2 800 MT/s CL6	-25

- Module Density  
4GByte with 16 dies and 2 ranks
- Standard Grade (T<sub>A</sub>) 0°C to 70°C  
(T<sub>C</sub>) 0°C to 85°C  
Grade W (T<sub>A</sub>) -40°C to 85°C  
(T<sub>C</sub>) -40°C to 95°C

\* The refresh rate has to be doubled when 85°C > T<sub>C</sub> > 95°C

### Environmental Requirements:

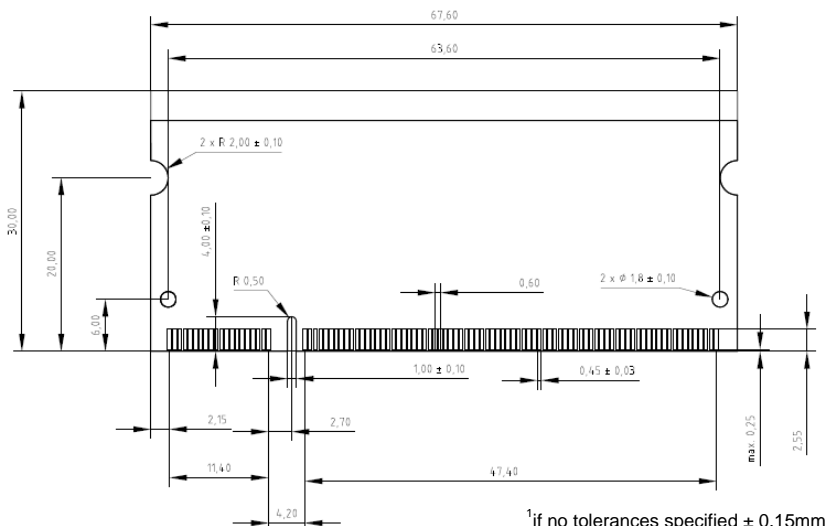
Operating temperature (ambient)	
Standard Grade	0°C to 70°C
Grade W	-40°C to 85°C

- Operating Humidity  
10% to 90% relative humidity, noncondensing
- Operating Pressure  
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature  
-55°C to 100°C
- Storage Humidity  
5% to 95% relative humidity, noncondensing
- Storage Pressure  
1682 PSI (up to 5000 ft.) at 50°C

### Features:

- 200-pin 64-bit Small Outline, Dual-In-Line Double Data Rate Synchronous DRAM Module
- Module organization: dual rank 512M x 64
- V<sub>DD</sub> = 1.8V ±0.1V, V<sub>DDQ</sub> 1.8V ±0.1V
- 1.8V I/O (SSTL\_18 compatible)
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC2-6400 spec. and JEDEC- Standard MO-224. (see [www.jedec.org](http://www.jedec.org))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR2 - SDRAM component Micron MT47H256M8EB-25E:C**
  - 256Mx8 DDR2 SDRAM in FBGA-60 package
  - Four bit prefetch architecture
  - DLL to align DQ and DQS transitions with CK
  - Eight internal device banks for concurrent operation
  - Programmable CAS latency (CL)
  - Posted CAS additive latency (AL)
  - WRITE latency = READ latency – 1 t<sub>CK</sub>
  - Programmable burst length: 4 or 8
  - Adjustable data-output drive strength
  - On-die termination (ODT)

Figure: mechanical dimensions<sup>1</sup>



This Swissbit module is an industry standard 200-pin 8-byte DDR2 SDRAM Small Outline Dual-In-line Memory Module (SO-DIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL\_18 compatible.

The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I<sup>2</sup>C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-DIMM manufacturer (swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

### Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Column Addr.	Refresh	Module Bank Select
512M x 64bit	16 x 256M x 8bit (2Gbit)	15	BA0, BA1, BA2	10	8k	S0#, S1#

### Module Dimensions

in mm

67.60 (long) x 30(high) x 3.80 [max] (thickness)

### Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEN04G64D2BC2MT-30[W]R	4GByte	5.3 GB/s	3.0ns / 667MT/s	5-5-5
SEN04G64D2BC2MT-25[W]R	4GByte	6.4 GB/s	2.5ns / 800MT/s	6-6-6

### Pin Name

A0 – A9, A11 – A14	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0 – DM7	Input Data Mask
DQS0 – DQS7	Data Strobe, positive line
DQS0# – DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK1	Clock Inputs, positive line

CK0# – CK1#	Clock Inputs, negative line
S0# – S1#	Chip Select
V <sub>DD</sub>	Supply Voltage (1.8V± 0.1V)
V <sub>REF</sub>	Input / Output Reference
V <sub>SS</sub>	Ground
V <sub>DDSPD</sub>	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0 – ODT1	On-Die Termination
NC	No Connection

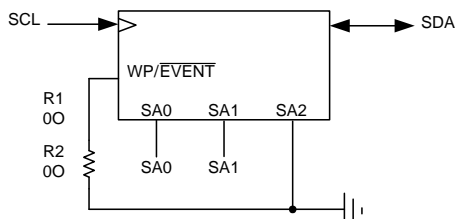
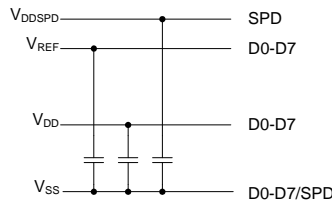
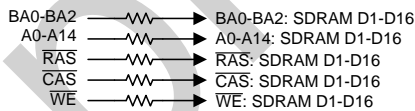
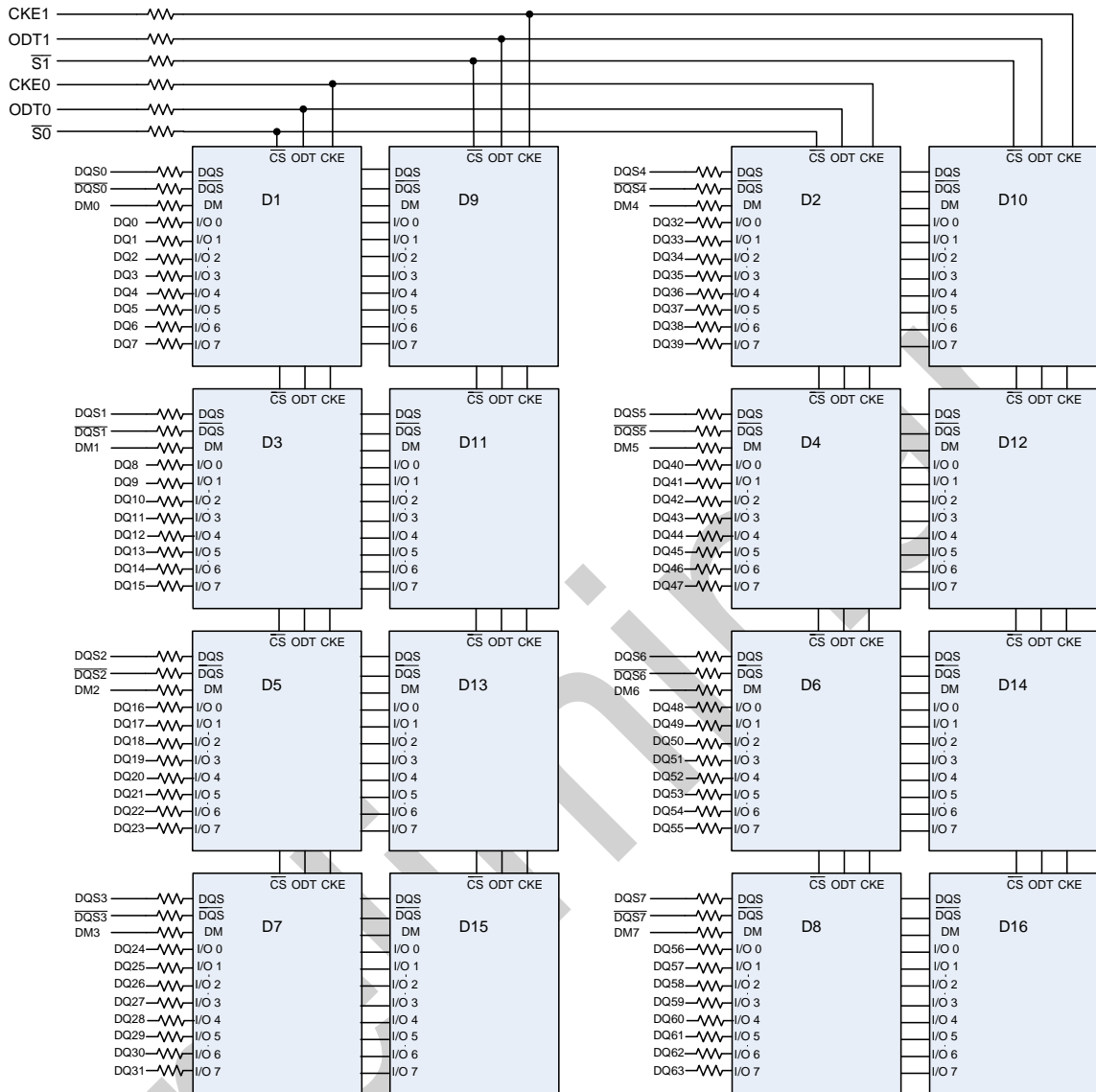
**Pin Configuration**

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	2	Vss	101	A1	102	A0
3	Vss	4	DQ4	103	VDD	104	VDD
5	DQ0	6	DQ5	105	A10/AP	106	BA1
7	DQ1	8	Vss	107	BA0	108	RAS#
9	Vss	10	DM0	109	WE#	110	S0#
11	DQS0#	12	Vss	111	VDD	112	VDD
13	DQS0	14	DQ6	113	CAS#	114	ODT0
15	Vss	16	DQ7	115	S1#	116	A13
17	DQ2	18	Vss	117	VDD	118	VDD
19	DQ3	20	DQ12	119	ODT1	120	NC (S3)
21	Vss	22	DQ13	121	Vss	122	Vss
23	DQ8	24	Vss	123	DQ32	124	DQ36
25	DQ9	26	DM1	125	DQ33	126	DQ37
27	Vss	28	Vss	127	Vss	128	Vss
29	DQS1#	30	CK0	129	DQS4#	130	DM4
31	DQS1	32	CK0#	131	DQS4	132	Vss
33	Vss	34	Vss	133	Vss	134	DQ38
35	DQ10	36	DQ14	135	DQ34	136	DQ39
37	DQ11	38	DQ15	137	DQ35	138	Vss
39	Vss	40	Vss	139	Vss	140	DQ44
41	Vss	42	Vss	141	DQ40	142	DQ45
43	DQ16	44	DQ20	143	DQ41	144	Vss
45	DQ17	46	DQ21	145	Vss	146	DQS5#
47	Vss	48	Vss	147	DM5	148	DQS5
49	DQS2#	50	NC (EVENT#)	149	Vss	150	Vss
51	DQS2	52	DM2	151	DQ42	152	DQ46

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	Vss	54	Vss	153	DQ43	154	DQ47
55	DQ18	56	DQ22	155	Vss	156	Vss
57	DQ19	58	DQ23	157	DQ48	158	DQ52
59	Vss	60	Vss	159	DQ49	160	DQ53
61	DQ24	62	DQ28	161	Vss	162	Vss
63	DQ25	64	DQ29	163	NC (TEST)	164	CK1
65	Vss	66	Vss	165	Vss	166	CK1#
67	DM3	68	DQS3#	167	DQS6#	168	Vss
69	NC (RESET#)	70	DQS3	169	DQS6	170	DM6
71	Vss	72	Vss	171	Vss	172	Vss
73	DQ26	74	DQ30	173	DQ50	174	DQ54
75	DQ27	76	DQ31	175	DQ51	176	DQ55
77	Vss	78	Vss	177	Vss	178	Vss
79	CKE0	80	CKE1	179	DQ56	180	DQ60
81	VDD	82	VDD	181	DQ57	182	DQ61
83	NC (S2#)	84	NC (A15)	183	Vss	184	Vss
85	BA2	86	A14	185	DM7	186	DQS7#
87	VDD	88	VDD	187	Vss	188	DQS7
89	A12	90	A11	189	DQ58	190	Vss
91	A9	92	A7	191	DQ59	192	DQ62
93	A8	94	A6	193	Vss	194	DQ63
95	VDD	96	VDD	195	SDA	196	Vss
97	A5	98	A4	197	SCL	198	SA0
99	A3	100	A2	199	VDDSPD	200	SA1

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

**FUNCTIONAL BLOCK DIAGRAM 4096MB DDR2 SDRAM SODIMM,  
2 RANKS AND 16 COMPONENTS**



**MAXIMUM ELECTRICAL DC CHARACTERISTICS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$	-1.0	2.3	V
I/O Supply Voltage	$V_{DDQ}$	-0.5	2.3	V
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	2.3	V
<b>INPUT LEAKAGE CURRENT</b> Any input $0V \leq V_{IN} \leq V_{DD}, V_{REF}$ pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	$I_I$			$\mu A$
Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
CK, CK#		-20	20	
DM		-5	5	
<b>OUTPUT LEAKAGE CURRENT</b> (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$
DQ, DQS, DQS#				
$V_{REF}$ LEAKAGE CURRENT ; $V_{REF}$ is on a valid level	$I_{VREF}$	-16	16	$\mu A$

**DC OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.125$	V

**AC INPUT OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.25$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.25$	V

**CAPACITANCE**

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

**I<sub>DD</sub> Specifications and Conditions**

 (0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

Parameter & Test Condition	max.			Unit	
	Symbol	6400-6-6-6	5300-5-5-5		
<b>OPERATING CURRENT *) :</b> One device bank Active-Precharge; t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	696	656	mA	
<b>OPERATING CURRENT *) :</b> One device bank; Active-Read-Precharge; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MIN (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I <sub>DD4W</sub>	I <sub>DD1</sub>	776	736	mA	
<b>PRECHARGE POWER-DOWN CURRENT:</b> All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2P</sub>	192	192	mA	
<b>PRECHARGE QUIET STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2Q</sub>	480	400	mA	
<b>PRECHARGE STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD2N</sub>	560	480	mA	
<b>ACTIVE POWER-DOWN CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>		Fast PDN Exit MR[12] = 0	400	400	mA
		Slow PDN Exit MR[12] = 1	224	224	mA
<b>ACTIVE STANDBY CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD3N</sub>	800	720	mA	

Parameter & Test Condition	max.			
	Symbol	6400-6-6-6	5300-5-5-5	Unit
<b>OPERATING READ CURRENT:</b> All device banks open, Continuous burst reads; One module rank active; $I_{OUT} = 0\text{mA}$ ; $BL = 4$ , $CL = CL(I_{DD})$ , $AL = 0$ ; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RAS} = t_{RAS\ MAX}(I_{DD})$ , $t_{RP} = t_{RP}(I_{DD})$ ; $CKE$ is HIGH, $CS\#$ is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	$I_{DD4R}$	1136	976	mA
<b>OPERATING WRITE CURRENT:</b> All device banks open, Continuous burst writes; One module rank active; $BL = 4$ , $CL = CL(I_{DD})$ , $AL = 0$ ; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RAS} = t_{RAS\ MAX}(I_{DD})$ , $t_{RP} = t_{RP}(I_{DD})$ ; $CKE$ is HIGH, $CS\#$ is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	$I_{DD4W}$	1136	976	mA
<b>BURST REFRESH CURRENT:</b> $t_{CK} = t_{CK}(I_{DD})$ ; refresh command at every $t_{RFC}(I_{DD})$ interval, $CKE$ is HIGH, $CS\#$ is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	$I_{DD5}$	2720	2640	mA
<b>SELF REFRESH CURRENT:</b> $CK$ and $CK\#$ at 0V; $CKE \leq 0.2V$ ; All other Control and Address bus inputs are floating at $V_{REF}$ ; DQ's are floating at $V_{REF}$	$I_{DD6}$	192	192	mA
<b>OPERATING CURRENT*) :</b> Four device bank interleaving READs, $I_{OUT} = 0\text{mA}$ ; $BL = 4$ , $CL = CL(I_{DD})$ , $AL = t_{RCD}(I_{DD}) - 1 \times t_{CK}(I_{DD})$ ; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RC} = t_{RC}(I_{DD})$ , $t_{RRD} = t_{RRD}(I_{DD})$ , $t_{RCD} = t_{RCD}(I_{DD})$ ; $CKE$ is HIGH, $CS\#$ is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	$I_{DD7}$	1856	1696	mA

**TIMING VALUES USED FOR  $I_{DD}$  MEASUREMENT**

<b><math>I_{DD}</math> MEASUREMENT CONDITIONS</b>			
SYMBOL	6400-6-6-6	5300-5-5-5	Unit
$CL(I_{DD})$	6	5	$t_{CK}$
$t_{RCD}(I_{DD})$	15	15	ns
$t_{RC}(I_{DD})$	60	60	ns
$t_{RRD}(I_{DD})$	7.5	7.5	ns
$t_{CK}(I_{DD})$	2.5	3.0	ns
$t_{RAS\ MIN}(I_{DD})$	45	45	ns
$t_{RAS\ MAX}(I_{DD})$	70'000	70'000	ns
$t_{RP}(I_{DD})$	15	15	ns
$t_{RFC}(I_{DD})$	195	195	ns



**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$ 

AC CHARACTERISTICS			6400-6-6-6		5300-5-5-5		Unit
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	
Clock cycle time	CL = 6	$t_{\text{CK}}(6)$	2.5	8.0	-	+	ns
	CL = 5	$t_{\text{CK}}(5)$	3.0-	8.0-	3.0	8.0	ns
	CL = 4	$t_{\text{CK}}(4)$	3.75	8.0	3.75	8.0	ns
	CL = 3	$t_{\text{CK}}(3)$	-	-	5.0	8.0	ns
CK high-level width		$t_{\text{CH}}$	0.48	0.52	0.45	0.55	$t_{\text{CK}}$
CK low-level width		$t_{\text{CL}}$	0.48	0.52	0.45	0.55	$t_{\text{CK}}$
Half clock period		$t_{\text{HP}}$	min ( $t_{\text{CH}}, t_{\text{CL}}$ )	-	min ( $t_{\text{CH}}, t_{\text{CL}}$ )	-	ps
Access window (output) of DQ <sub>s</sub> from CK/CK#		$t_{\text{AC}}$	-0.40	+0.40	-0.45	+0.45	ns
Data-out high-impedance window from CK/CK#		$t_{\text{HZ}}$	-	$t_{\text{AC max}}$	-	+0.45 (= $t_{\text{AC max}}$ )	ns
Data-out low-impedance window from CK/CK#		$t_{\text{LZ}}$	$t_{\text{AC min}}$	$t_{\text{AC max}}$	-0.45 (= $t_{\text{AC min}}$ )	+0.45 (= $t_{\text{AC max}}$ )	ns
DQ and DM input setup time relative to DQS		$t_{\text{DS}}$	0.05	-	0.10	-	ns
DQ and DM input hold time relative to DQS		$t_{\text{DH}}$	0.125	-	0.30	-	ns
DQ and DM input pulse width (for each input)		$t_{\text{DIPW}}$	0.35	-	0.35	-	$t_{\text{CK}}$
Data hold skew factor		$t_{\text{QHS}}$		0.3		0.34	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		$t_{\text{QH}}$	$t_{\text{HP}} - t_{\text{QHS}}$	-	$t_{\text{HP}} - t_{\text{QHS}}$	-	ns
Data valid output window		$t_{\text{DVW}}$	$t_{\text{QH}} - t_{\text{DQSQ}}$	-	$t_{\text{QH}} - t_{\text{DQSQ}}$	-	ns
DQS input high pulse width		$t_{\text{DQSH}}$	0.35	-	0.35	-	$t_{\text{CK}}$
DQS input low pulse width		$t_{\text{DQSL}}$	0.35	-	0.35	-	$t_{\text{CK}}$
DQS falling edge to CK rising - setup time		$t_{\text{DSS}}$	0.2	-	0.2	-	$t_{\text{CK}}$
DQS falling edge from CK rising - hold time		$t_{\text{DSH}}$	0.2	-	0.2	-	$t_{\text{CK}}$
DQS -DQ skew, DQS to last DQ valid, per group, per access		$t_{\text{DQSQ}}$	-	0.2	-	0.24	ns
DQS read preamble		$t_{\text{RPRE}}$	0.9	1.1	0.9	1.1	$t_{\text{CK}}$
DQS read postamble		$t_{\text{RPST}}$	0.4	0.6	0.4	0.6	$t_{\text{CK}}$
DQS write preamble		$t_{\text{WPRE}}$	0.35	-	0.35	-	$t_{\text{CK}}$
DQS write preamble setup time		$t_{\text{WPRES}}$	0	-	0	-	ns
DQS write postamble		$t_{\text{WPST}}$	0.4	0.6	0.4	0.6	$t_{\text{CK}}$
Positive DQS latching edge to associated clock edge		$t_{\text{DQSS}}$	- 0.25	+ 0.25	- 0.25	+ 0.25	$t_{\text{CK}}$
Write command to first DQS latching transition			WL- $t_{\text{DQSS}}$	WL+ $t_{\text{DQSS}}$	WL- $t_{\text{DQSS}}$	WL+ $t_{\text{DQSS}}$	$t_{\text{CK}}$
Address and control input pulse width (for each input)		$t_{\text{IPW}}$	0.6	-	0.6	-	$t_{\text{CK}}$
Address and control input setup time		$t_{\text{ISa}}$	0.175	-	0.4	-	ns

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**

(0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-6-6-6		5300-5-5-5		Unit
PARAMETER	SYMBOL	Min	Max	MIN	MAX	
Address and control input hold time	t <sub>IH</sub>	0.25	-	0.4	-	ns
CAS# to CAS# command delay	t <sub>CCD</sub>	2	-	2	-	t <sub>CK</sub>
ACTIVE to ACTIVE (same bank) command period	t <sub>RC</sub>	60	-	55	-	ns
ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	15	-	15	-	ns
Four bank Activate period	t <sub>FAW</sub>	37.5	-	37.5	-	ns
ACTIVE to PRECHARGE command	t <sub>RAS</sub>	45	70'000	45	70'000	ns
Internal READ to precharge command delay	t <sub>RTP</sub>	7.5	-	7.5	-	ns
Write recovery time	t <sub>WR</sub>	15	-	15	-	ns
Auto precharge write recovery + precharge time	t <sub>DAL</sub>	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>WR</sub> + t <sub>RP</sub>	-	ns
Internal WRITE to READ command delay	t <sub>WTR</sub>	7.5	-	7.5	-	ns
PRECHARGE command period	t <sub>RP</sub>	15	-	15	-	ns
PRECHARGE ALL command period	t <sub>RPA</sub>	t <sub>RP</sub> + t <sub>CK</sub>	-	t <sub>RP</sub> + t <sub>CK</sub>	-	ns
LOAD MODE command cycle time	t <sub>MRD</sub>	2	-	2	-	t <sub>CK</sub>
CKE low to CK, CK# uncertainty	t <sub>DELAY</sub>	t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>CK</sub>
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t <sub>RFC</sub>	195	70'000	195	70'000	ns
Average periodic refresh interval (0°C < T <sub>C</sub> < 85°C)	t <sub>REFI</sub>	-	7.8	-	7.8	μs
Average periodic refresh interval (85°C < T <sub>C</sub> < 95°C)		-	3.9	-	3.9	
Exit SELF REFRESH to non-READ command	t <sub>XSNR</sub>	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	ns
Exit SELF REFRESH to READ command	t <sub>XSRD</sub>	200	-	200	-	t <sub>CK</sub>
Exit SELF REFRESH timing reference	t <sub>ISXR</sub>	t <sub>IS</sub>	-	t <sub>IS</sub>	-	ps
ODT turn-on delay	t <sub>AOND</sub>	2	2	2	2	t <sub>CK</sub>
ODT turn-on	t <sub>AON</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1,000	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1,000	ps
ODT turn-off delay	t <sub>AOFD</sub>	2.5	2.5	2.5	2.5	t <sub>CK</sub>
ODT turn-off	t <sub>AOF</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	ps
ODT turn-on (power-down mode)	t <sub>AONPD</sub>	t <sub>AC</sub> (min) + 2,000	2 x t <sub>CK</sub> + t <sub>AC</sub> (max) + 1,000	t <sub>AC</sub> (min) + 2,000	2 x t <sub>CK</sub> + t <sub>AC</sub> (max) + 1,000	ps
ODT turn-off (power-down mode)	t <sub>AOFPD</sub>	t <sub>AC</sub> (min) + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (max) + 1,000	t <sub>AC</sub> (min) + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (max) + 1,000	ps
ODT to power-down entry latency	t <sub>ANPD</sub>	3	-	3	-	t <sub>CK</sub>

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**(0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-6-6-6		5300-5-5-5		Unit
PARAMETER	SYMBOL	Min	MAX	MIN	MAX	
ODT power-down exit latency	t <sub>AXPD</sub>	8	-	8	-	t <sub>CK</sub>
ODT enable from MRS command	t <sub>MOD</sub>	12	-	12	-	ns
Exit active power-down to READ command, MR [bit 12 = 0]	t <sub>XARD</sub>	2	-	2	-	t <sub>CK</sub>
Exit active power-down to READ command, MR [bit 12 = 1]	t <sub>XARDS</sub>	8 – AL	-	7 – AL	-	t <sub>CK</sub>
Exit precharge power-down to any non-READ command	t <sub>XP</sub>	2	-	2	-	t <sub>CK</sub>
CKE minimum high/low time	t <sub>CKE</sub>	3	-	3	-	t <sub>CK</sub>

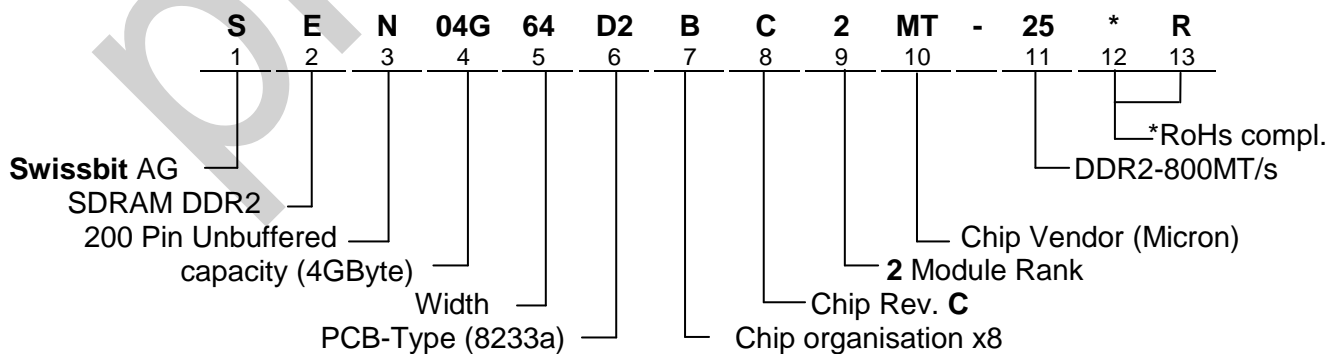
**SERIAL PRESENCE-DETECT MATRIX**

BYTE	DESCRIPTION	6400-6-6-6	5300-5-5-5
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x08	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0F	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A	
5	DIMM HIGHT AND MODULE RANKS	0x61	
6	MODULE DATA WIDTH	0x40	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V <sub>DDQ</sub> )	0x05	
9	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL] CL = 6 (6400), CL = 5 (5300)	0x25	0x30
10	SDRAM ACCESS FROM CLOCK, (t <sub>AC</sub> ) [max CL] CL = 6 (6400), CL = 5 (5300)	0x40	0x45
11	MODULE CONFIGURATION TYPE	0x00	
12	REFRESH RATE / TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00	
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00	
16	BURST LENGTHS SUPPORTED	0x0C	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08	
18	CAS LATENCIES SUPPORTED	0x70	0x38
19	MODULE THICKNESS	0x01	
20	DDR2 DIMM TYPE	0x04	
21	SDRAM MODULE ATTRIBUTES	0x00	
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03	
23	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL – 1] CL = 5 (6400), CL = 4 (5300)	0x30	0x3D
24	SDRAM ACCESS FROM CK, (t <sub>AC</sub> ) [max CL – 1] CL = 5 (6400), CL = 4 (5300)	0x40	0x45
25	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL – 2] CL = 4 (6400), CL = 3 (5300)	0x3D	0x50
26	SDRAM ACCESS FROM CK, (t <sub>AC</sub> ) [max CL – 2] CL = 4 (6400), CL = 3 (5300)	0x40	0x45
27	MINIMUM ROW PRECHARGE TIME, (t <sub>RP</sub> )	0x3C	
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t <sub>RRD</sub> )	0x1E	
29	MINIMUM RAS# TO CAS# DELAY, (t <sub>RCD</sub> )	0x3C	
30	MINIMUM RAS# PULSE WIDTH, (t <sub>RAS</sub> )	0x2D	
31	MODULE BANK DENSITY	0x02	

**SERIAL PRESENCE-DETECT MATRIX (continued)**

BYTE	DESCRIPTION	6400-6-6-6	5300-5-5-5
32	ADDRESS AND COMMAND SETUP TIME, (t <sub>ISb</sub> )	0x17	0x20
33	ADDRESS AND COMMAND HOLD TIME, (t <sub>IHb</sub> )	0x25	0x27
34	DATA / DATA MASK INPUT SETUP TIME, (t <sub>DSb</sub> )	0x05	0x10
35	DATA / DATA MASK INPUT HOLD TIME, (t <sub>DHb</sub> )	0x12	0x17
36	WRITE RECOVERY TIME, (t <sub>WR</sub> )	0x3C	
37	WRITE to READ Command Delay, (t <sub>WTR</sub> )	0x1E	
38	READ to PRECHARGE Command Delay, (t <sub>RTP</sub> )	0x1E	
39	Mem Analysis Probe	0x00	
40	Extension for Bytes 41 and 42	0x00	
41	MIN ACTIVE AUTO REFRESH TIME, (t <sub>RC</sub> )	0x3C	
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t <sub>RFC</sub> )	0xC3	
43	SDRAM DEVICE MAX CYCLE TIME, (t <sub>CKMAX</sub> )	0x80	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t <sub>DQSQ</sub> )	0x14	0x18
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t <sub>QHS</sub> )	0x1E	0x22
46	PLL Relock Time	0x00	
47-61	Optional Features, not supported	0x00	
62	SPD REVISION	0x13	
63	CHECKSUM FOR BYTES 0-62	0x0B	0x30
64-66	MANUFACTURER'S JEDEC ID CODE	0x7F	
67	MANUFACTURER'S JEDEC ID CODE (continued)	0xDA	
68-71	RESERVED	0x00	
72	MANUFACTURING LOCATION	0x01 (Switzerland)   0x02 (Germany)   0x03 (USA)	
73-90	MODULE PART NUMBER (ASCII)	"SEN04G64D2BC2MT-XX"	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	x	
128-255	Open for customer use	0xFF	

**Part Number Code**



\* optional / additional information

Revision History		
Revision	Changes	Date
0.9	Initial Revision	12.07.2013

preliminary

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# CE Declaration of Conformity

We

**Manufacturer:** Swissbit AG  
Industriestrasse 4  
CH-9552 Bronschhofen  
Switzerland

declare under our sole responsibility that the product

**Product Type:** 4GB DDR2 SO-DIMM  
**Brand Name:** SWISSMEMORY™  
**Product Series:** DDR2 SO-DIMM  
**Part Number:** SEN04G64D2BC2MT-xxxR

to which this declaration relates is in conformity with the following directives:

**2002/96/EC Category 3 (WEEE)**

following the provisions of Directive

**Restriction of the use of certain hazardous substances 2011/65/EU**

Swissbit AG, July 2013



Manuela Kögel  
Head of Quality Management