

# Advanced Power MOSFET

# SSP7N80A

## FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 $\mu$ A (Max.) @  $V_{DS} = 800V$
- Low  $R_{DS(ON)}$  : 1.472  $\Omega$  (Typ.)

$$BV_{DSS} = 800 V$$

$$R_{DS(on)} = 1.8 \Omega$$

$$I_D = 7 A$$

TO-220



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	800	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	7	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	4.4	
$I_{DM}$	Drain Current-Pulsed ①	28	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	523	mJ
$I_{AR}$	Avalanche Current ①	7	A
$E_{AR}$	Repetitive Avalanche Energy ①	16	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ C$ )	160	W
	Linear Derating Factor	1.28	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.78	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

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## N-CHANNEL POWER MOSFET

### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	800	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.93	--	V/°C	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-30V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=800V$
		--	--	250		$V_{DS}=640V, T_C=125^\circ C$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	1.8	$\Omega$	$V_{GS}=10V, I_D=0.85A$ ④*
$g_{fs}$	Forward Transconductance	--	4.95	--	$\text{S}$	$V_{DS}=50V, I_D=0.85A$ ④
$C_{iss}$	Input Capacitance	--	1500	1950	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	140	165		
$C_{rss}$	Reverse Transfer Capacitance	--	57	66		
$t_{d(on)}$	Turn-On Delay Time	--	23	55	ns	$V_{DD}=400V, I_D=2A,$ $R_G=16\Omega$ <b>See Fig 13</b> ④ ⑤
$t_r$	Rise Time	--	40	90		
$t_{d(off)}$	Turn-Off Delay Time	--	92	195		
$t_f$	Fall Time	--	34	80		
$Q_g$	Total Gate Charge	--	67	88	nC	$V_{DS}=640V, V_{GS}=10V,$ $I_D=2A$ <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
$Q_{gs}$	Gate-Source Charge	--	11.2	--		
$Q_{gd}$	Gate-Drain("Miller") Charge	--	29.6	--		

### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	7	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	28		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.4	V	$T_J=25^\circ C, I_S=7A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	520	--	ns	$T_J=25^\circ C, I_F=7A$
$Q_{rr}$	Reverse Recovery Charge	--	6.66	--	$\mu C$	$di_F/dt=100A/\mu s$ ④

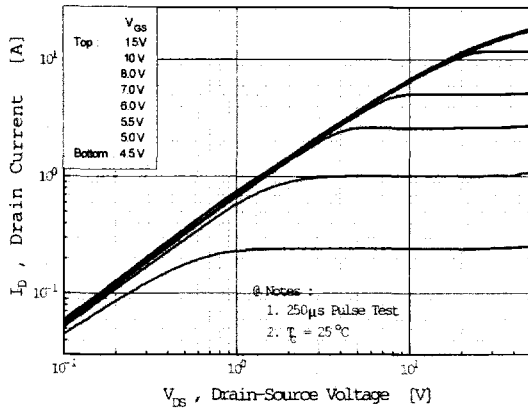
#### Notes ;

- Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- $L=20\text{mH}, I_{AS}=7A, V_{DD}=50V, R_G=27\Omega$ , Starting  $T_J=25^\circ C$
- $I_{SD} \leq 7A, di/dt \leq 150A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ C$
- Pulse Test : Pulse Width =  $250\mu s$ , Duty Cycle  $\leq 2\%$
- Essentially Independent of Operating Temperature

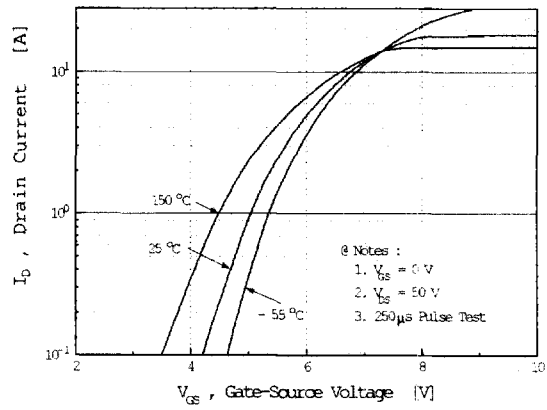
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**SSP7N80A**

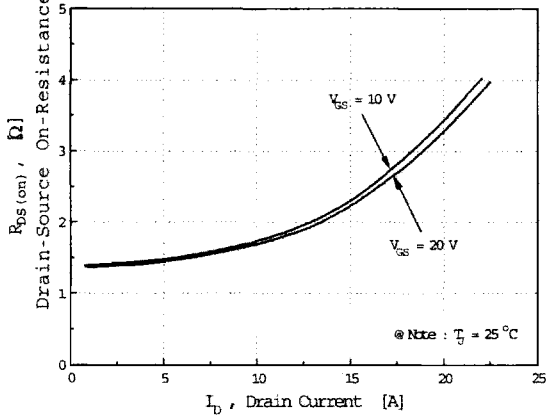
**Fig 1. Output Characteristics**



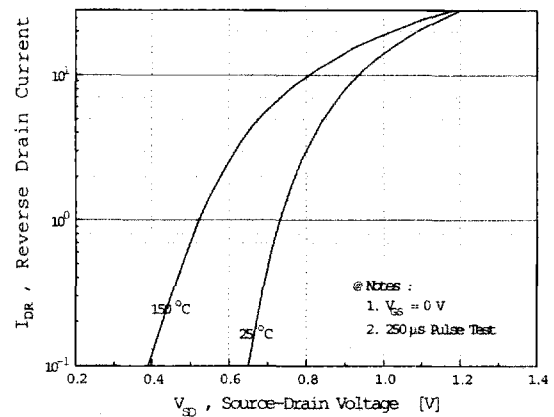
**Fig 2. Transfer Characteristics**



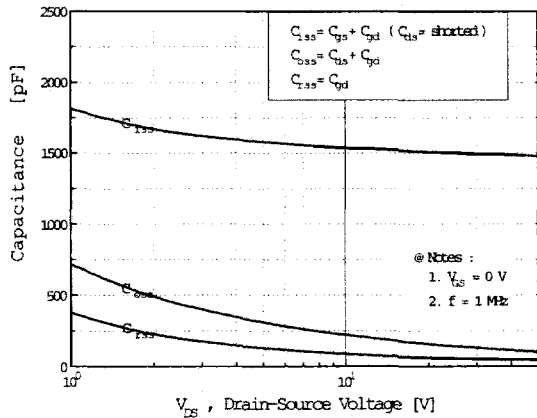
**Fig 3. On-Resistance vs. Drain Current**



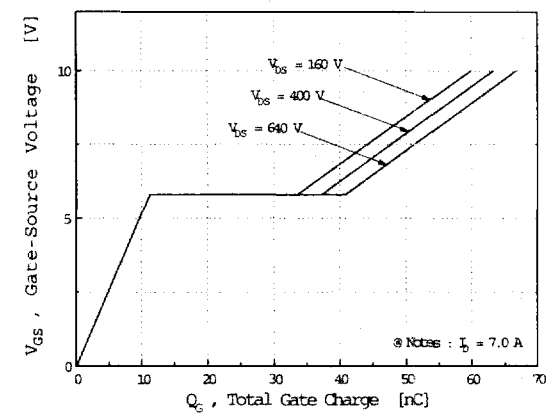
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**

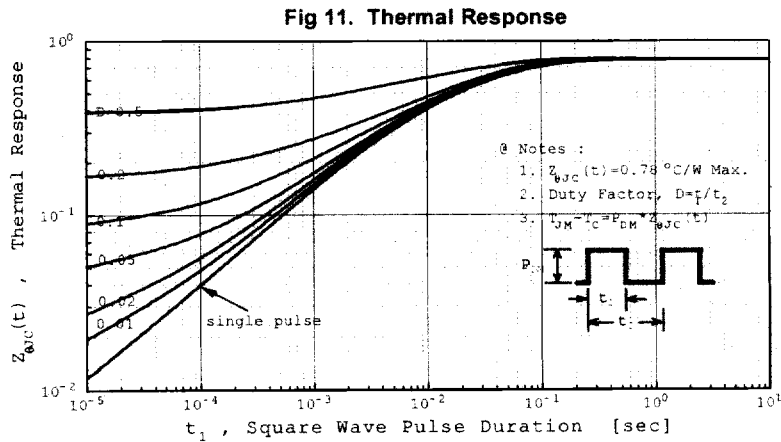
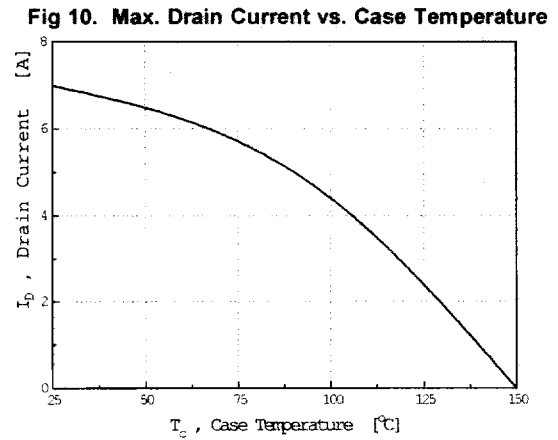
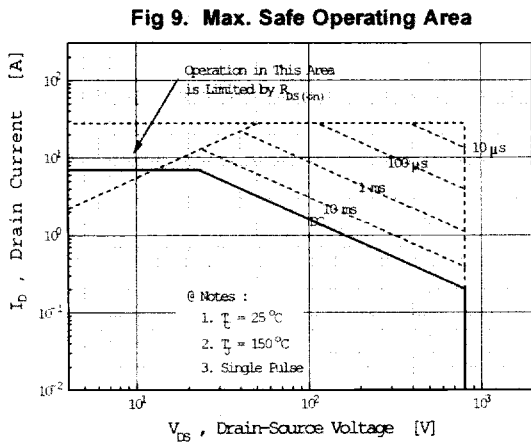
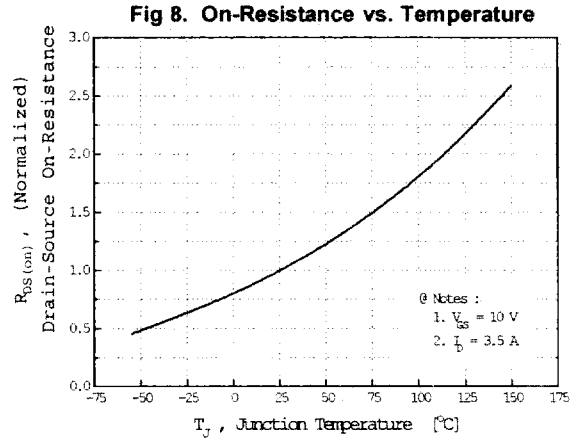
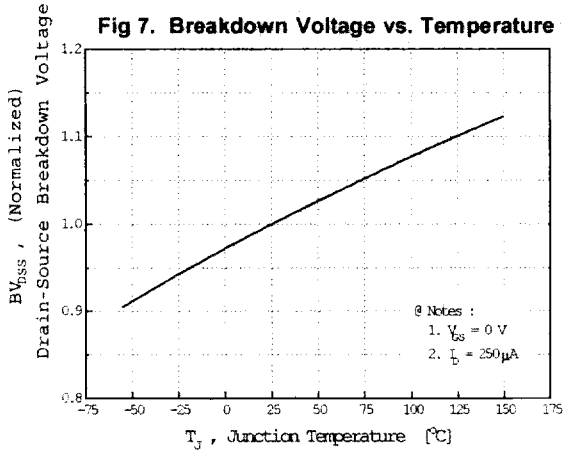


**Fig 6. Gate Charge vs. Gate-Source Voltage**

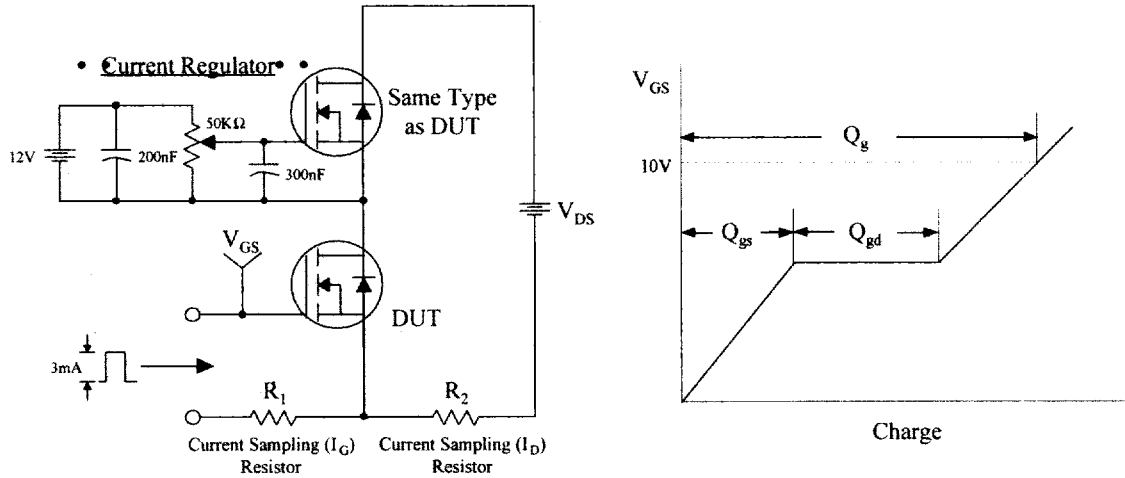


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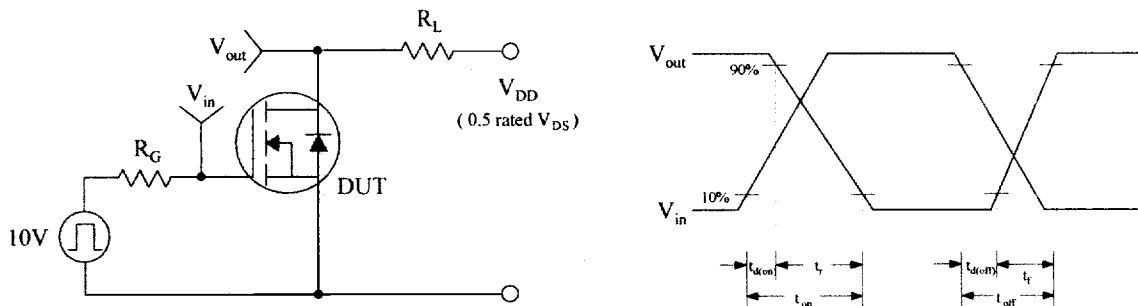
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**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

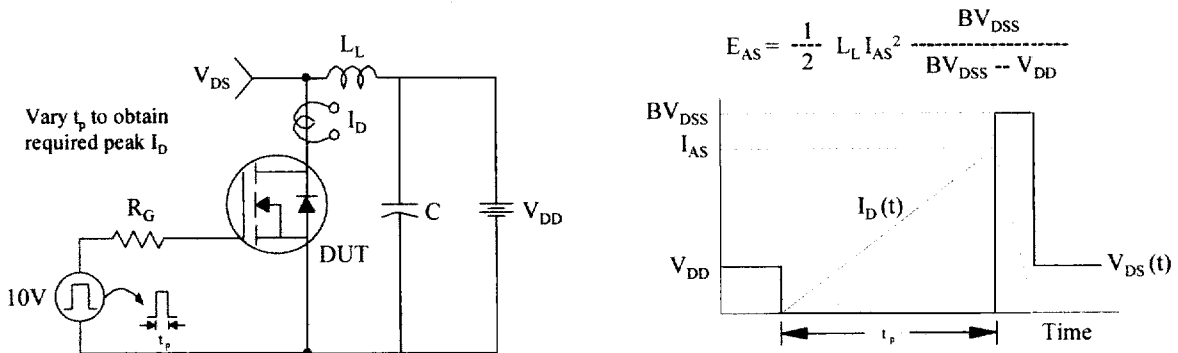


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

