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AK1542A

20 to 600MHz Integer-N Frequency Synthesizer

1. Overview

Consisting a highly accurate charge pump that supports current adjustment in 9 steps, a reference divider, a programmable divider and a dual-modulus prescaler (P/P+1), the AK1542A provides high performance, low consumption current and small footprint for a wide range of frequency conversions . This synthesizer also has two general-purpose output pins which allow it to be used to control the RF front end.

An ideal Phase Locked Loop (PLL) can be achieved by combining the AK1542A with the external loop filter and VCO (Voltage Controlled Oscillator). Access to the registers is controlled via a 3-wire serial interface. The operating supply voltage is from 2.7 to 5.5V; and the supply voltage for the charge pump and that for the serial interface can be driven separately.

2. Features

□	Operating frequency:	20 to 600MHz
□	Programmable charge pump current:	
		158 to 2528μA typical The charge pump current can be changed in 9 steps; and the current range can be adjusted by the external resistance. Two current settings can be specified with the register and switched over from one to another using the timer.
□	Supply Voltage:	2.7 to 5.5 V (PVDD pin)
□	Separate power supply for the charge pump:	PVDD to 5.5V (CPVDD pin)
□	On-chip power-saving features	
□	On-chip lock detection feature of PLL:	Direct output to the PFD (Phase frequency detector) or digital filtering output can be selected.
□	General-purpose output:	It has two general-purpose output ports to control peripheral parts.
□	Very low consumption current:	2.2mA typical
□	Package:	24pin QFN (0.5mm pitch, 4mm×4mm×0.75mm)
□	Operating temperature:	-40°C to 85°C

Table of Contents

In this specification (draft version), the following notations are used for specific signal and register names:

[Name]: Pin name

<Name>: Register group name (Address name)

{Name}: Register bit name

3. Block Diagram

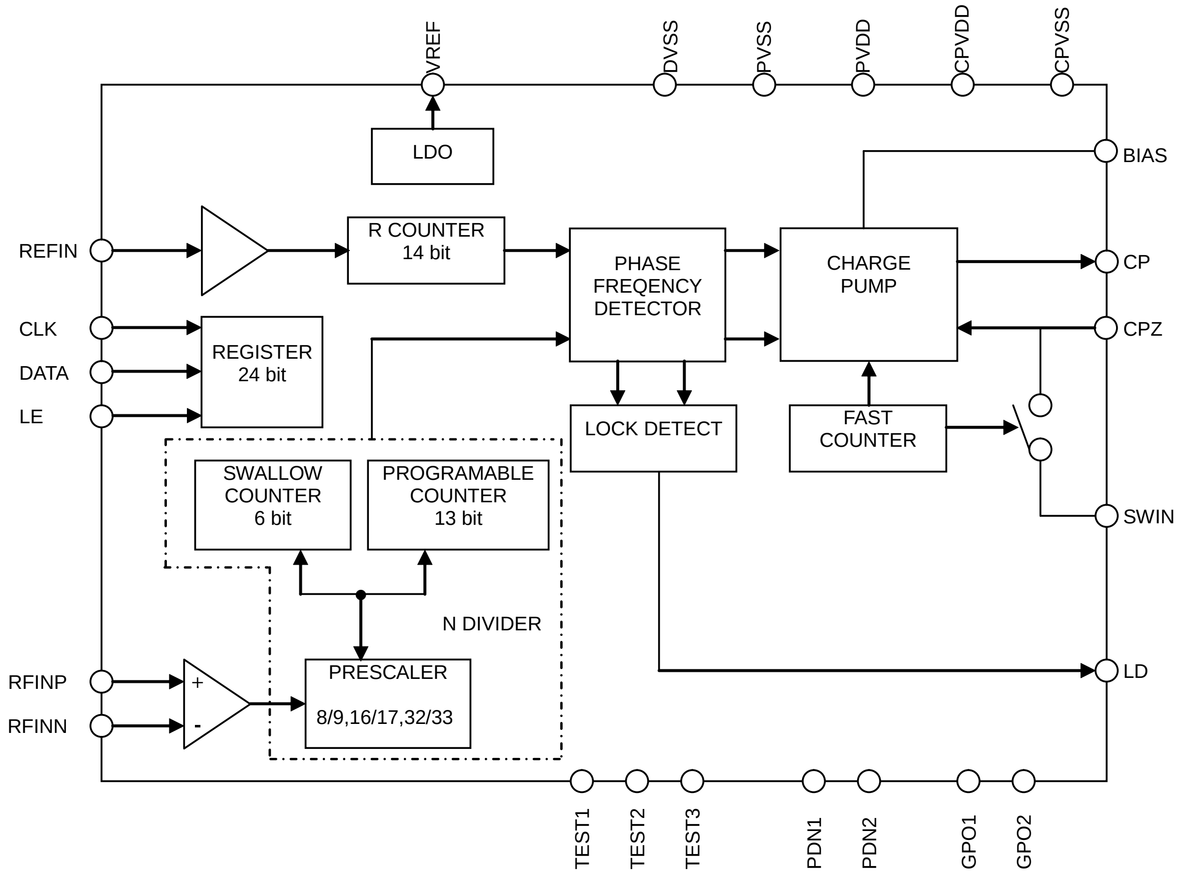


Fig. 1 Block Diagram

4. Pin Functional Description

Table 1 Pin Functions

No.	Name	I/O	Pin Functions	Power down	Remarks
1	CPVDD	P	Power supply for charge pump		
2	TEST3	DI	Test pin 3, This pin must be connected to ground.		Internal pull-down, Schmidt trigger input
3	TEST1	DI	Test pin 1, This pin must be connected to ground.		Internal pull-down, Schmidt trigger input
4	LE	DI	Load enable		Schmidt trigger input
5	DATA	DI	Serial data input		Schmidt trigger input
6	CLK	DI	Serial clock		Schmidt trigger input
7	LD	DO	Lock detect	“Low”	
8	PDN2	DI	Power down pin for PLL		Schmidt trigger input
9	PDN1	DI	Power down signal for LDO		Schmidt trigger input
10	REFIN	AI	Reference input		
11	TEST2	DI	Test pin 2, This pin must be connected to ground.		Internal pull-down, Schmidt trigger input
12	GPO1	DO	General-purpose output pin 1	“Low”	
13	GPO2	DO	General-purpose output pin 2	“Low”	
14	DVSS	G	Digital ground pin		
15	VREF	AO	Connect to LDO reference voltage capacitor	“Low”	
16	RFINN	AI	Prescaler input		
17	RFINP	AI	Prescaler input		
18	PVDD	P	Power supply for peripherals		
19	BIAS	AIO	Resistance pin for setting charge pump current		
20	PVSS	G	Ground pin for peripherals		
21	CP	AO	Charge pump output	“Hi-Z”	
22	CPZ	AIO	Connect to the loop filter capacitor		Notes 1) & 2)
23	SWIN	AI	Connect to resistance pin for fast Lock Up		Notes 1) & 2)
24	CPVSS	G	Ground pin for charge pump power supply		

Note 1) For detailed functional descriptions, see the section “Charge Pump and Loop Filter” in “8. Block Functional Descriptions”.

Note 2) The input voltage from the [CPZ] pin is used in the internal circuit. The [CPZ] pin must not be open even when the fast Lock Up feature is unused.

For the output destination from the [CPZ] pin, see “P.12 Fig.5 Loop Filter Schematic”. The [SWIN] pin could be open when the fast Lock Up feature is not used.

Note 3) Power down refers to the state where [PDN1]=[PDN2]=”Low” after power-on.

Note 4) TEST1 to 3 must be connected to ground.

AI: Analog input pin	AO: Analog output pin	AIO: Analog I/O pin	DI: Digital input pin
DO: Digital output pin	P: Power supply pin	G: Ground pin	

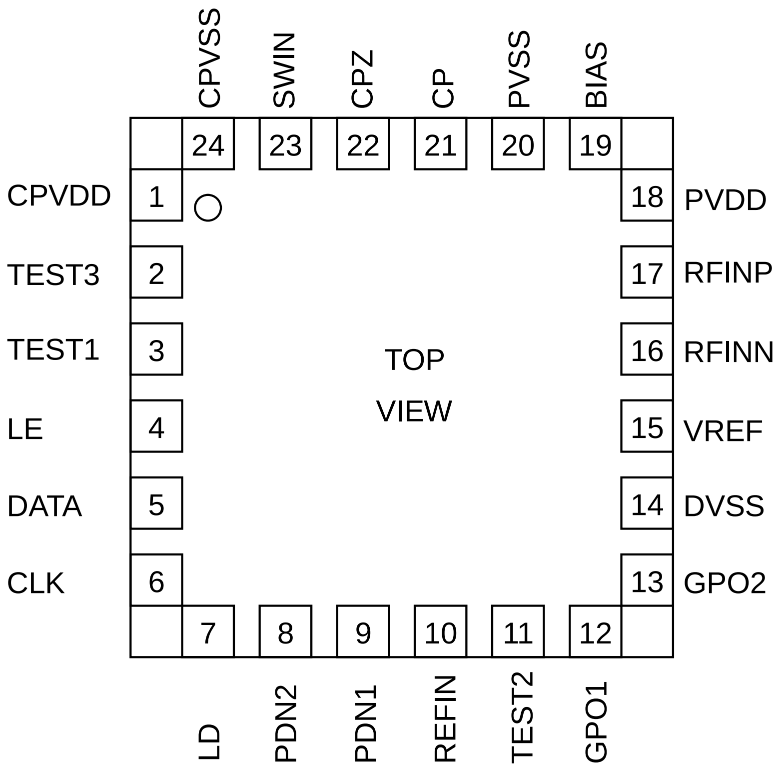


Fig. 2 Package Pin Layout

5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD1	-0.3	6.5	V	Note 1), Applied to [PVDD] pin
	VDD2	-0.3	6.5	V	Note 1), Applied to [CPVDD] pin
Ground Level	VSS1	0	0	V	Voltage ground level, applied to [PVSS] pin
	VSS2	0	0	V	Voltage ground level, applied to [CPVSS] pin
	VSS3	0	0	V	Voltage ground level, applied to [DVSS] pin
Analog Input Voltage	VAIN1	VSS1-0.3	VDD1+0.3	V	Notes 1) & 2)
	VAIN2	VSS2-0.3	VDD2+0.3	V	Notes 1) & 3)
Digital Input Voltage	VDIN	VSS3-0.3	VDD1+0.3	V	Notes 1) & 4)
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note 1) 0V reference for all voltages.

Note 2) Applied to [REFIN], [RFINN] and [RFINP] pins.

Note 3) Applied to [CPZ] and [SWIN] pins.

Note 4) Applied to [CLK], [DATA], [LE], [PDN1], [PDN2], [TEST1], [TEST2] and [TEST3] pins.

Exceeding these maximum ratings may result in damage to the AK1542A. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Range

Table 3 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD1	2.7	3.3	5.5	V	Applied to [PVDD] pin
	VDD2	VDD1	5.0	5.5	V	Applied to [CPVDD] pin

Note 1) VDD1 and VDD2 can be driven individually within the recommended operating range.

The specifications are applicable within the recommended operating range (supply voltage /operating temperature).

7. Electrical Characteristics

1. Digital DC Characteristics

Table 4 Digital DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
High level input voltage	Vih		0.8×VDD1			V	Note 1)
Low level input voltage	Vil				0.2×VDD1	V	Note 1)
High level input current 1	Iih1	Vih = VDD1=5.5V	-1		1	µA	Note 2)
High level input current 2	Iih2	Vih = VDD1=5.5V	27	55	110	µA	Note 3)
Low level input current	Iil	Vil = 0V, VDD1=5.5V	-1		1	µA	Note 1)
High level output voltage	Voh	Ioh = -500µA	VDD1-0.4			V	Note 4)
Low level output voltage	Vol	Iol = 500µA			0.4	V	Note 4)

Note 1) Applied to [CLK], [DATA], [LE], [PDN1], [PDN2], [TEST1], [TEST2] and [TEST3] pins.

Note 2) Applied to [CLK], [DATA], [LE] , [PDN1]and [PDN2] pins.

Note 3) Applied to [TEST1], [TEST2] and [TEST3] pins.

Note 4) Applied to [LD], [GPO1] and [GPO2] pins.

2. Serial Interface Timing

<Write-In Timing>

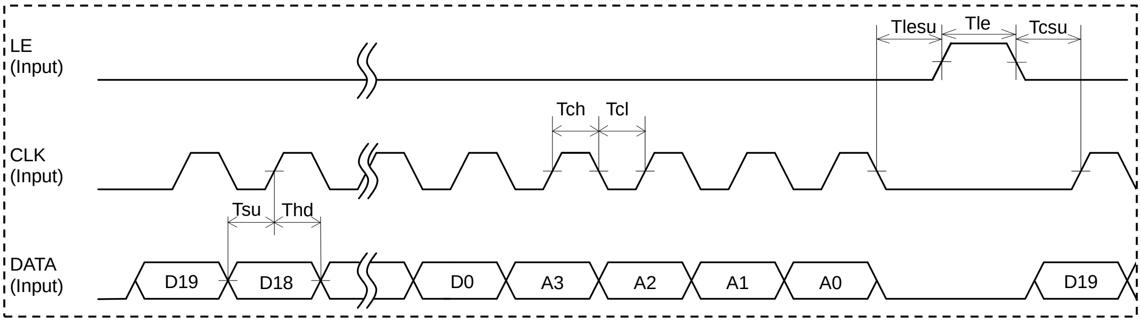


Fig. 3 Serial Interface Timing

Table 5 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock L level hold time	Tcl	40			ns	
Clock H level hold time	Tch	40			ns	
Clock setup time	Tcsu	20			ns	
Data setup time	Tsu	20			ns	
Data hold time	Thd	20			ns	
LE Setup Time	Tlesu	20			ns	
LE Pulse Width	Tle	40			ns	

Note 1) While [LE] pin is setting at “Low”, 24 iteration clocks have to be set with [CLK] pin. If 25 or larger clocks are set, the last 24 clocks synchronized data are valid.

3. Analog Circuit Characteristics

The resistance of 27kΩ is connected to the [BIAS] pin, VDD1=2.7 to 5.5V, VDD2=VDD1 to 5.5V, –40°C≤Ta≤85°C

Parameter	Min.	Typ.	Max.	Unit	Remarks
RF Characteristics					
Input Sensitivity	-15		+5	dBm	Input frequency ≥ 100MHz
	-5		+5		20MH ≤ Input frequency < 100MHz
Input Frequency	20		600	MHz	
REFIN Characteristics					
Input Sensitivity	0.4		2	Vpp	
Input Frequency	5		40	MHz	
Maximum Allowable Prescaler Output Frequency			75	MHz	
Phase Detector					
Phase Detector Frequency			3	MHz	
Charge Pump					
Charge Pump Maximum Value		2528		µA	
Charge Pump Minimum Value		158		µA	
Icp TRI-STATE Leak Current		1		nA	0.7 ≤ Vcpo ≤ VDD2-0.7 Vcpo : Voltage at [CP] pin
Mismatch between Source and Sink Currents Note 1)			10	%	Vcpo = VDD2/2, Ta=25°C
Icp vs. Vcpo Note 2)			15	%	0.5 ≤ Vcpo ≤ VDD2-0.5, Ta=25°C
Others					
VREF Rise Time			50	µs	
Consumption Current					
IDD1			10	µA	[PDN1]="Low", [PDN2]="Low"
IDD2		1.8	2.7	mA	[PDN1]="High",[PDN2]="High" IDD for [PVDD]
IDD3 Note 3)		0.4	0.9	mA	[PDN1]="High",[PDN2]="High" IDD for [CPVDD]
IDD4		0.5	1	mA	[PDN1]="High",[PDN2]="Low" IDD for [PVDD]

Note 1) Mismatch between Source and Sink Currents: [(|Isink|-|Isource|)/{(|Isink|+|Isource|)/2}] × 100 [%]

Note 2) See "Fig. 4 Charge Pump Characteristics - Voltage vs. Current": Icp vs. Vcpo:

[{1/2×(|I1|-|I2|)}/{1/2×(|I1|+|I2|)}]×100 [%]

Note 3) IDD3 doesn't include the current depending on Phase Detector Frequency. IDD3 is the current the Charge Pump circuit consumes constantly.

Note 4) In the case of [PDN1]="High" and [PDN2]="High", the total current consumption = IDD2 + IDD3.

Note 5) The shipment test is done with the exposed pad at the center of backside connected to VSS.

Resistance Connected to the BIAS Pin for Setting Charge Pump Output Current

Parameter	Min.	Typ.	Max.	Unit	Remarks
BIAS resistance	22	27	33	kΩ	

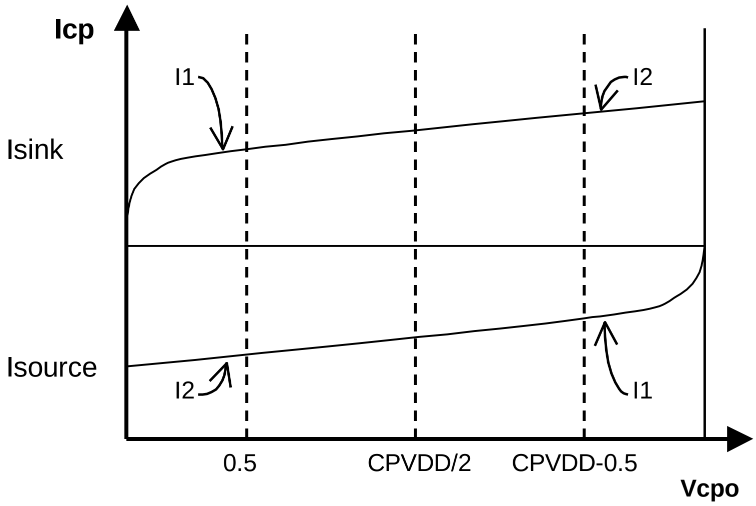


Fig. 4 Charge Pump Characteristics - Voltage (Vcpo) vs. Current (Icp)

8. Block Functional Descriptions

1. Frequency Setup

The following formula is used to calculate the frequency setting for AK1542A.

Frequency setting (external VCO output frequency) = $F_{PFD} \times N$

N	: Dividing number $N = [(P \times B) + A]$
F_{PFD}	: Phase detector frequency F_{PFD} = [REFIN] pin input frequency / R counter dividing number
P	: Prescaler Value (See<Address2>:{Pre[1:0]})
B	: B (Programmable) counter value (See <Address1>:{B[12:0]})
A	: A (Swallow) counter value (See <Address1>:{A[5:0]})

Calculation examples

When the [REFIN] pin input frequency is 10MHz, the phase detector frequency F_{PFD} =5kHz and the frequency setting = 460.1MHz;

[The AK1542A Settings]

R=10000000/5000 = 2000 (<Address3> : {R[13:0]}=2000dec)

P=32 (<Address2>:{Pre[1:0]} =10bin)

B=2875 (<Address1>:{B[12:0]} =2875dec)

A=20 (<Address1>:{A[5:0]} =20dec)

Frequency setting = 5000 × [(32×2875) + 20] = 460.1MHz

Lower limit for setting consecutive dividing numbers

In the AK1542A, it is impossible to set consecutive dividing numbers below the lower limit. The lower limit is calculated by the following formula;

$N_{min}=P^2-P$

For example, in the case of P=16, it can be set 240 and over as consecutive dividing numbers.

2. Charge Pump and Loop Filter

In AK1542A, the fast Lock Up could be achieved by changing a charge pump current and enabling the loop filter. This is called Fast Lock Up mode. For details, see ”3. Fast Lock Up Mode” on page 13.

The loop filter is external and connected to [CP], [SWIN] and [CPZ] pins. The [CPZ] pin should be connected to the R2 and C2, which are intermediate nodes, even if the Fast Lock Up is not used. Therefore, R2 must be connected to the [CP] pin, while C2 must be connected to the ground.

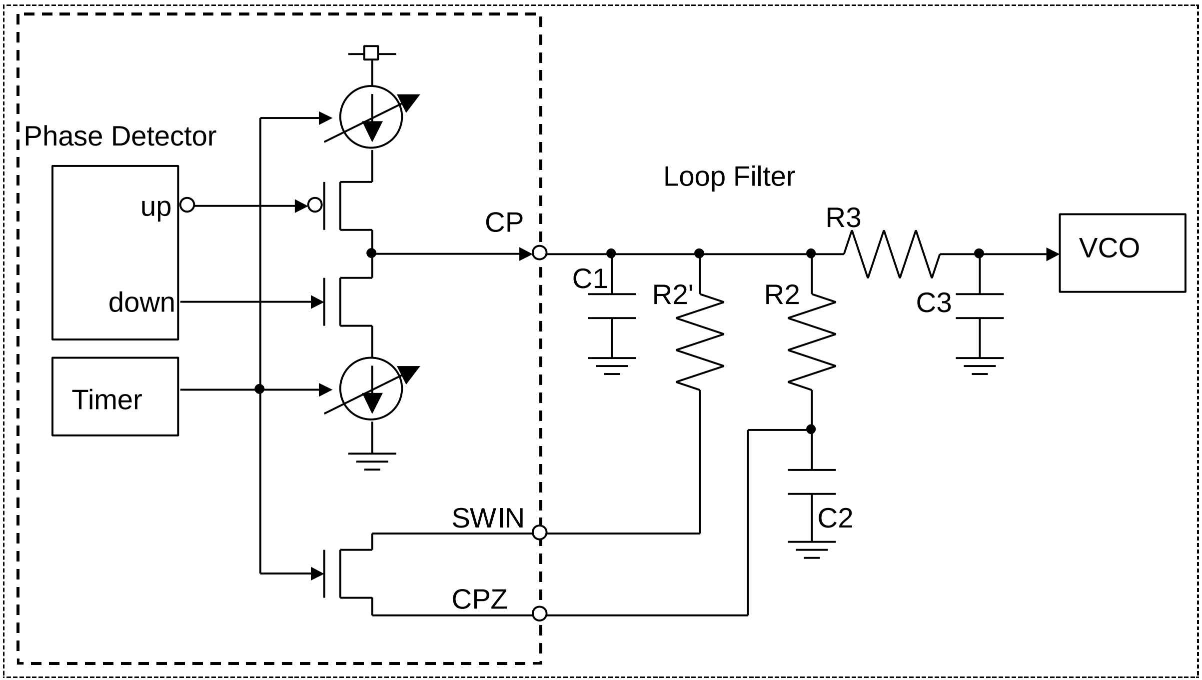


Fig. 5 Loop Filter Schematic

3. Fast Lock Up Mode

Setting D[16]={FASTEN} in <Address4> to 1 enables the Fast Lock Up mode for AK1542A.

Changing a frequency setting (The frequency is changed at the rising edge of [LE] when <Address1> and <Address2> are accessed.) or [PDN2] pin is set from ”Low” to ”High” with {FASTEN}=1 enables the Fast Lock Up mode. The loop filter switch turns ON during the timer period specified by the counter value in D[12:0] = {FAST[12:0]} in <Address4>, and the charge pump for the Fast Lock Up mode (Charge Pump 2) set by D[9:6] = {CP2[3:0]} in <Address2> is enabled.

After the timer period elapsed, the loop filter switch turns OFF, the charge pump for normal operation (Charge Pump 1) set by D[3:0] = {CP1[3:0]} in <Address2> is enabled and thus normal operation returns.

The register D[12:0] = {FAST[12:0]} in <Address4> is used to set the timer period for this mode. The following formula is used to calculate the time period:

Phase detector frequency cycle × counter value set in {FAST[12:0]}

The charge pump current could be adjusted with 9 steps for both normal operation (Charge Pump 1) and the Fast Lock Up operation (Charge Pump 2).

The absolute value of the charge pump current is determined by the Resistor value connected to the [BIAS] pin. The following formula shows the relationship between the resistance value, the register setting and the electric current value.

Charge pump minimum current (Icp_min) [A] = 8.55 / Resistance connected to the [BIAS] pin (Ω)

Charge pump current [A] = Icp_min [A] × (CP1 or CP2 setting + 1)

The allowed range value for the resistance connected to the [BIAS] pin is from 22 to 33 [kΩ]. For details of current settings, see ”Register Functional Description”.

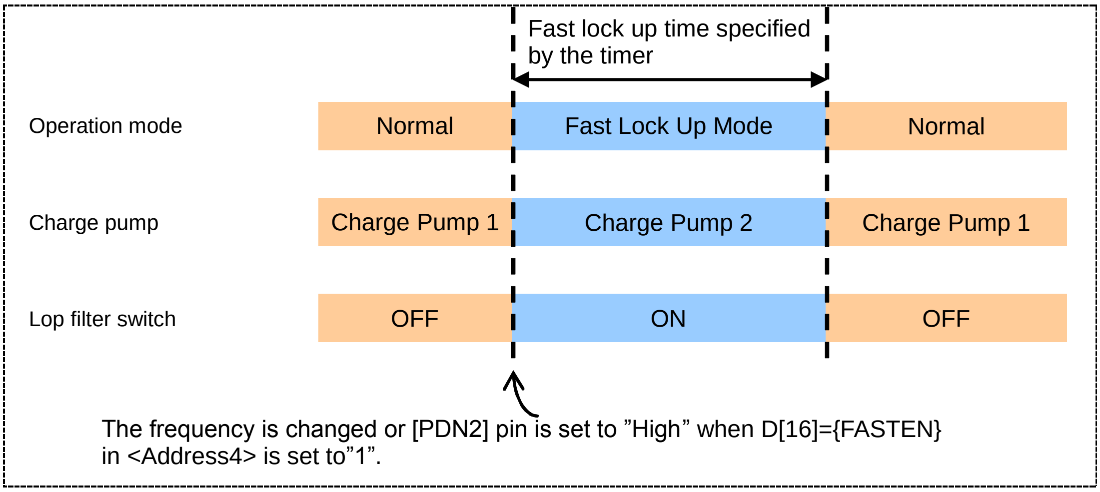


Fig. 6 Timing Chart for Fast Lock Up Mode

4. Lock Detect (LD) Signal

In AK1542A, the lock detect output can be selected by D[13] = {LD} in <Address4>. When D[13] is set to "1", the phase detector outputs provide a phase detection as an analog level (comparison result). This is called "analog lock detect".
When D[13] is set to "0", the lock detect signal is output according to the internal logic. This is called "digital lock detect".

4.1 Analog Lock Detect

In analog lock detect, the phase detector output comes from the LD pin.

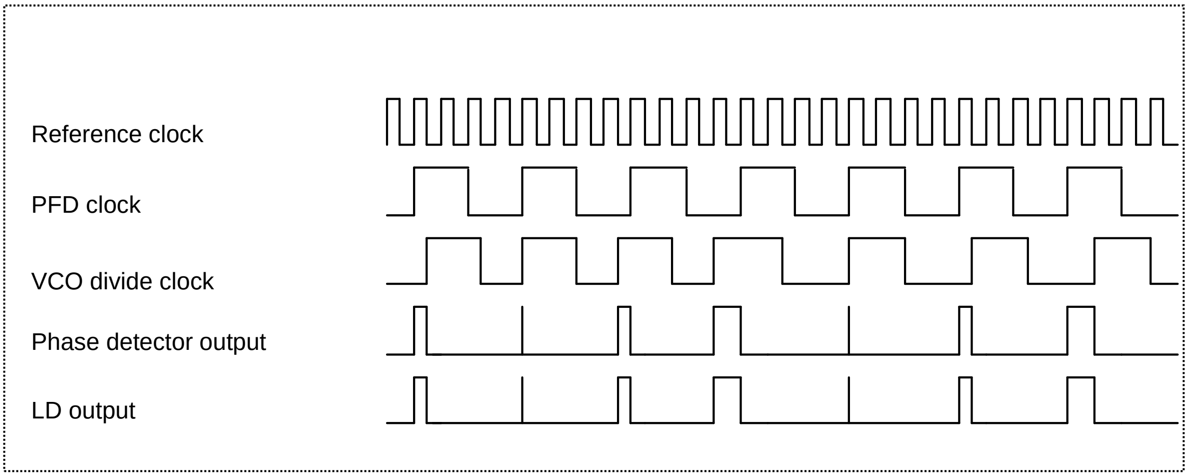


Fig. 7 Analog Lock Detect Operation

4.2 Digital Lock Detect

In the digital lock detect, the [LD] pin outputs is "Low" every time when the frequency is set. And the [LD] pin outputs "High" (which means the locked state) when a phase error smaller than T is detected for N times consecutively. If the phase error larger than T is detected for N times consecutively when the [LD] pin outputs "High", the [LD] pin outputs "Low"(which means the unlocked state).

The threshold counts for lock detection N could be set by D[18:17]={LDCNTSEL[1:0]} in <Address4>.

{LDCNTSEL[1:0]} settings and corresponding counts (N) are as follows:

00: N = 7

01: N = 15

10: N = 31

11: N = 63

The lock detect signal is shown below:

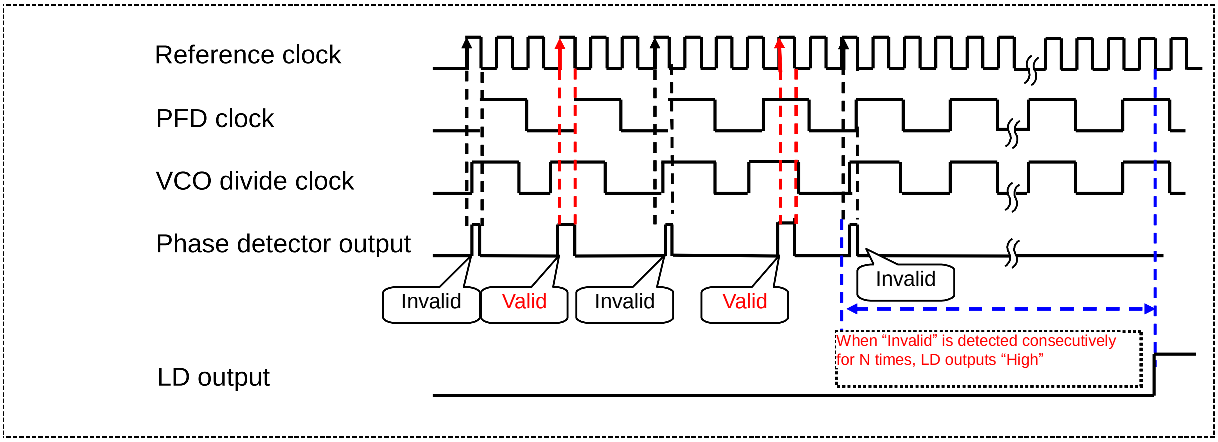


Fig. 8 Digital Lock Detect Operations

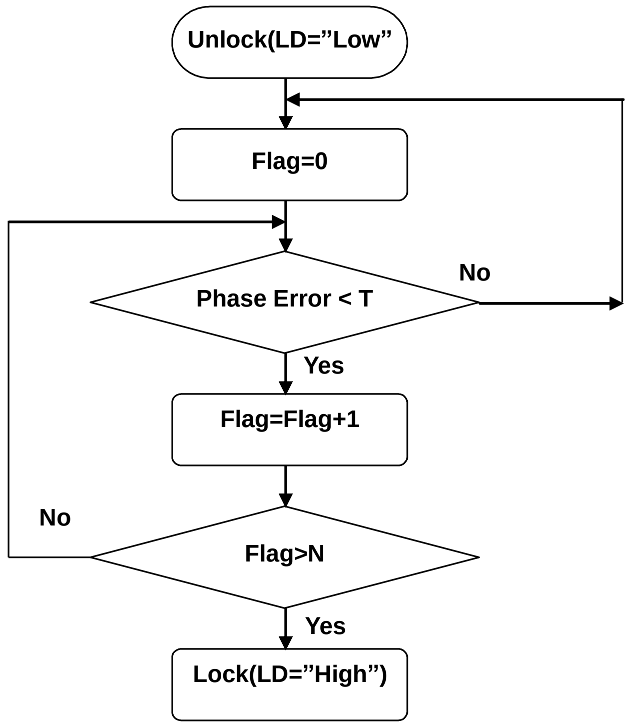


Fig. 9 Transition Flow Chart: Unlock State to Lock State

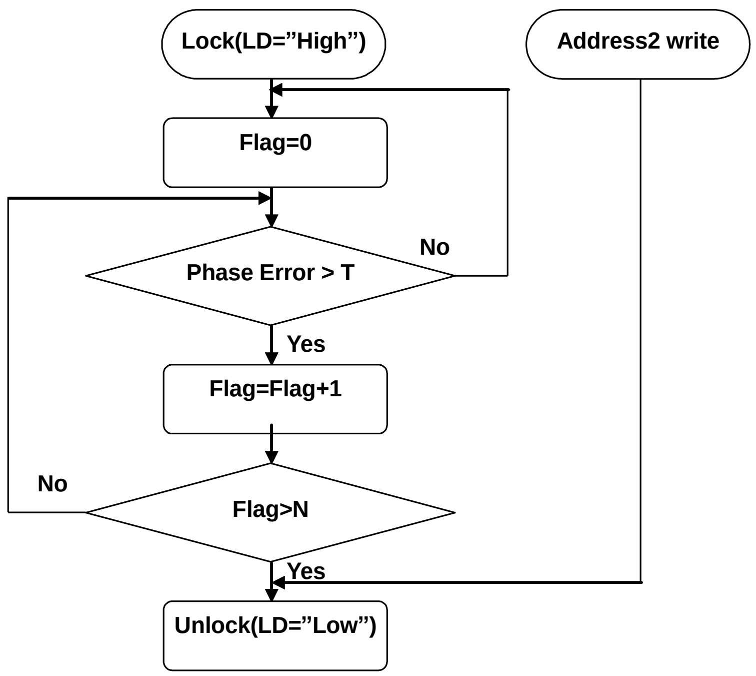


Fig. 10 Transition Flow Chart: Lock State to Unlock State

5. Reference Input

The reference input could be set to a dividing number in the range of 4 to 16383 using {R[13:0]}, which is a 14-bit address of D[13:0] in <Address3>. A dividing number from 0 to 3 could not be set.

6. Prescaler and Swallow Counter

The dual modular prescaler (P/P+1) and the swallow counter are used to provide a large dividing ratio. The prescaler is set by {PRE[1:0]}, which is a 2-bit address of D[15:14] in <Address3>.

{PRE[1:0]}=”00”: P=8, dividing ratio = 8/9
{PRE[1:0]}=”01”: P=16, dividing ratio = 16/17
{PRE[1:0]}=”10”: P=32, dividing ratio = 32/33
{PRE[1:0]}=”11”: Prohibited

7. Power Save Mode

AK1542A can be operated in the power-down or power-save mode as necessary by using the external control pins [PDN1] and [PDN2].

Power On

See “13. Power-up Sequence”. It is necessary to bring [PDN1] to “High” first, then [PDN2]. Bringing [PDN1] and [PDN2] to “High” simultaneously is prohibited.

Normal Operation

Pin name		State
PDN1	**PDN2**	
“Low”	“Low”	Power down
“Low”	“High”	Prohibited
“High”	“Low”	Power save Mode Note 1) and Note 2)
“High”	“High”	Normal Operation

Note 1) Register setup can be made 50μs after [PDN1] is set to “High”. The charge pump is in the Hi-Z state.

Note 2) Register settings are maintained when [PDN2] is set to “Low” during normal operation.

9. Register Map

Name	Data	Address			
A/B	D19 to D0	0	0	0	1
CP		0	0	1	0
Ref/Pres		0	0	1	1
Function		0	1	0	0
GPO		0	1	0	1

	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
A/B	0	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	0x01
CP	0	0	0	0	0	0	0	0	0	0	CP2 [3]	CP2 [2]	CP2 [1]	CP2 [0]	0	0	CP1 [3]	CP1 [2]	CP1 [1]	CP1 [0]	0x02
Ref/Pres	0	0	0	0	PRE [1]	PRE [0]	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x03
Function	0	LDCNT SEL[1]	LDCNT SEL[0]	FAST EN	CP HiZ	CP POLA	LD	FAST [12]	FAST [11]	FAST [10]	FAST [9]	FAST [8]	FAST [7]	FAST [6]	FAST [5]	FAST [4]	FAST [3]	FAST [2]	FAST [1]	FAST [0]	0x04
GPO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPO 2	GPO 1	0x05

Notes for writing into registers

(1) The data at addresses 0x02 and 0x03 are committed to all related circuits when address 0x01 is written, which means that the data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at the same time.

(2) Addresses 0x04 and 0x05 could be written individually from other addresses.

(3) The initial register values are not defined. Therefore, even after [PDN1] is turned ON, each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

○ Examples of writing into registers

(Ex. 1) Power-On ⇒Writing these three-word data is required.

(1) Write a charge pump current value to address 0x02.
The data at address 0x02 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.

(2) Write a division number for the prescaler and a reference counter value to address 0x03.
The data at the address 0x03 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.

(3) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at this time.

(Ex. 2) Changing frequency settings

(1) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The last data written into addresses 0x02 and 0x03 are committed.

(Ex. 3) Changing charge pump current ⇒Writing these two-word data is required.

(1) Write a charge pump current value at the address 0x02.
The data in address 0x02 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.

(2) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The last data written into address 0x03 is committed.

(Ex. 4) Changing reference dividing number ⇒Writing these two-word data is required.

(1) Write a division number for the prescaler and a reference counter value at the address 0x03.
The data at the address 0x03 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.

(2) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The last data written into address 0x03 is committed.

10. Register Function Description

< Address1 : A/B >

D19	D[18:6]	D[5:0]	Address
0	B[12:0]	A[5:0]	0001

B[12:0]: B (Programmable) counters value

D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	1	3 Dec	
DATA														
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	

A[5:0]: A (Swallow) counter value

D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	
0	0	0	0	0	1	1 Dec	
0	0	0	0	1	0	2 Dec	
0	0	0	0	1	1	3 Dec	
DATA							
1	1	1	1	0	1	61 Dec	
1	1	1	1	1	0	62 Dec	
1	1	1	1	1	1	63 Dec	

*** Requirements for A[5:0] and B[12:0]**

The data at A[5:0] and B[12:0] must meet the following requirements:

B[12:0] ≥ 3, B[12:0] ≥ A[5:0]

See “1. Frequency Setup” on Page 11 for details of the relationship between a frequency division number and the data at A[5:0] and B[12:0].

< Address2 : CP >

D19	D18	D17	D16	D15	D14	D13	D12	D[11:10]	D[9:6]	D[5:4]	D[3:0]	Address
0	0	0	0	0	0	0	0	0	CP2[3:0]	0	CP1[3:0]	0010

CP1[3:0] : Charge pump current for normal operation

CP2[3:0] : Charge pump current for Fast Lock Up mode

In AK1542A, two types of charge pump current CP1 and CP2 could be set.

CP1 is the charge pump current setting for normal operation.

CP2 is the charge pump current setting for Fast Lock Up mode.

The following formula shows the relationship between the resistance value, the register setting and the electric current value.

Setting 0~7;

Charge pump minimum current (Icp_min) [A] = 8.55 / Resistance connected to the [BIAS] pin (Ω)

Charge pump current [A] = Icp_min [A] × (CP1 or CP2 + 1)

Setting 8;

Charge pump current [A] = Icp_min [A] × 0.5

CP1[3:0]	Charge pump currents [μA]		
CP2[3:0]	22kΩ	27kΩ	33kΩ
000	388	316	259
001	776	632	518
010	1164	948	777
011	1552	1264	1036
100	1940	1580	1295
101	2328	1896	1554
110	2716	2212	1813
111	3104	2528	2072
1XXX	194	158	129

< Address3 : Ref/Pres >

D19	D18	D17	D16	D[15:14]	D[13:0]	Address
0	0	0	0	PRE[1:0]	R[13:0]	0011

PRE[1:0] : Prescaler division ratio (8/9, 16/17, 32/33)

The following settings can be chosen for the prescaler division.

D15	D14	Function	Remarks
0	0	8/9 (P=8)	
0	1	16/17 (P=16)	
1	0	32/33 (P=32)	
1	1	Prohibited	

R[13:0]: Reference clock division number

The following settings can be chosen for the reference clock division.

The allowed range is 4 (1/4 division) to 16383 (1/16383 division).

0 to 3 cannot be set.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1/1 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1/2 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1/3 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1/4 division	
DATA															
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1/16381 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1/16382 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1/16383 division	

< Address4 : Function >

D19	D18	D17	D16	D15	D14	D13	D[12:0]	Address
0	LDCNT SEL[1]	LDCNT SEL[0]	FAST EN	CP HiZ	CP POLA	LD	FAST[12:0]	0100

LDCNTSEL[1:0] : Counter value for lock detect

The counter value for digital lock detect can be set.

D18	D17	Function	Remarks
0	0	Counter value = 7	
0	1	Counter value = 15	
1	0	Counter value = 31	
1	1	Counter value = 63	

FASTEN : The Fast Lock Up mode enable/disable setting

The Fast Lock Up mode can be enabled or disabled.

D16	Function	Remarks
0	The data in CP2[3:0] and FAST[12:0] are disabled.	
1	The data in CP2[3:0] and FAST[12:0] are enabled.	

CPHIZ: TRI-STATE output setting for charge pumps 1 and 2

D15	Function	Remarks
0	Charge pump is activated.	Use this setting for normal operation.
1	TRI-STATE	Note 1)

Note 1) The charge pump output is turned OFF and put in the Hi-Z state.

CPPOLA: Selects positive or negative output polarity for CP1 and CP2.

D14	Function	Remarks
0	Positive	
1	Negative	

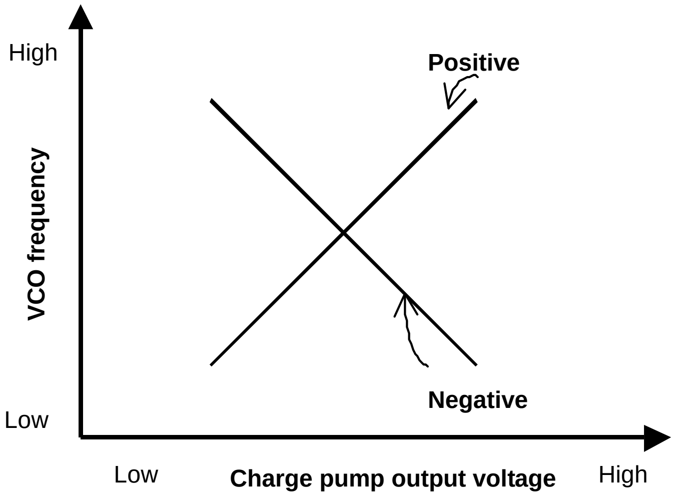


Fig. 11 Charge Pump Output Polarity

LD: Selects analog or digital for Lock Detect.

D13	Function	Remarks
0	Digital lock detect mode	
1	Analog lock detect mode	

For detailed functional descriptions, see the section “Lock Detect (LD) Signal” in “8. Block Functional Description”.

FAST[12:0] : FAST counter value

A decimal number from 1 to 8191 can be set. This value determines the time period during which the CP2 is ON for the Fast Lock Up mode.

After the time period calculated by [phase detector frequency cycle × {FAST[12:0]} setting], the CP2 is turned OFF.

0 could not be set.

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	
DATA														
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	

< Address5 : GPO >

D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPO2	GPO1	0101

GPO2: The state of the GPO2 pin

This value controls the General-Purpose output pin GPO2.

The voltage applied to the PVDD pin determines the “High” level output.

D1	Function	Remarks
0	“Low” output from the GPO2 pin	
1	“High” output from the GPO2 pin	

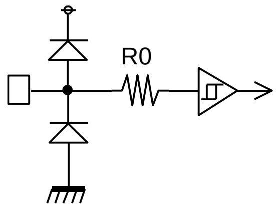
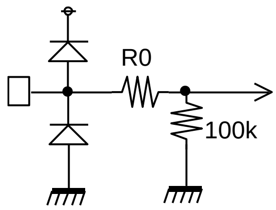
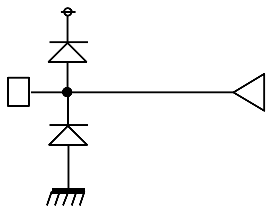
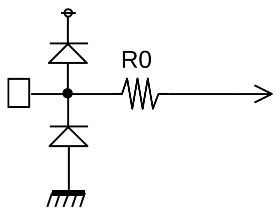
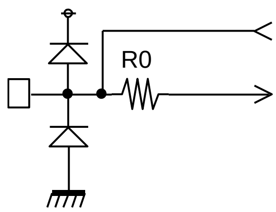
GPO1: The state of the GPO1 pin

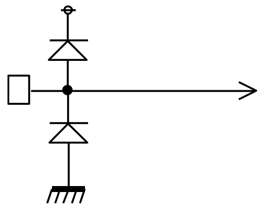
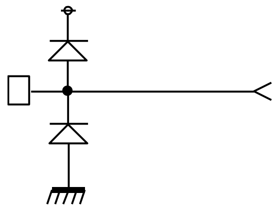
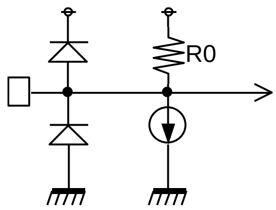
This value controls the General-Purpose output pin GPO1.

The voltage applied to the PVDD pin determines the “High” level output.

D0	Function	Remarks
0	“Low” output from the GPO1 pin	
1	“High” output from the GPO1 pin	

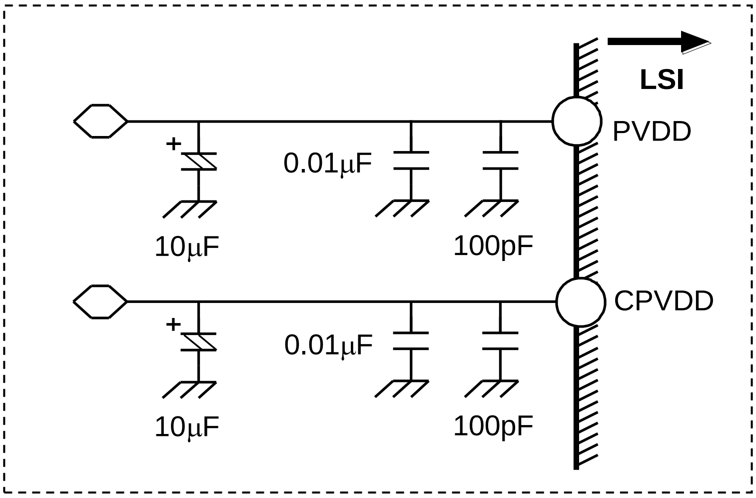
11. IC Interface Schematic

No.	Name	I/O	R0(Ω)	Cur(μA)	Function
4	LE	I	300		**Digital input pins** 
5	DATA	I	300		
6	CLK	I	300		
8	PDN2	I	300		
9	PDN1	I	300		
2	TEST3	I	300		**Digital input pins Pull-Down** 
3	TEST1	I	300		
11	TEST2	I	300		
7	LD	O			**Digital output pin** 
12	GPO1	O			
13	GPO2	O			
10	REFIN	I	300		**Analog input pin** 
15	VREF	IO	300		**Analog I/O pin** 
19	BIAS	IO	300		
22	CPZ	IO	300		

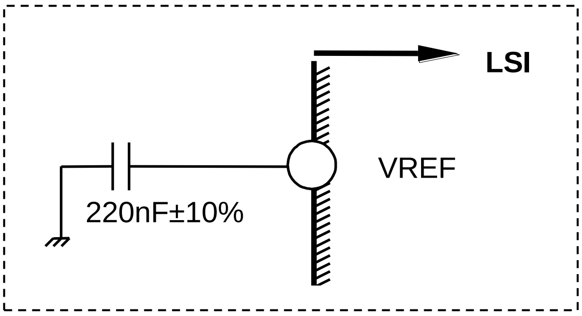
<table>
<tr><th>No.</th><th>Name</th><th>I/O</th><th>R0(Ω)</th><th>Cur(μA)</th><th>Function</th></tr>
<tr><td>23</td><td>SWIN</td><td>I</td><td></td><td></td><td rowspan="2">Analog input pin
</td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>21</td><td>CP</td><td>O</td><td></td><td></td><td rowspan="2">Analog output pin
</td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>16</td><td>RFINN</td><td>I</td><td>12k</td><td>20</td><td rowspan="3">Analog input pin(RF signal input)

</td></tr>
<tr><td>17</td><td>RFINP</td><td>I</td><td>12k</td><td>20</td></tr>
<tr><td colspan="5"></td></tr>
</table>

12. Recommended Schematic for Off-Chip Component

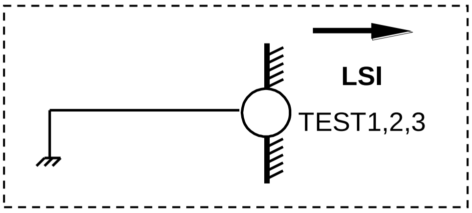
1. PVDD, CPVDD



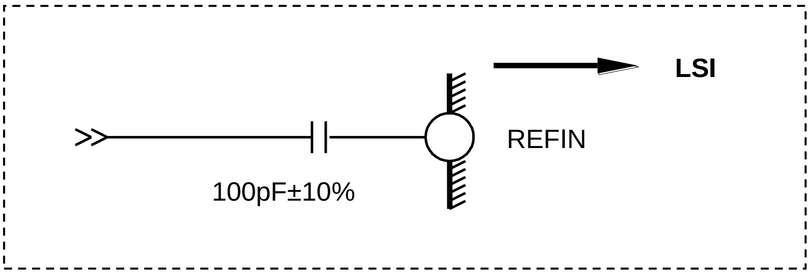
2. VREF



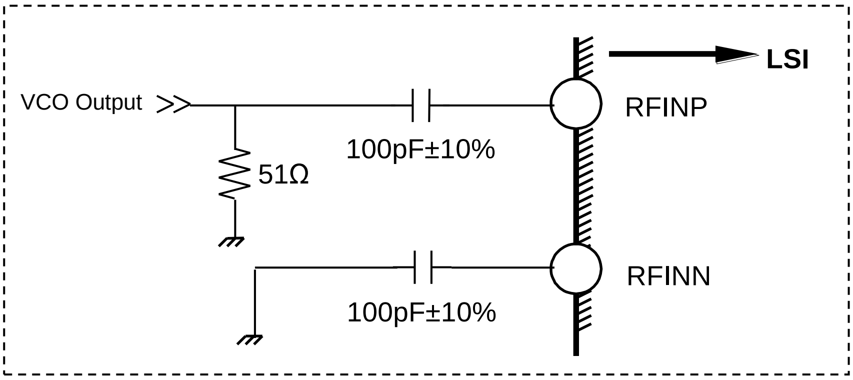
3. TEST [1,2,3]



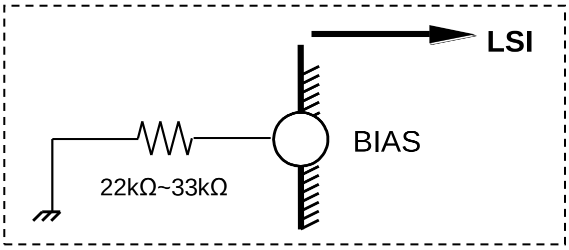
4. REFIN



5. RFINP, RFINN



6. BIAS



13. Power-up Sequence

1. Power-up Sequence (Recommended)

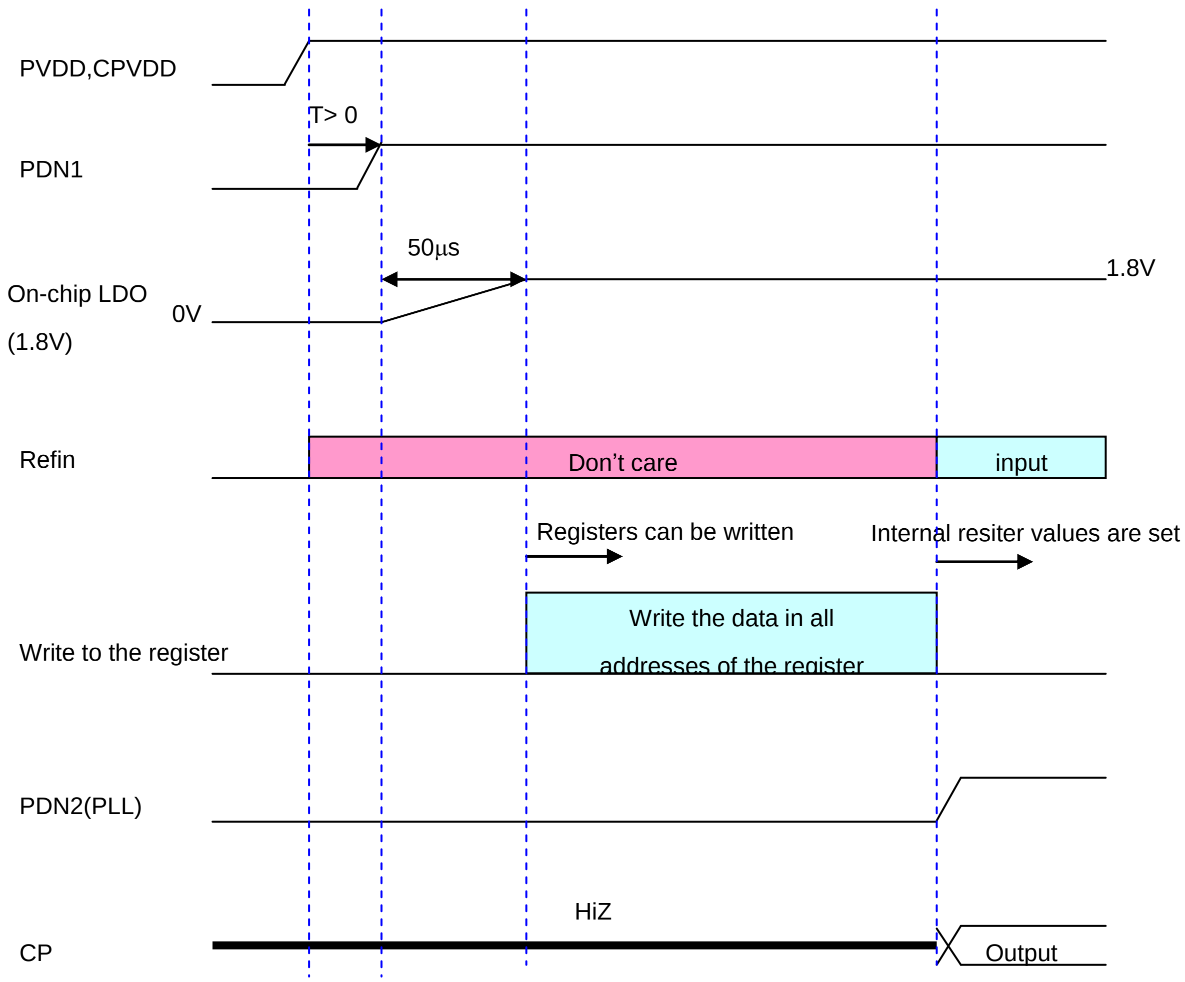


Fig. 12 Recommended Power Sequence

Note 1) The initial register values are not defined. Therefore, even after [PDN1] is set to "High", each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

2. Power-up Sequence

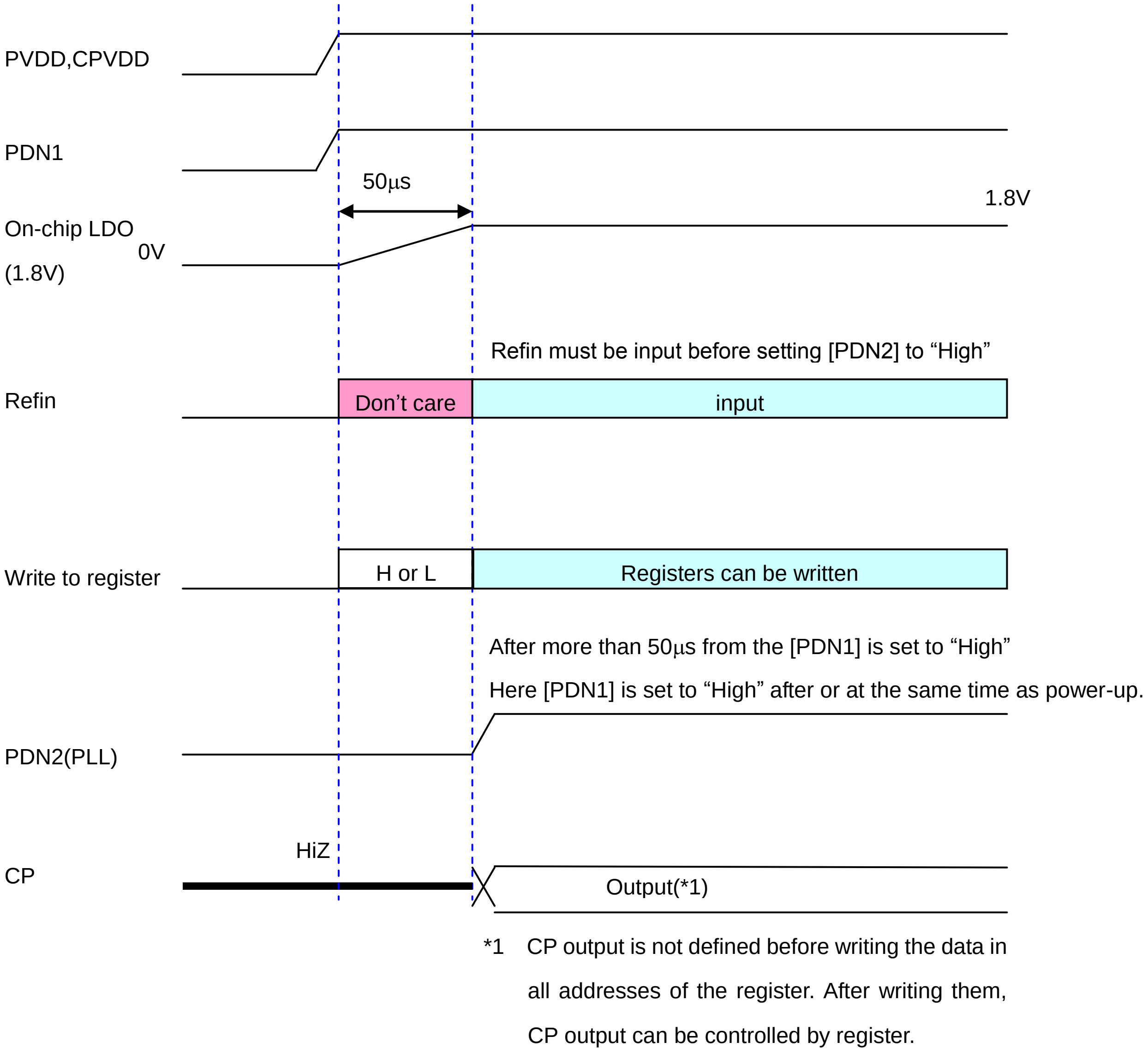


Fig. 13 Power Sequence

14. Typical Evaluation Board Schematic

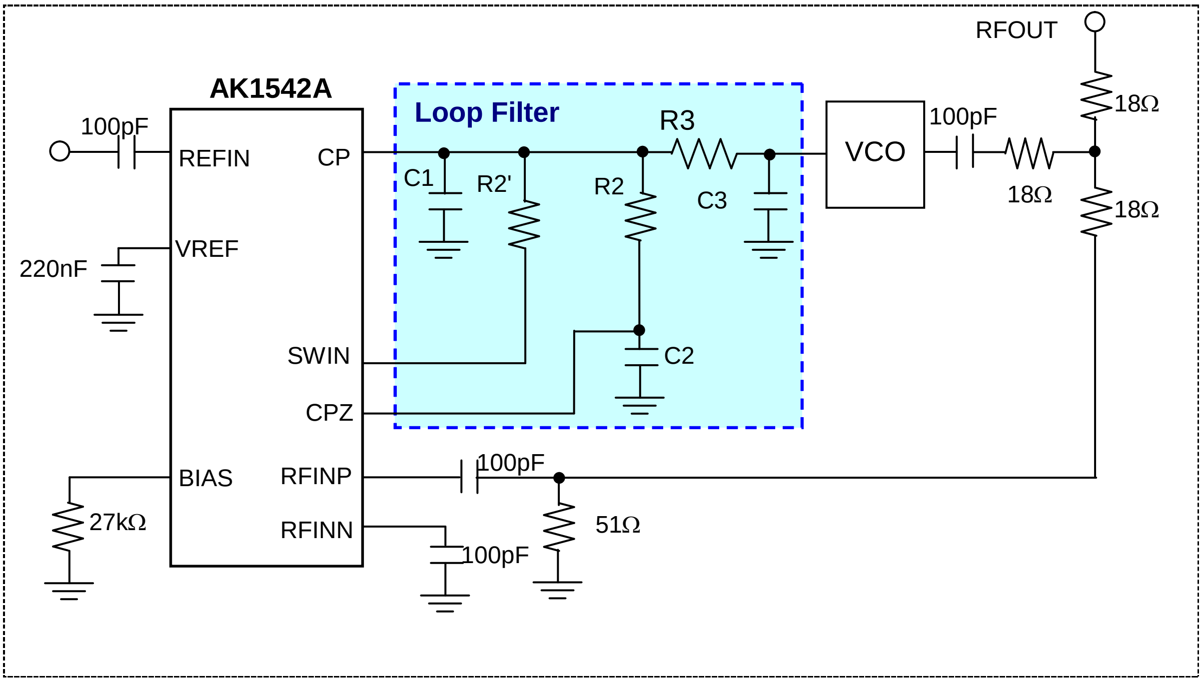


Fig. 14 Typical Evaluation Board Schematic

Note 1) The [CPZ] pin should be connected to the R2 and C2, which are intermediate nodes, even if the Fast Lock Up is not used. Therefore, R2 must be connected to the [CP] pin, while C2 must be connected to the ground.

Note 2) In Fast Lock Up mode, R2 and R2' are connected in parallel by internal switching. For calculation of loop band width and phase margin at Fast Lock Up mode, the resistance should be considered as parallel of R2 and R2'.

Note 3) It is recommended that the exposed pad at the center of the backside should be connected to the ground.

Note 4) Test pins (TEST1 to 3) should be connected to the ground.

15. Block Diagram by Power Supply

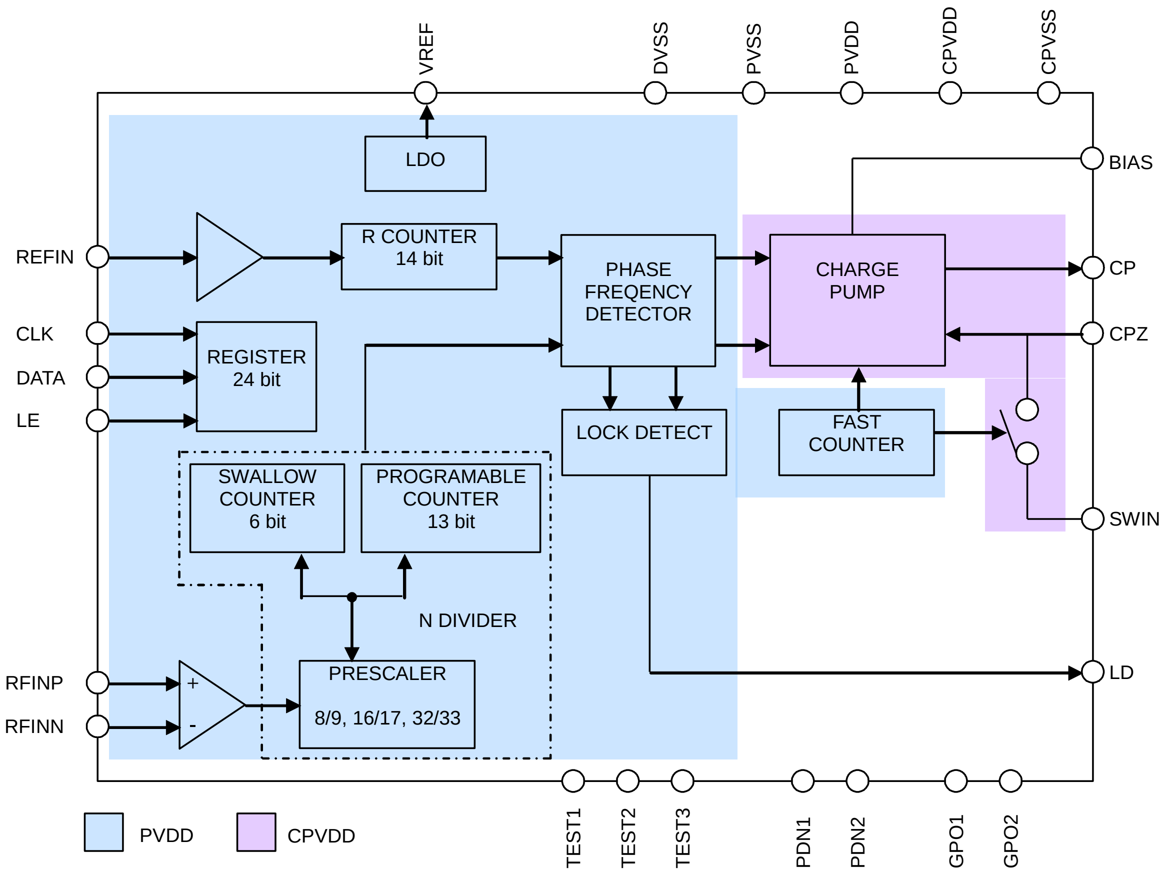


Fig. 15 Power Supply Block Diagram

16. Outer Dimensions

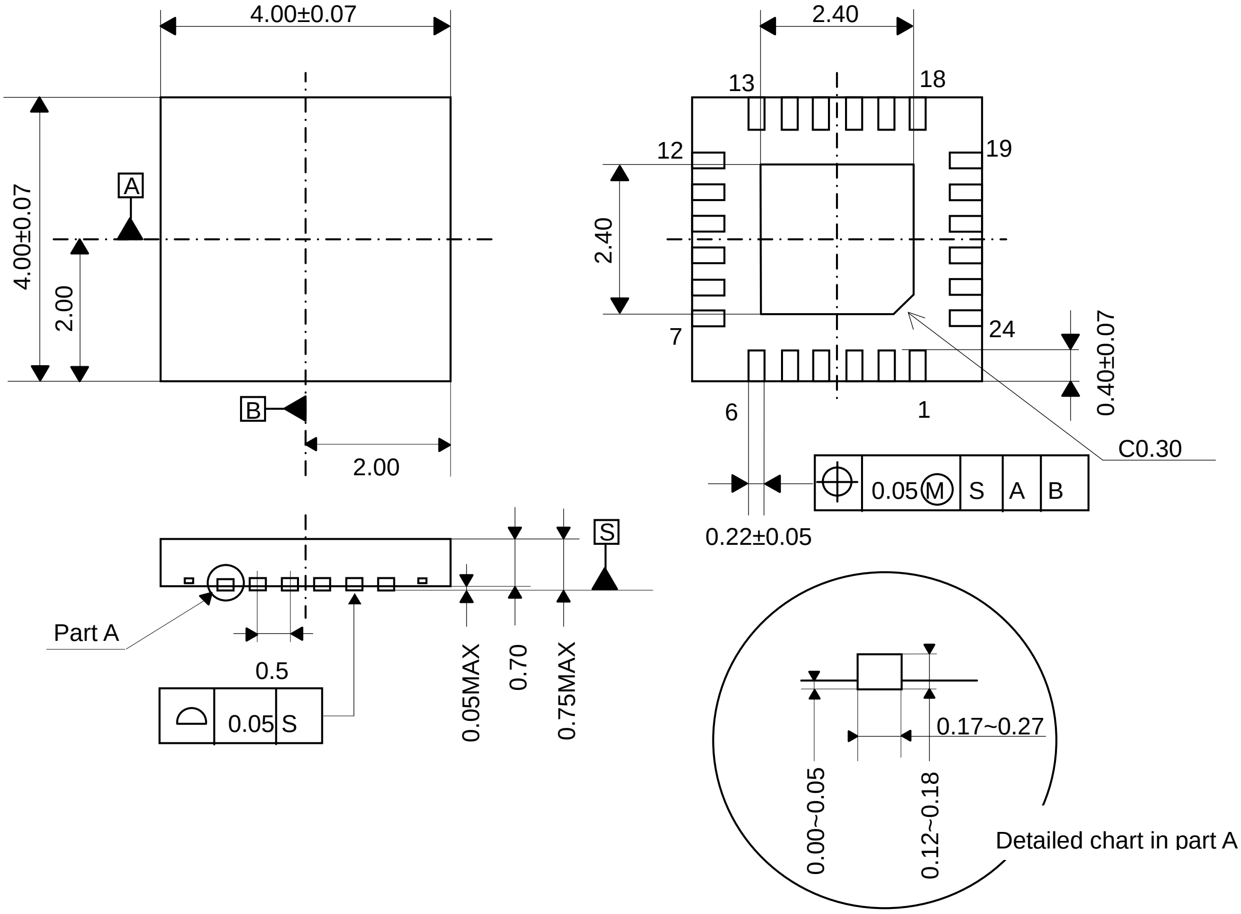


Fig. 16 Package Outer Dimensions

Note) It is recommended to connect the exposed pad at the center of the backside to the ground, although it will not make any impact on the electrical characteristics if it is open.

17. Marking

(a) Style	:	QFN
(b) Number of pins	:	24
(c) 1 pin marking:	:	○
(d) Product number	:	1542A
(e) Date code	:	YWWL (4 digits)

Y	:	Lower 1 digit of calendar year (Year 2012 → 2, 2013 → 3 ...)
WW	:	Week
L	:	Lot identification, given to each product lot which is made in a week
		→ LOT ID is given in alphabetical order (A, B, C…).

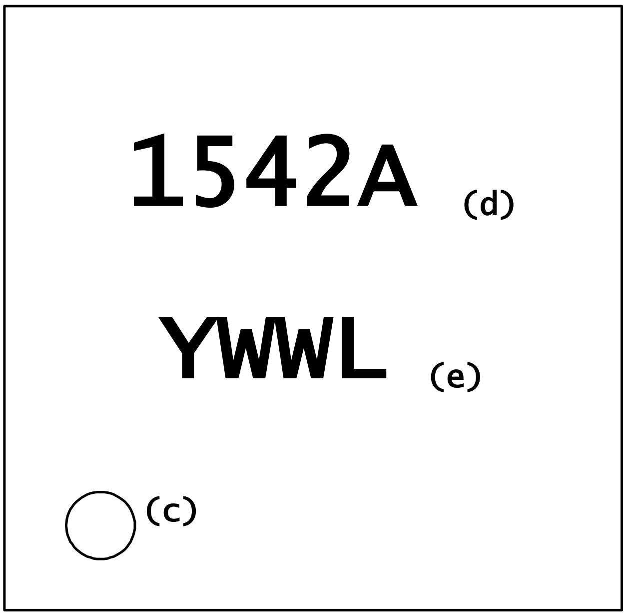


Fig. 17 Marking