Am9016

16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Low maximum power dissipation – 462mW active, 20mW standby
- High speed operation – 150ns access, 320ns cycle
- ±10% tolerance on standard +12, +5, –5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

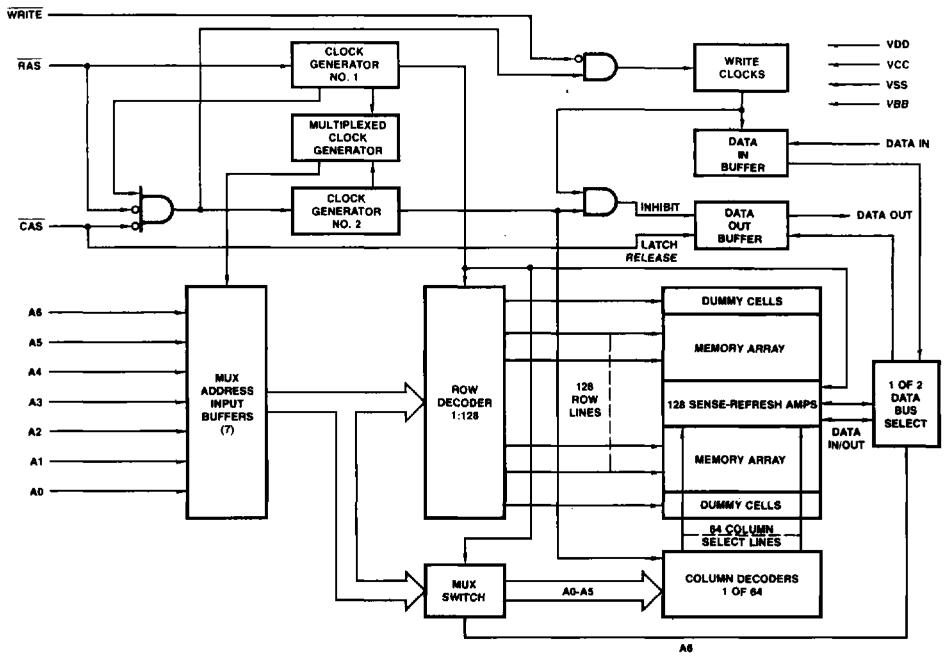
GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM

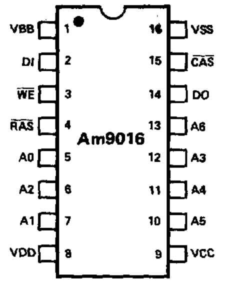


MOS-190

ORDERING INFORMATION

Ambient Temperature	Package Type	Access Time			
		300ns	250ns	200ns	150ns
$0°C \leq T_A \leq +70°C$	Hermetic DIP	AM9016CDC	AM9016DDC	AM9016EDC	AM9016FDC
	Molded DIP	AM9016CPC	AM9016DPC	AM9016EPC	AM9016FPC

CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

A0 – A6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
$\overline{WE}$	WRITE ENABLE

MOS-191

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	–65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
Voltage on Any Pin Relative to VBB	–0.5V to +20V
VDD and VCC Supply Voltages with Respect to VSS	–1.0V to +15.0V
VBB – VSS (VDD – VSS > 0V)	0V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
$0°C \leq T_A \leq +70°C$	+12V ±10%	+5V ±10%	0	–5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description		Test Conditions	Am9016X Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage		IOH = –5.0mA	2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA	VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In			2.4		7.0	Volts
VIHC	Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$			2.7		7.0	Volts
VIL	Input LOW Voltage			–1.0		0.80	Volts
IIX	Input Load Current		VSS ≤ VI ≤ 7V	–10		10	μA
IOZ	Output Leakage Current		VSS ≤ VO ≤ VCC, Output OFF	–10		10	μA
ICC	VCC Supply Current		Output OFF (Note 4)	–10		10	μA
IBB	VBB Supply Current, Average		Standby, $\overline{RAS}$ ≥ VIHC			100	μA
			Operating, Minimum Cycle Time			200	
IDD	VDD Supply Current, Average	Operating IDD1	$\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times			35	mA
		Page Mode IDD4	$\overline{RAS}$ ≤ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times			27	
		$\overline{RAS}$ Only Refresh IDD3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ VIHC, Minimum Cycle Times			27	
		Standby IDD2	$\overline{RAS}$ ≥ VIHC			1.5	
CI	Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Inputs at 0V, f = 1MHz, Nominal Supply Voltages			10	pF
		Address, Data In				5.0	
CO	Output Capacitance		Output OFF			7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

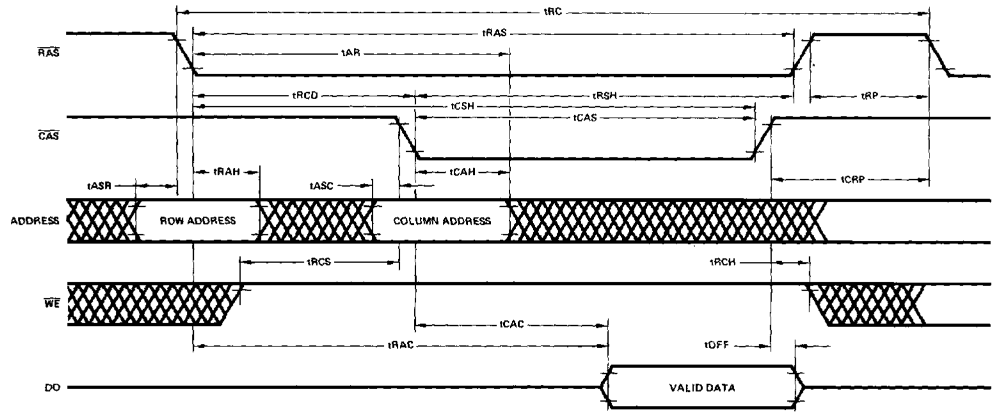
Parameters	Description	Am9016C		Am9016D		Am9016E		Am9016F		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tAR	RAS LOW to Column Address Hold Time	200		160		120		95		ns
tASC	Column Address Set-up Time	−10		−10		−10		−10		ns
tASR	Row Address Set-up Time	0		0		0		0		ns
tCAC	Access Time from CAS (Note 6)		185		165		135		100	ns
tCAH	CAS LOW to Column Address Hold Time	85		75		55		45		ns
tCAS	CAS Pulse Width	185	10,000	165	10,000	135	10,000	100	10,000	ns
tCP	Page Mode CAS Precharge Time	100		100		80		60		ns
tCRP	CAS to RAS Precharge Time	−20		−20		−20		−20		ns
tCSH	CAS Hold Time	300		250		200		150		ns
tCWD	CAS LOW to WE LOW Delay (Note 9)	145		125		95		70		ns
tCWL	WE LOW to CAS HIGH Set-up Time	100		85		70		50		ns
tDH	CAS LOW or WE LOW to Data In Valid Hold Time (Note 7)	85		75		55		45		ns
tDHR	RAS LOW to Data In Valid Hold Time	200		160		120		95		ns
tDS	Data In Stable to CAS LOW or WE LOW Set-up Time (Note 7)	0		0		0		0		ns
tOFF	CAS HIGH to Output OFF Delay	0	60	0	60	0	50	0	40	ns
tPC	Page Mode Cycle Time	295		275		225		170		ns
tRAC	Access Time from RAS (Note 6)		300		250		200		150	ns
tRAH	RAS LOW to Row Address Hold Time	45		35		25		20		ns
tRAS	RAS Pulse Width	300	10,000	250	10,000	200	10,000	150	10,000	ns
tRC	Random Read or Write Cycle Time	460		410		375		320		ns
tRCD	RAS LOW to CAS LOW Delay (Note 6)	35	115	35	85	25	65	20	50	ns
tRCH	Read Hold Time	0		0		0		0		ns
tRCS	Read Set-up Time	0		0		0		0		ns
tREF	Refresh Interval		2		2		2		2	ms
tRMW	Read Modify Write Cycle Time	600		500		405		320		ns
tRP	RAS Precharge Time	150		150		120		100		ns
tRSH	CAS LOW to RAS HIGH Delay	185		165		135		100		ns
tRWC	Read/Write Cycle Time	525		425		375		320		ns
tRWD	RAS LOW to WE LOW Delay (Note 9)	260		210		160		120		ns
tRWL	WE LOW to RAS HIGH Set-up Time	100		85		70		50		ns
tT	Transition Time	3	50	3	50	3	50	3	35	ns
tWCH	Write Hold Time	85		75		55		45		ns
tWCR	RAS LOW to Write Hold Time	200		160		120		95		ns
tWCS	WE LOW to CAS LOW Set-up Time (Note 9)	−20		−20		−20		−20		ns
tWP	Write Pulse Width	85		75		55		45		ns

NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both RAS and CAS must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on RAS and tRAC governs. When tRCD is more than the maximum value shown access time depends on CAS and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of CAS or WE.
8. At least eight initialization cycles that exercise RAS should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of WE follows the falling edge of CAS by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of WE follows the falling edges of RAS and CAS by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of WE may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

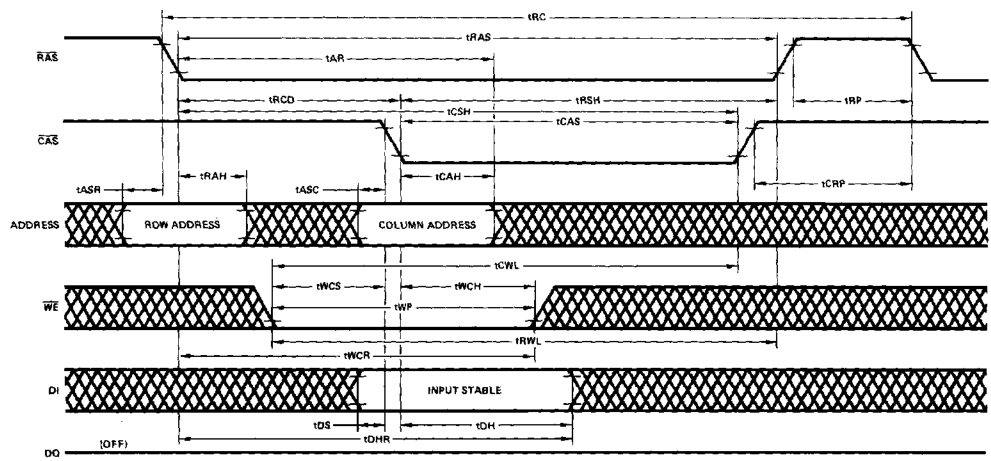
SWITCHING WAVEFORMS

READ CYCLE



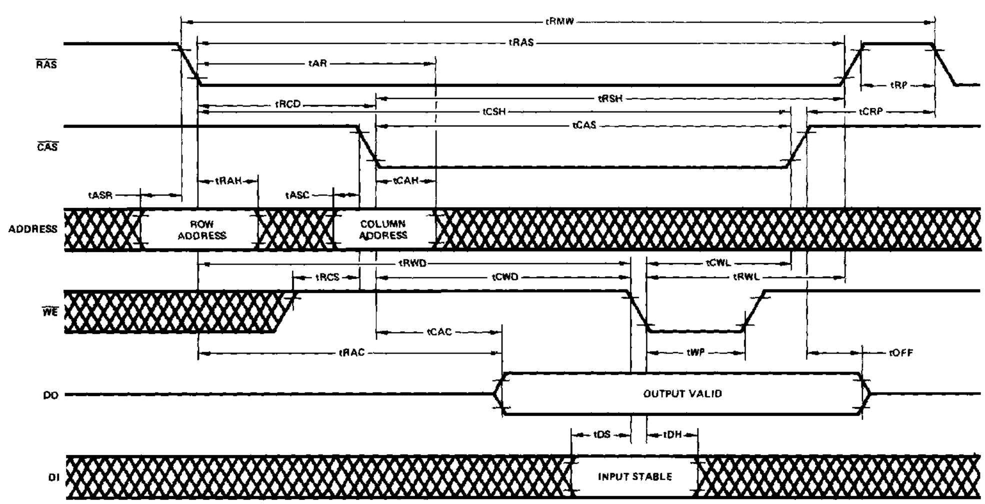
MOS-192

WRITE CYCLE (EARLY WRITE)



MOS-193

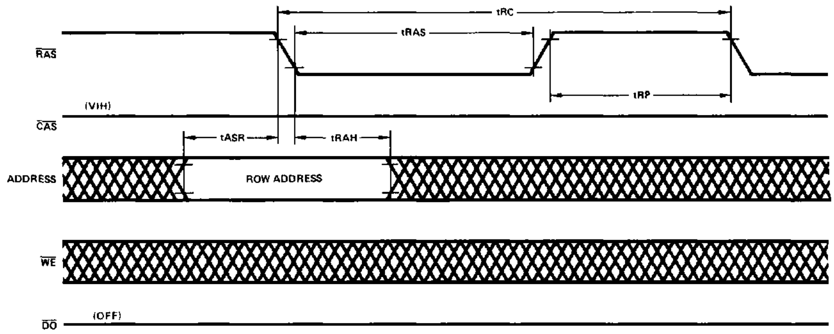
READ-WRITE/READ-MODIFY-WRITE CYCLE



MOS-194

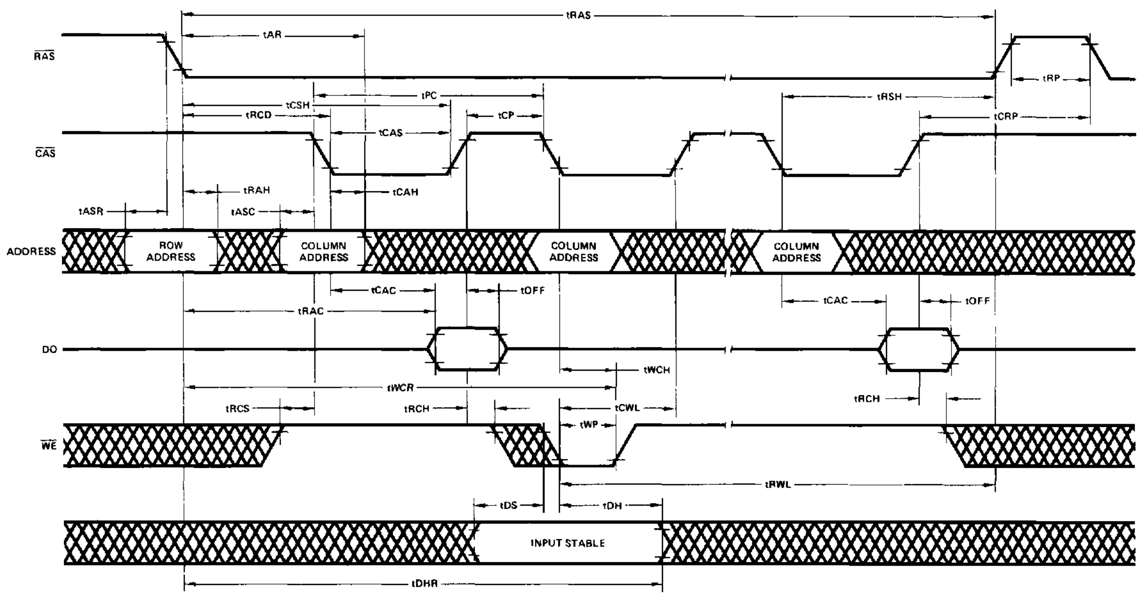
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



MOS-195

PAGE MODE CYCLE



MOS-196

APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{\text{WE}}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{\text{RAS}}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{\text{CAS}}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{\text{CAS}}$ is low.
4) $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{\text{WE}}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{\text{WE}}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{\text{WE}}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{\text{WE}}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{\text{RAS}}$ before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{\text{RAS}}$) enters the row address bits and the Column Address Strobe ($\overline{\text{CAS}}$) enters the column address bits.

When $\overline{\text{RAS}}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{\text{RAS}}$ low while $\overline{\text{CAS}}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{\text{RAS}}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{\text{RAS}}$-only" cycles. Since only the rows need to be addressed, $\overline{\text{CAS}}$ may be held high while $\overline{\text{RAS}}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is low. The later negative transition of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ strobes the data into the internal register. In a write cycle, if the $\overline{\text{WE}}$ input is brought low prior to $\overline{\text{CAS}}$, the data is strobed by $\overline{\text{CAS}}$, and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{\text{WE}}$.

In the read cycle the data is read by maintaining $\overline{\text{WE}}$ in the high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{\text{CAS}}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{\text{CAS}}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{\text{WE}}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

POWER CONSIDERATIONS

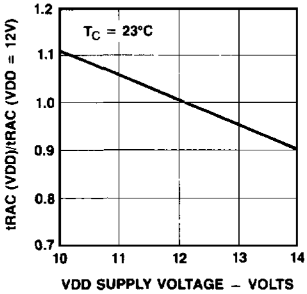
$\overline{\text{RAS}}$ and/or $\overline{\text{CAS}}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{\text{RAS}}$ is used for this purpose. The devices which do not receive $\overline{\text{RAS}}$ will be in low power standby mode regardless of the state of $\overline{\text{CAS}}$.

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

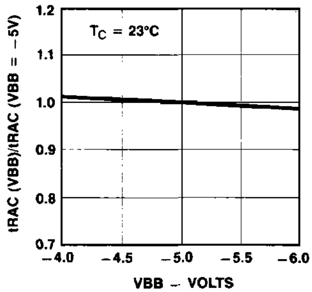
2

TYPICAL CHARACTERISTICS

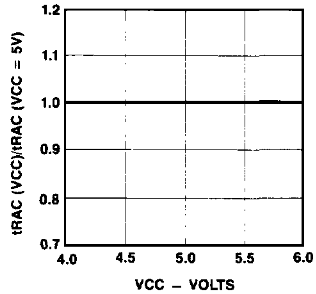
Typical Access Time (Normalized) tRAC Versus VDD



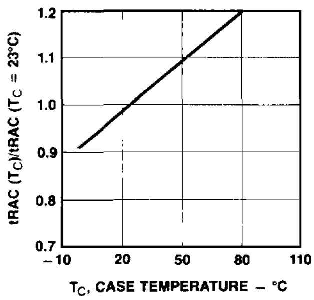
Typical Access Time (Normalized) tRAC Versus VBB



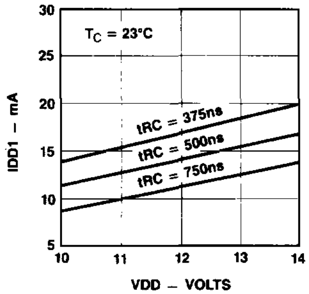
Typical Access Time (Normalized) tRAC Versus VCC



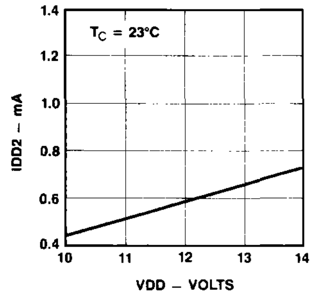
Typical Access Time (Normalized) tRAC Versus Case Temperature



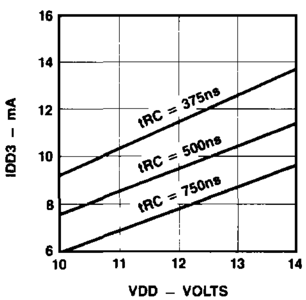
Typical Operating Current IDD1 Versus VDD



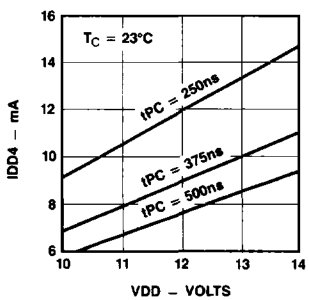
Typical Standby Current IDD2 Versus VDD



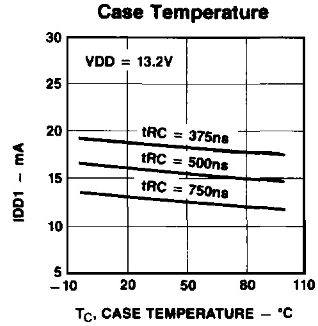
Typical Refresh Current IDD3 Versus VDD



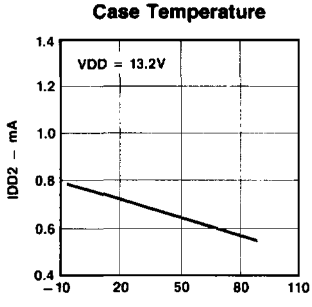
Typical Page Mode Current IDD4 Versus VDD



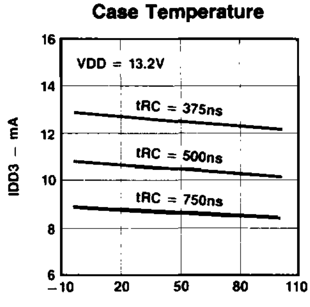
Typical Operating Current IDD1 Versus Case Temperature



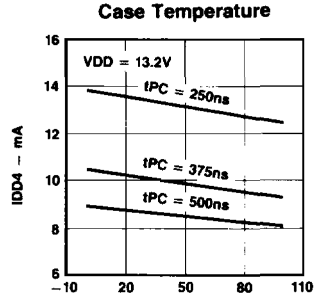
Typical Standby Current IDD2 Versus Case Temperature



Typical Refresh Current IDD3 Versus Case Temperature



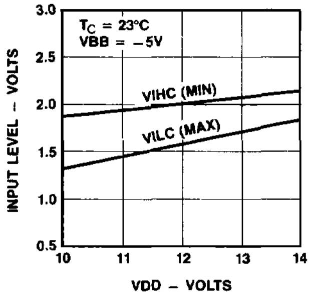
Typical Page Mode Current IDD4 Versus Case Temperature



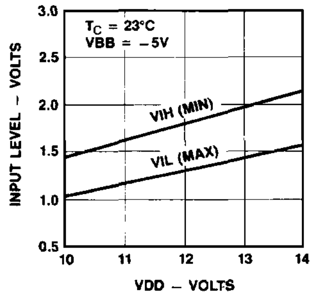
MOS-197

TYPICAL CHARACTERISTICS (Cont.)

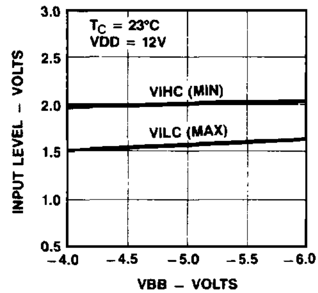
Input Voltage Levels Versus VDD



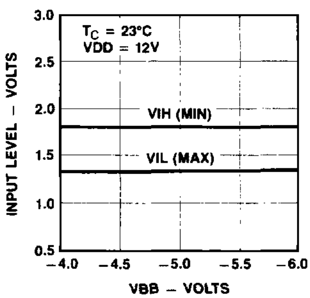
Input Voltage Levels Versus VDD



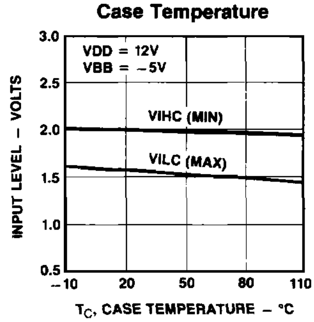
Input Voltage Levels Versus VBB



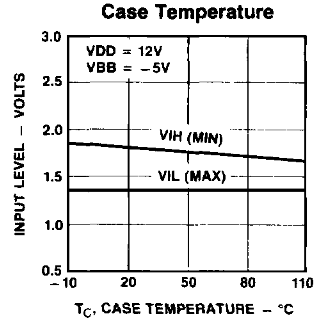
Input Voltages Levels Versus VBB



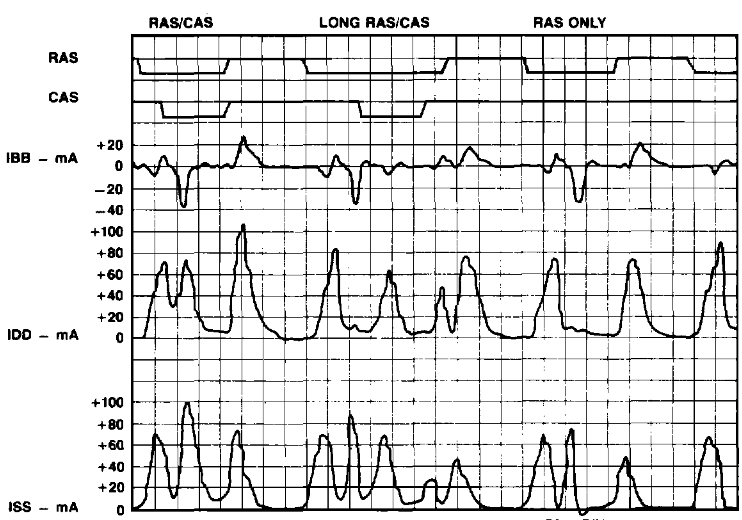
Input Voltage Levels Versus Case Temperature



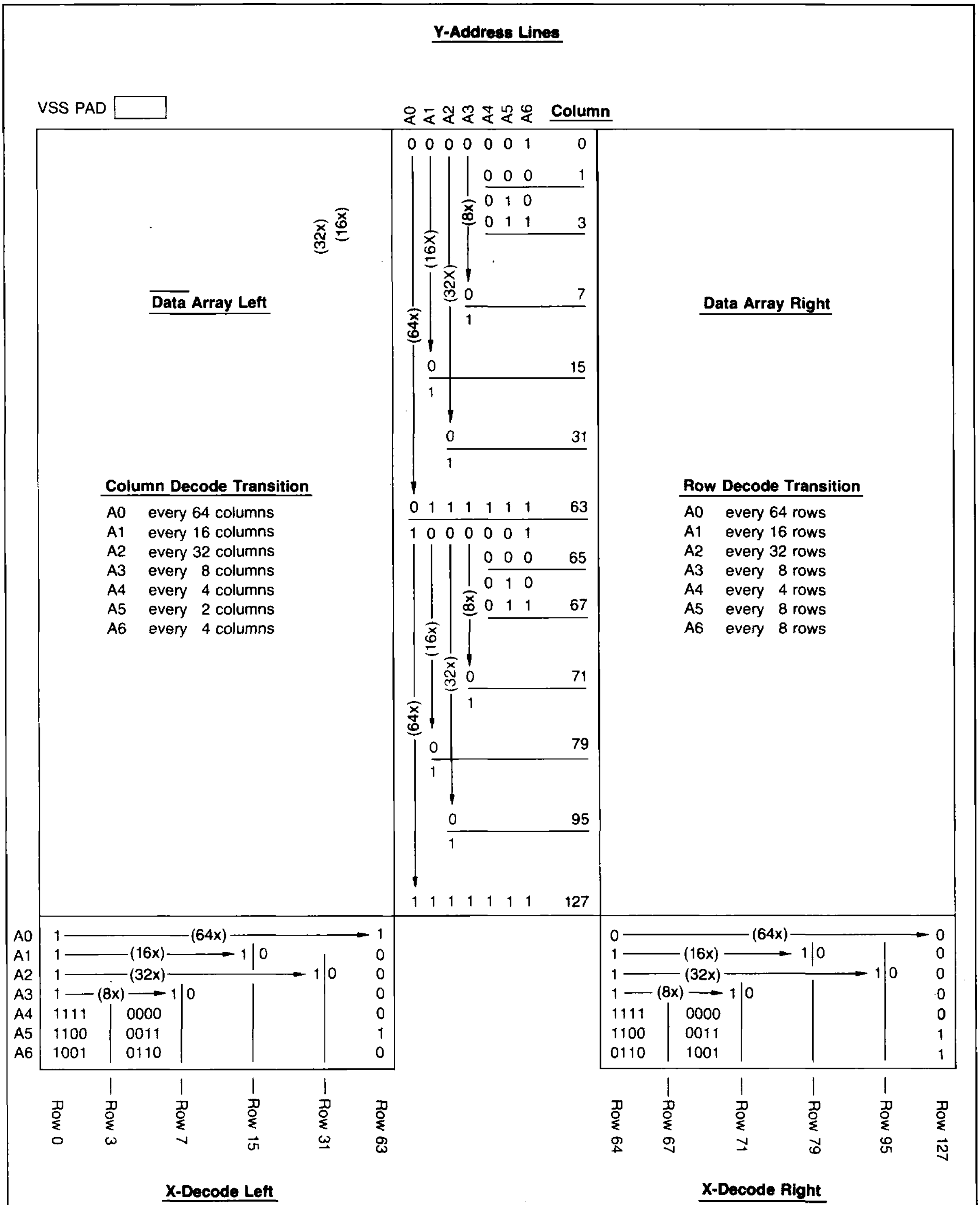
Input Voltage Levels Versus Case Temperature



TYPICAL CURRENT WAVEFORMS

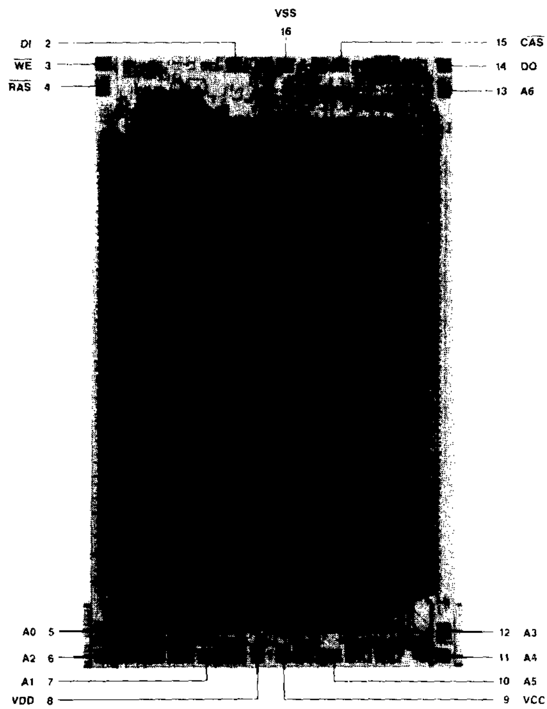


MOS-196



TOPOLOGICAL BIT MAP

Metallization and Pad Layout



DIE SIZE 0.106" X 0.205"