

Biasing Circuits and Considerations for GaAs MESFET Power Amplifiers

Summary

In order to properly use any amplifier it is necessary to provide the correct operating environment, especially the DC bias. This application note outlines some of the considerations for biasing MESFET amplifiers. Items considered herein are:

- Constant current operation,
- Temperature compensation of the biasing network, and
- Power sequencing of the applied voltages.

Overview

The I-V curves of Figure 1 represent a typical MESFET device in a common source configuration. For a typical device operating in Class A the desired current is 50% of the maximum current for any particular part. Typical MESFET devices are depletion mode, meaning that the highest drain-source current occurs for a gate voltage of approximately zero (Vgg \sim +0.5 V). As the gate voltage becomes more negative, the device current drops and eventually approaches zero at the pinch-off voltage. The two main variables in the production of MESFET power amplifiers are the maximum current and the pinch-off voltage. Since the operating voltage is assumed to be fixed by the available voltages in the system, it is the drain current that should be monitored and controlled in order to provide consistent performance from unit to unit.



Figure 1. IV characteristics of a typical MESFET device.

The schematic of Figure 2 is a simplified representation of a circuit that provides constant drain current bias for MESFET amplifiers. Since MESFETs are voltage controlled, the amount of gate current is quite low. An exception to this condition occurs under conditions of high-level RF drive where the gate current increases and eventually changes sign.



Figure 2. Simple constant current circuit for use with MESFET amplifiers.

In this circuit a reference voltage is established by the simple resistive voltage divider consisting of R1 and R2. The voltage across R1 should be equal to the voltage drop across R3 plus the emitter-base voltage of Q2 (typically 0.6 - 0.7 Volts). The actual current flowing through the PNP transistor is quite modest, typically only 1 mA. The circuit constantly adjusts the gate voltage of the amplifier in order to maintain the voltage at the base of Q2 such that it equals the reference voltage. This has the effect of holding the current through R3 constant.

The designer must also consider some tradeoffs concerning the available voltages and the choice of resistors such as R3. As an example, consider the RFS1003 with a desired operating point of 7V, 400 mA. Since the RFS1003 has a desired operating voltage of 7V, it is generally desirable to restrict R3 to small values. Selecting R3 to be 1 ohm, and neglecting the 1 mA flowing through Q2 would require a supply voltage of approximately 7.4 volts. This also sets the voltage at the base of Q2 to be approximately 6.3 Volts, and allows the resistor values in the voltage divider to be easily calculated. Typically the voltage divider would be set to have approximately 1 mA of current flowing through it.

The value of R4 can be calculated by knowing that the typical gate voltage for operation is -1.1 Volts. Assuming that the negative voltage available is -2 V, and setting the current flowing through Q2 to 1 mA results in a value of approximately 900 Ohms.

This biasing circuit works well for room temperature operation, but has the disadvantage that the baseemitter voltage of Q2 will change with temperature, even if the reference voltage is held constant. This can be overcome by the addition of another PNP transistor to form a matched pair. It is important that these transistors be well matched, operating at the same bias, and in the same thermal environment. The schematic of Figure 3 is a refinement of the basic circuit that incorporates temperature compensation as well as several other features. The user does not need to implement all of the functions, but they are shown here for illustrative purposes.

The main features of this circuit are:

- Constant Operating Current
- Reduction of Part-to-Part Variation
- Temperature Compensation
- Negative Voltage Generator
- Power Sequencing (Negative before positive)



Figure 3. Schematic for a Negative Bias Generator.

The Maxim MAX881 voltage inverter is shown in its standard configuration. This provides the negative voltage necessary for the gates of the amplifier. The Maxim part works from supply voltages (V) of 2.5 to

5.5 volts. The capacitors listed in the bill of materials (BOM) are those used by Maxim in their application circuit. Other choices are possible, depending upon the ripple requirements. In this application the output voltage was set to -2V.

The Shutdown pin is active low (pull it to ground for the circuit to operate).

Power sequencing is very important in order to assure that the amplifier is not overstressed. From the IV curves it can be observed that if the drain voltage were to be applied first, while the gate voltage remained at 0V, then the current through the device would be at its maximum, roughly double the nominal value. Instead, the negative voltage should be applied first, which holds the FETs pinched off to keep power dissipation low until the drain voltage reaches its desired value. R5 is a pull-up resistor that holds FET Q3 off when the circuit is off (Shutdown = High). The Maxim part monitors the output voltage during power-up, and sets /POK low when the negative voltage has reached 92% of its final value. Setting /POK low turns on FET Q3, which safely powers up the rest of the circuit.

Example: Biasing the RFS1006

If the input voltage is 7.8V, and the desired voltage is 7.0V for the RFS1006, with an average operating current of 520 mA, then the resistor, R3, should be 1.5Ω . This value does dissipate some power (0.42W in this example). This resistor should be W and also 1% tolerance, if possible, since the bias current will change directly with the resistor value.

Resistor R2 sets the bias current through Q1, which is the supply voltage minus the drop across R3 and the V_{EB} (0.7V) of Q2. With a bias of 1 mA, and neglecting base currents, the closest standard value of R2 is 6.34 k Ω . Selecting a bias current of 1 mA for Q2 determines the value of R4 (909 Ω is the closest 1% standard value).

Transistor Q1 forms part of the temperature compensation/current mirror. Biasing it to 1 mA, and setting the base voltage equal to that of Q2, the voltage drop across R1 should be the same as that across R3. This resistor should be 806Ω .

In some cases only a maximum of 7V will be available to run the ANADIGICS power amplifier. Since resistor R3 will introduce a voltage drop, it should be made as small as possible, on the order of 0.1 Ohms. This will cause only a negligible voltage drop of approximately 50 mV, allowing the amplifier to achieve nearly its full output power. Resistor R1 will need to be resized accordingly. The disadvantage to this approach is that it is more sensitive to the resistor values.

In some cases it is desirable to vary the operating current of the circuit. In production this may be achieved by changing the value of R1. In a lab environment, this can be achieved through the use of a small potentiometer in series with R1.

Conclusion

A simple method for achieving consistent amplifier operation has been presented. For additional information contact the factory.

Ref Des	Value	Description	Part No.	Manufacturer	Quantity
C1, C2, C3	1 uF	1206, 16 V, low ESR ceramic Cap	EMK316BJ105KF	Taiyo Yuden	3
C4	4.7 uF	1206, 10 V, low ESR ceramic Cap	LMK316BJ475KL	Taiyo Yuden	1
Q1/Q2	N/A	SOT-363, Dual 3906 PNP Transistor	MMDT3906TR-ND	Diodes Incorporated	1
Q3	N/A	HEXFET Power Mosfet, Low On Resistance	IRLML6401TR-ND	International Rectifier	1
R1	806 ?	0603, 1/16W, 1%	ERJ-3EKF8060V	Panasonic	1
R2	6340 ?	0603, 1/16W, 1%	ERJ-3EKF6341V	Panasonic	1
R3	1.5 ?	2512, 1 W, 5%	ERJ-1TYJ1R5U	Panasonic	1
R4	909 ?	0603, 1/16W, 1%	ERJ-3EKF9090V	Panasonic	1
R5	10 K?	0603, 1/16W, 1%	ERJ-3EKF1002V	Panasonic	1
R6	1 M?	0603, 1/16W, 1%	ERJ-3EKF1004V	Panasonic	1
U2	N/A	10 uMAX, Low - Noise Bias Supply	MAX881REUB	Maxim	1

Table 1.	Bill of Materials for Ad	ditional Functions	Illustrated in Figure 3.



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