

**Legal Disclaimer Notice**

**GENERAL DESCRIPTION**

The LT4953C is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and low in-line power loss are needed in a very small outline surface mount package.

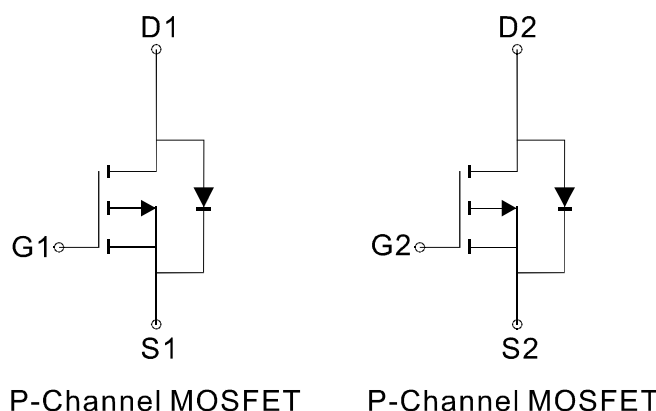
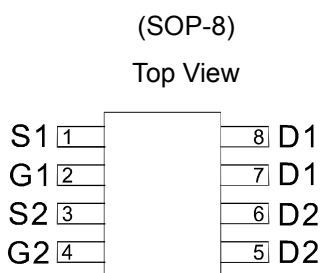
**FEATURES**

- $R_{DS(ON)} \leq 60m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 90m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

**PIN CONFIGURATION**



Ordering Information: LT4953C (Pb-free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

| Parameter                                    | Symbol          | Limit        | Unit |
|--|-----------------|--------------|------|
| Drain-Source Voltage                         | $V_{DSS}$       | -30          | V    |
| Gate-Source Voltage                          | $V_{GSS}$       | $\pm 20$     | V    |
| Continuous Drain Current (Tj=150°C)          | $I_D$           | TA=25°C      | -5.3 |
|  |                 | TA=70°C      | -4.3 |
| Pulsed Drain Current                         | $I_{DM}$        | -30          | A    |
| Continuous Source Current (Diode Conduction) | $I_S$           | -1.7         | A    |
| Maximum Power Dissipation                    | $P_D$           | TA=25°C      | 2.0  |
|  |                 | TA=70°C      | 1.3  |
| Operating Junction Temperature               | $T_J$           | -55 to 150   | °C   |
| Storage Temperature Range                    | $T_{stg}$       | -55 to 150   | °C   |
| Thermal Resistance-Junction to Ambient*      | $R_{\theta JA}$ | T ≤ 10 sec   | 47   |
|  |                 | Steady State | 75   |
| Thermal Resistance-Junction to Case          | $R_{\theta JC}$ | 45           | °C/W |

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

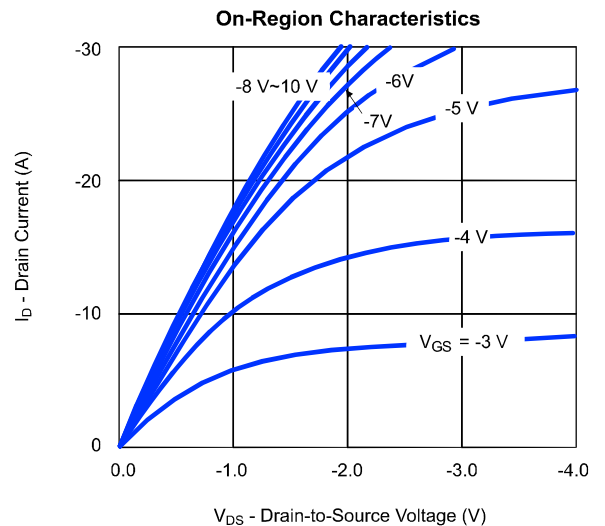
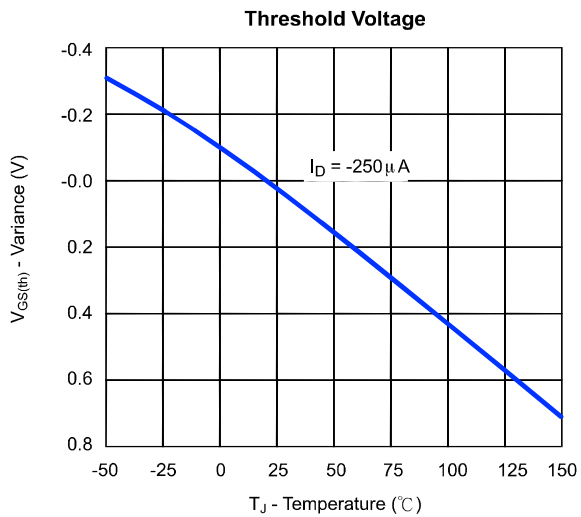
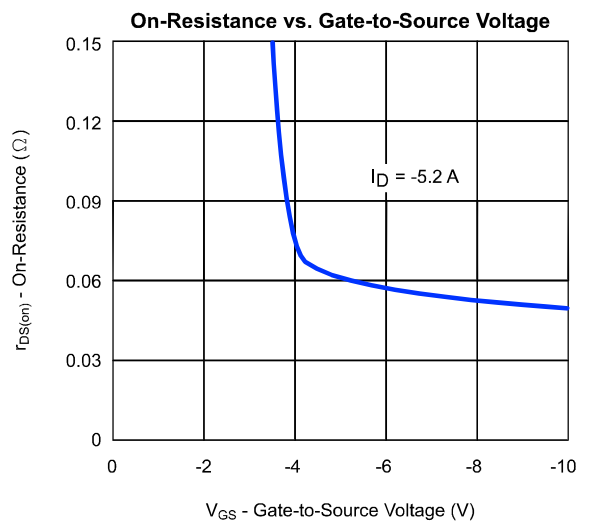
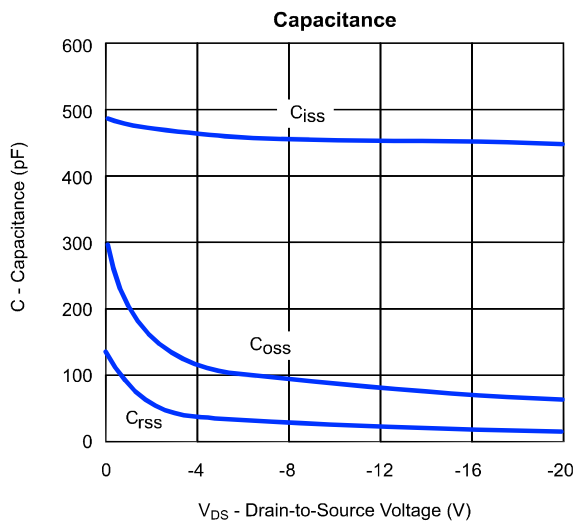
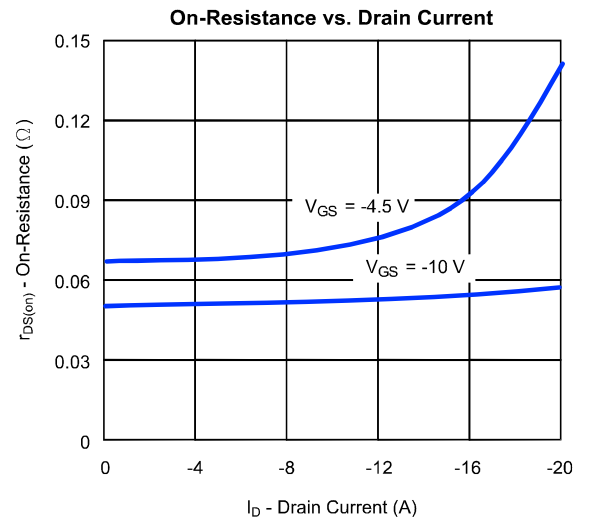
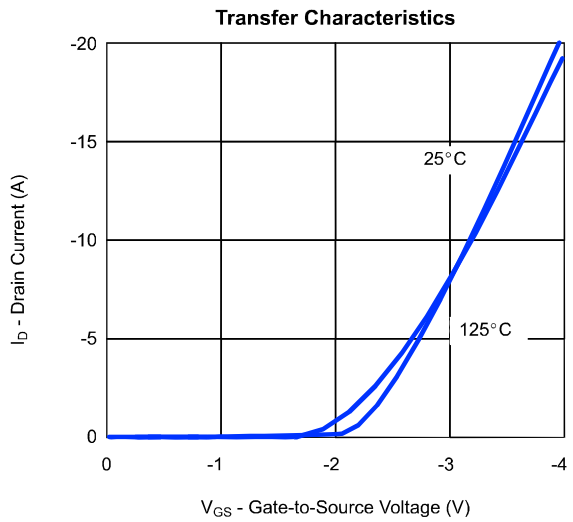
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**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  Unless Otherwise Specified)

| Symbol         | Parameter                       | Limit  | Min | Typ  | Max       | Unit          |
|----------------|---------------------------------|--|-----|------|-----------|---------------|
| <b>STATIC</b>  |                                 |  |     |      |           |               |
| $V_{GS(th)}$   | Gate Threshold Voltage          | $V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$   | -1  | -1.4 | -3        | V             |
| $I_{GSS}$      | Gate Leakage Current            | $V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$  |     |      | $\pm 100$ | nA            |
| $I_{DSS}$      | Zero Gate Voltage Drain Current | $V_{DS}=-30\text{V}, V_{GS}=0\text{V}$   |     |      | -1        | $\mu\text{A}$ |
|                |                                 | $V_{DS}=-30\text{V}, V_{GS}=0\text{V}$<br>$T_J=55^\circ\text{C}$                               |     |      | -25       |               |
| $R_{DS(ON)}$   | Drain-Source On-Resistance      | $V_{GS}=-10\text{V}, I_D=-5.3\text{A}$   |     | 50   | 60        | m $\Omega$    |
|                |                                 | $V_{GS}=-4.5\text{V}, I_D=-4.2\text{A}$  |     | 69   | 90        |               |
| $V_{SD}$       | Diode Forward Voltage           | $I_S=-1.7\text{A}, V_{GS}=0\text{V}$   |     | -0.8 | -1.2      | V             |
| <b>DYNAMIC</b> |                                 |  |     |      |           |               |
| $R_g$          | Gate resistance                 | $V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$  |     | 3.5  |           | $\Omega$      |
| $C_{iss}$      | Input capacitance               | $V_{DS}=-15\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$  |     | 450  | 490       | pF            |
| $C_{oss}$      | Output Capacitance              |  |     | 70   |           |               |
| $C_{rss}$      | Reverse Transfer Capacitance    |  |     | 20   |           |               |
| $Q_g$          | Total Gate Charge               | $V_{DS}=-15\text{V}, V_{GS}=-10\text{V},$<br>$I_D=-5.3\text{A}$                                |     | 14   | 17        | nC            |
| $Q_{gs}$       | Gate-Source Charge              |  |     | 4    |           |               |
| $Q_{gd}$       | Gate-Drain Charge               |  |     | 3    |           |               |
| $t_{d(on)}$    | Turn-On Delay Time              | $V_{DD}=-15\text{V}, R_L=15\Omega$<br>$I_D=-1.0\text{A}, V_{GEN}=-10\text{V}$<br>$R_G=6\Omega$ |     | 27   | 33        | ns            |
| $t_r$          | Turn-On Rise Time               |  |     | 11   | 15        |               |
| $t_{d(off)}$   | Turn-Off Delay Time             |  |     | 40   | 52        |               |
| $t_f$          | Turn-Off Fall Time              |  |     | 4    | 6         |               |

 Notes: a. Pulse test; pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

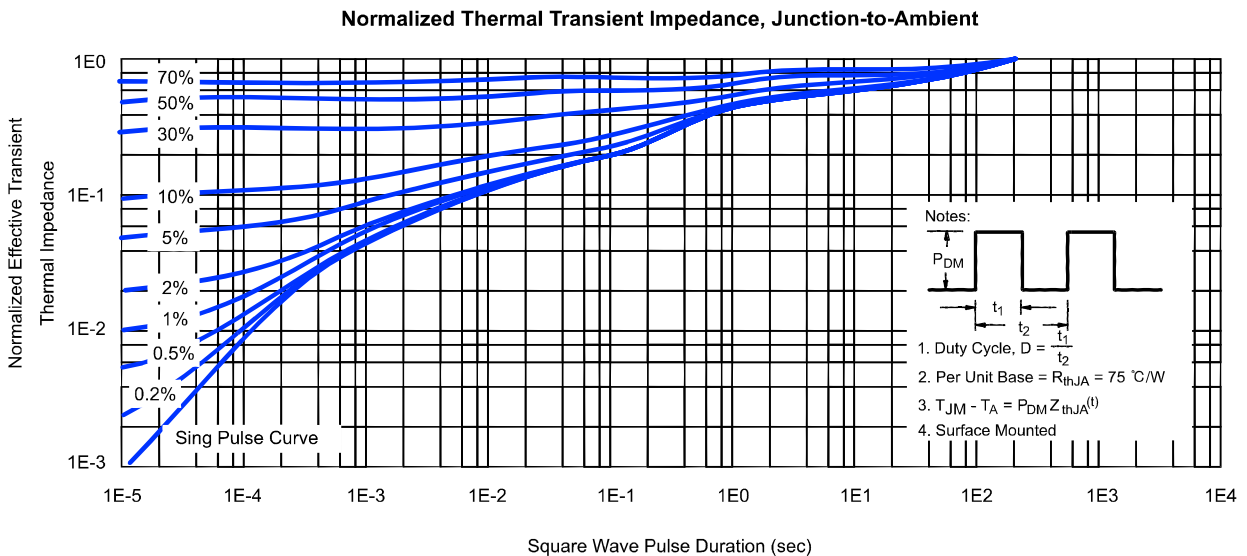
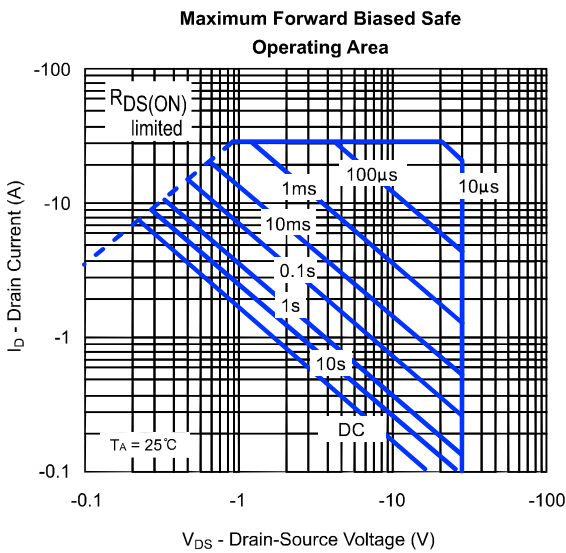
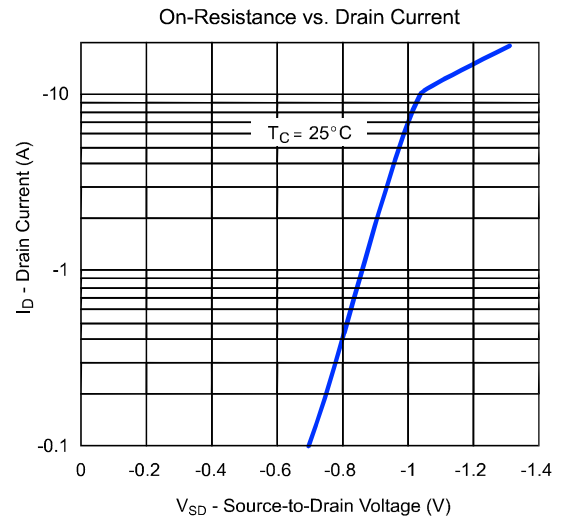
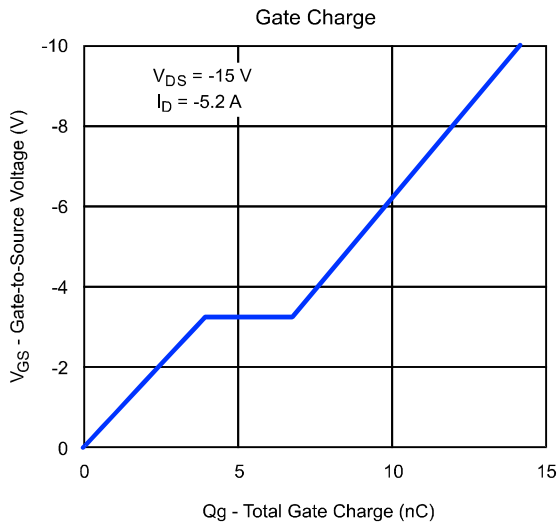
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**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**



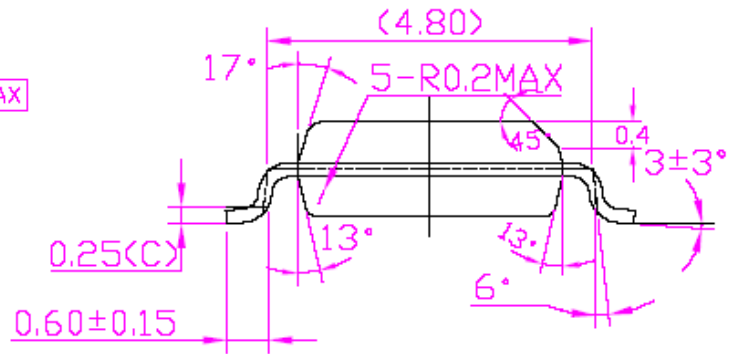
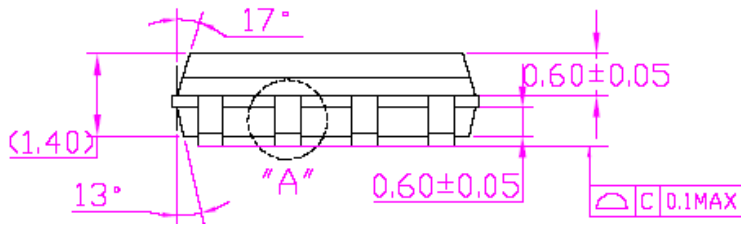
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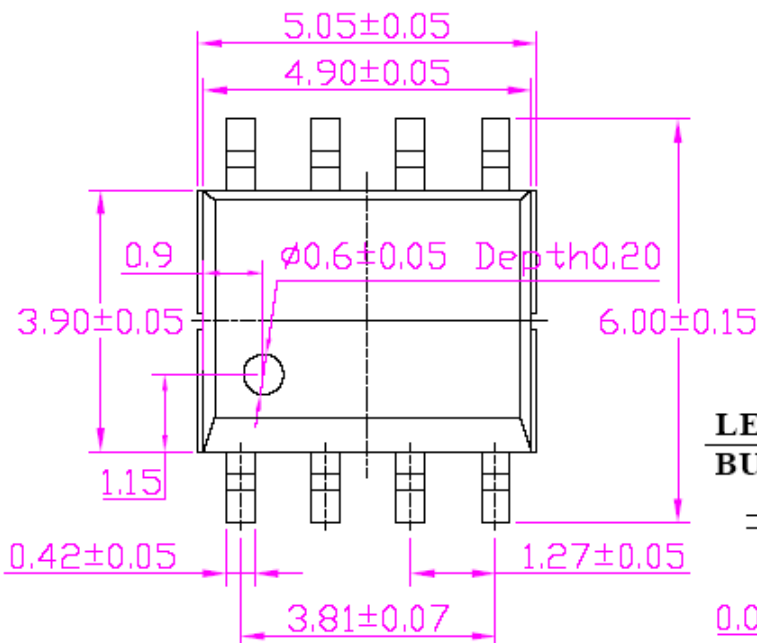
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**SOP-8 Package Outline**

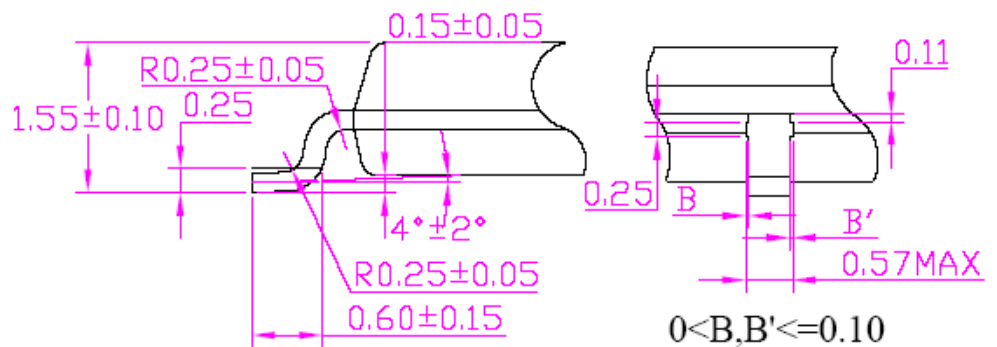
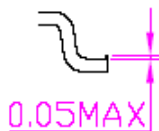


**LEAD FORM**  
**PART 15:1**

**"A"PART**  
**15:1**



**LEAD TIP**  
**BURR 10:1**



**NOTES:**

1. PKG ALL SURFACES ARE Ra0.8-1.2um.
2. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).

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