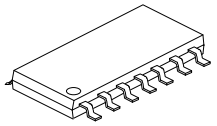
VOLTAGE MODE PWM CONTROLLER WITH LINEAR POWER REGULATOR



SOP-14

■ DESCRIPTION

The UTC **U8021** provides the control and protection features necessary for a synchronous buck converter and a linear regulator in high performance graphic card applications.

The UTC **U8021** is designed to directly drive the high and low MOSFETs of the buck converter. It allows the converter to operate with 4V~25V power rail and as low as 0.5V output. The UTC **U8021** is capable to drive a N-type MOSFET in a linear regulator with as low as 0.5V output.

The UTC **U8021** features soft-start, UVLO, and OCP. The UTC **U8021** monitors the output current by using the Rdson of the low MOSFET in the buck converter that eliminates the need for a current sensing resistor.

■ FEATURES

* 4V~25V power rails
* Internal LDO
* 1.5A gate drive current
* Adaptive non-overlapping gate drives provide shoot-through protection for MOSFETs
* Programmable output voltages
* Internal soft start
* Under voltage lockout
* Short circuit protection

■ ORDERING INFORMATION

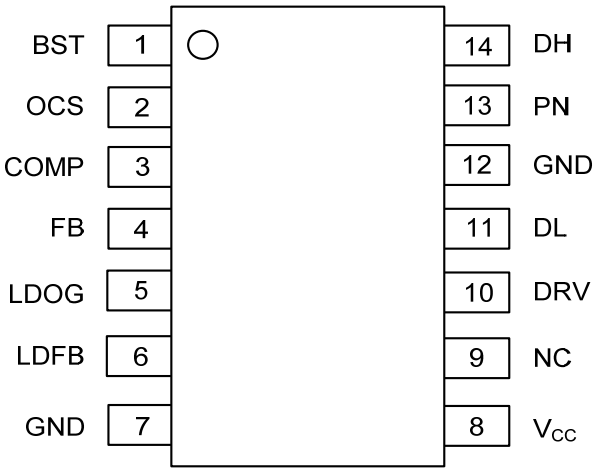
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U8021L-S14-T	U8021G-S14-T	SOP-14	Tube
U8021L-S14-R	U8021G-S14-R	SOP-14	Tape Reel

U8021L-S14-T

(1)Packing Type
(2)Package Type
(3)Halogen Free

(1) T: Tube, R: Tape Reel
(2) S14: SOP-14
(3) L: Lead Free, G: Halogen Free

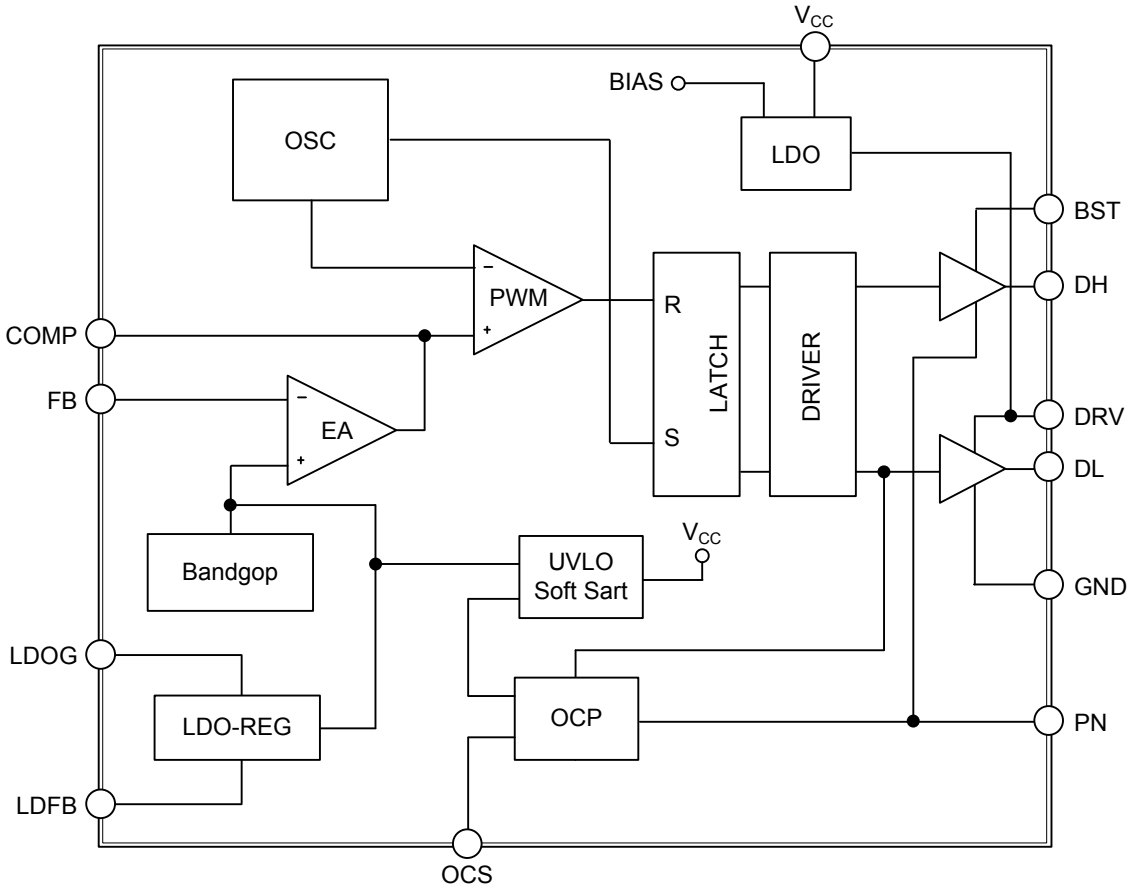
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BST	Boost input for top gate drive bias.
2	OCS	Current limit setting.
3	COMP	Compensation PIN.
4	FB	Feedback voltage
5	LDOG	External LDO gate drive.
6	LDFB	External LDO feedback voltage.
7	GND	Ground.
8	V_{CC}	Power supply.
9	NC	No Bonding.
10	DRV	Internal LDO output.
11	DL	Gate drive for low MOSFET.
12	GND	Ground.
13	PN	Phase PIN.
14	DH	Gate drive for high MOSFET.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

PARAMETER	SYMBOL	RATINGS	UNIT
Input Supply Voltage	V_{CC}	18	V
BST to GND	V_{BST}	40	V
BST to PN	V_{BST_PN}	10	V
PN to GND	V_{PN}	-1~30	V
PN to GND Negative Pulse (t_{pulse}<20ns)	V_{PN_PULSE}	-5	V
DL to GND	V_{DL}	-1~+10	V
DL to GND Negative Pulse (t_{pulse}<20ns)	V_{DL_PULSE}	-3	V
DH to PN	V_{DH_PN}	-1~+10	V
DH to PN Negative Pulse (t_{pulse}<20ns)	V_{DH_PULSE}	-3	V
DRV to GND	V_{DRV}	10	V
Operating Ambient Temperature Range	T_A	-25~85	°C
Operating Junction Temperature	T_J	-25~125	°C
Storage Temperature	T_{STG}	-65~150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL RESISTANCES

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	100	°C/W
Junction to Case	θ_{JC}	32	°C/W

■ ELECTRICAL CHARACTERISTICS

(Unless specified: V_{CC}= 5V~16V, V_{FB}=V_{OUT}, V_{BST}-V_{PN}=5V~8.2V, T_A=-25°C~85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
V_{CC} Supply Voltage	V_{CC}		4		16	V
V_{CC} Quiescent Current	I_{QVCC}	V_{CC}=12V, V_{BST}-V_{PN}=8.2V		5	7	mA
V_{CC} Under Voltage Lockout	UV_{VCC}	V_{HYST}=100mV			4	V
BST to PN Supply Voltage	V_{BST_PN}		4		10	V
BST Quiescent Current	I_{QBST}	V_{CC}=12V, V_{BST}-V_{PN}=8.2V			3	mA
Internal LDO						
LDO Output	V_{DRV}	8.6V<V_{CC}<16V		8		V
Dropout Voltage	V_{DROP}	4V<V_{CC}<8.6V		0.4		V
Linear Section						
Reference Voltage	V_{OL}	L_{DFB}=V_{OL}, T_A=25°C, V_{CC}=12V	0.65	0.75	0.85	V
Load Regulation		I_O=0~1A, V_{IN}=3.3V, V_{CC}=12V			0.4	%
Line Regulation		V_{IN}=3.2V~3.4V, V_{CC}=12V			0.4	%
V_{CC} Supply Rejection		V_{IN}=3.3V, V_{CC}=10V~14V			0.4	%
Gate Sourcing Current		VGATE=6.5V		1		mA
Gate Sinking Current		VGATE=6.5V		1		mA
LDFB Input Bias Current		LDFB=.5V		-0.2	-1.0	uA
Soft Start Time		V_{IN}=3.3V, V_{CC}=12V T_A=25°C		1.5		ms
Switching Section						
Reference Voltage	V_{REF}	T_A=25°C, V_{CC}=12V	0.495	0.500	0.505	V
Load Regulation		I_O=0.2~4A		0.4		%
Line Regulation		V_{CC}=10V~14V		0.4		%
Operating Frequency	F_S		500	600	700	KHz
Ramp Amplitude (Note 2)	V_m			0.8		V
Maximum Duty Cycle (Note 2)	D_{MAX}			97		%
Minimum On-Time (Note 2)	T_{ON_MIN}			125		ns
DH Rising/Falling Time	t_{SRC_DH}	6V Swing at C_L=3.3nF, V_{BST}-V_{PN}=8.2V		40		ns
	t_{SINK_DH}			25		
DL Rising/Falling Time	t_{SRC_DL}	6V Swing at C_L=3.3nF, V_{DRV}=8.2V		30		ns
	t_{SINK_DL}			40		
DH, DL Nonoverlapping Time				30		ns
Voltage Error Amplifier						
Output Source Current				0.9		mA
Output Sink Current				0.9		mA

Notes: 1. This device is ESD sensitive. Use of standard ESD handling precautions is required.
2. Guaranteed by design, not tested in production.

■ TYPICAL APPLICATION CIRCUIT