Input Voltage 3.5 V to 36 V
Output SW Current 4 A / 2.5A / 1.25A
1ch Step-Down Switching Regulator

BD906xxEFJ-C

General Description

BD906xxEFJ-C is a step-down switching regulator controllers with integrated POWER MOS FET and has the capability to withstand high input voltage, providing a free setting function of operating frequency with external resistor. This switching regulator controller features a wide input voltage range (3.5 V to 36 V) and operating temperature range (-40 °C to +125 °C). Furthermore, an external synchronization input pin enables synchronous operation with external clock.

Features

- Minimal External Components
- Integrated Pch POWER MOS FET
- Low Dropout: 100 % ON Duty Cycle
- External Synchronization Enabled
- Soft Start Function: 1.38 ms (f = 500 kHz)
- Current Mode Control
- Over Current Protection
- Low Supply Voltage Error Prevention
- Thermal Shut Down Protection
- Short Circuit Protection
- Compact and High power HTSOP-J8 package mounted
- AEC-Q100 Qualified

Applications

- Automotive Battery Powered Supplies (Cluster Panels, Car Multimedia)
- Industrial / Consumer Supplies

Key Specifications

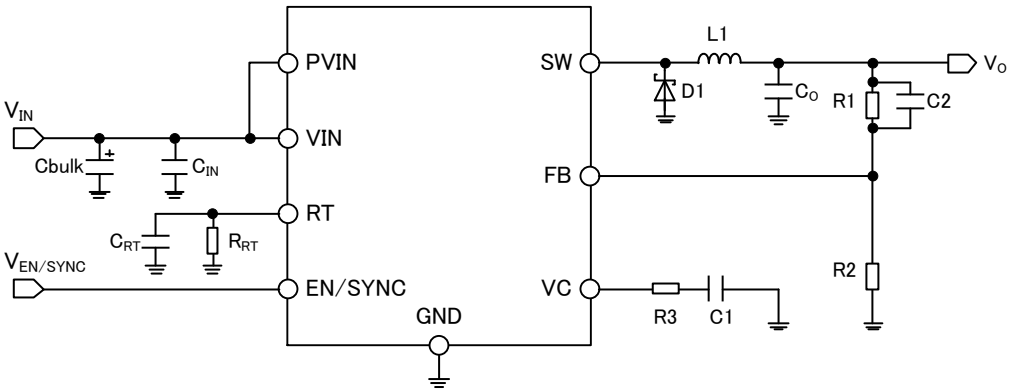
- Input Voltage Range: 3.5 V to 36 V (Initial startup is over 3.9 V)
- Output Voltage Range: 0.8V to V_{IN}
- Output Switch Current: 4 A / 2.5 A / 1.25 A (Max)
- Selectable Operating Frequency: 50 kHz to 600 kHz
- Reference Voltage Accuracy: ±1 %
- Shutdown Circuit Current: 0 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

	W(Typ) x D(Typ) x H(Max)
HTSOP-J8	4.90 mm x 6.00 mm x 1.00 mm

HTSOP-J8

Typical Application Circuit

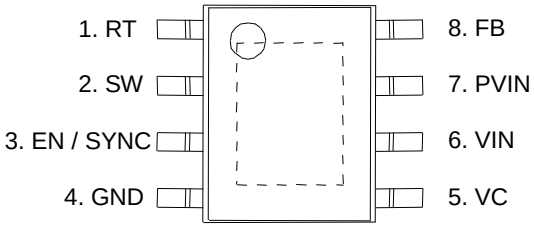


Lineup

Product Name	BD90640EFJ-C	BD90620EFJ-C	BD90610EFJ-C
Output Switch Current	4 A	2.5 A	1.25 A
Input Maximum Ratings	42 V		
Input Range (Note 1)	3.5 V to 36 V		
POWER MOS FET ON Resistance	0.16 Ω		
Package	HTSOP-J8		
Power Dissipation (Note 2)	3.75 W		

(Note 1) Initial startup is over 3.9 V
(Note 2) Reduce by 30 mW / °C, when mounted on 4-layer PCB of 70 mm × 70 mm × 1.6 mm.

Pin Configuration

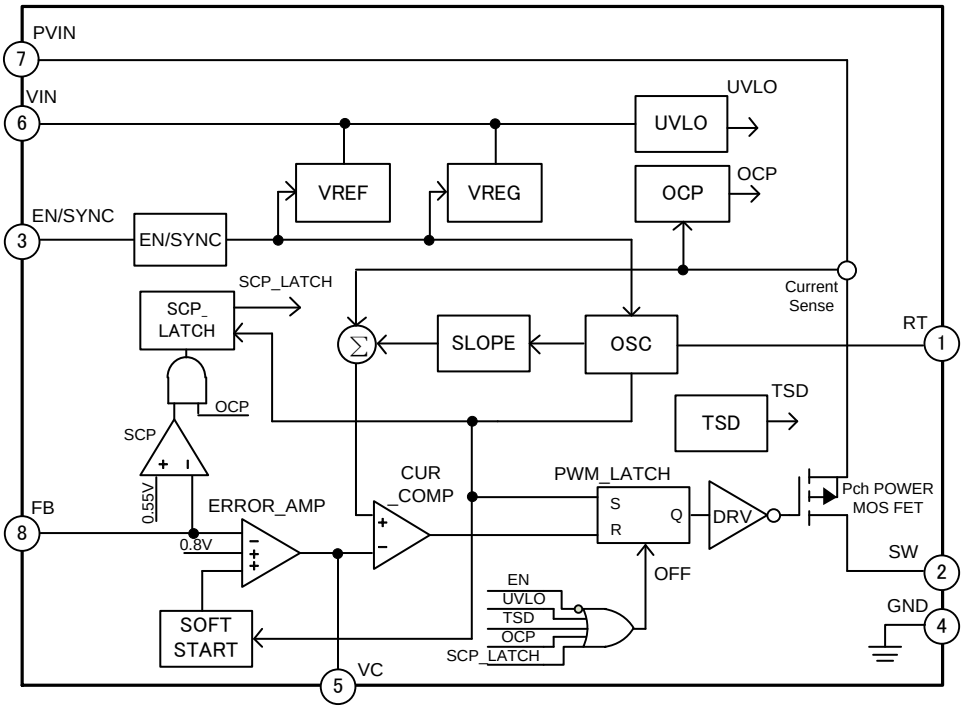


Pin Description

Pin No.	Symbol	Function
1	RT	Frequency Setting Resistor Connection
2	SW	Switching Output
3	EN / SYNC	Enable / Synchronizing Pulse Input
4	GND	GND
5	VC	Error Amp Output
6	VIN	Power Supply Input (Note 1)
7	PVIN	Power System Power Supply Input (Note 1)
8	FB	Output Voltage Feedback

(Note 1) VIN and PVIN are shorted.

Block Diagram



Description of Blocks

・ERROR-AMP
The ERROR-AMP block is an error amplifier and its inputs are the reference voltage 0.8 V (Typ) and the “FB” pin voltage. (Refer to recommended examples on p.16 to 17) The output “VC” pin controls the switching duty and output voltage Vo. These “FB” and “VC” pins are externally mounted for phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin.

・SOFT START
The function of the SOFT START block is to prevent the overshoot of the output voltage V_O through gradually increasing the input of the error amplifier when the power supply turns ON, which also results to the gradual increase of the switching duty. The soft start time is set to 1.38 ms (f = 500 kHz).
The soft start time is changed by setting of the oscillating frequency. (Refer to p.17)

・EN / SYNC
The IC is in normal operation when the voltage on the “EN / SYNC” terminal is more than 2.6V. The IC is shut down when the voltage on the “EN / SYNC” terminal is less than 0.8V. Furthermore, external synchronization is possible when pulses are applied to the “EN / SYNC” terminal. The frequency range of the external synchronization is within ±20 % of the oscillation frequency and is limited by the external resistance connected to the RT pin.
ex) When R_{RT} is 27 kΩ (f = 500 kHz), the frequency range of the external synchronization is 400 kHz to 600 kHz.

・OSC (Oscillator)
This circuit generates the input pulse wave of the SLOPE block. The frequency of the pulse wave can be configured by connecting a resistor to the RT pin. The range of the oscillating frequency is from 50 kHz to 600 kHz. (Refer to p.16 Figure 13). The output of the OSC block send clock signals to PWM_LATCH. The generated pulses of the OSC block are also used as clock of the counter of SS and SCP_LATCH blocks.

・SLOPE
This block generates saw tooth waves using the clock generated by the OSC block. The generated saw tooth waves are sent to the CUR_COMP block and to current sense.

・CUR_COMP
The CUR_COMP block compares the signals between the “VC” pin and the combined signals from the SLOPE block and current sense. The output signals are sent to the PWM_LATCH block.

・PWM_LATCH
The PWM_LATCH block is a LATCH circuit. The OSC block output (set) and CUR_COMP block output (reset) are the inputs of this block. The PWM_LATCH block outputs PWM signals.

・TSD (Thermal Shutdown)
The TSD block prevents thermal destruction / thermal runway of the IC by turning OFF the output when the temperature of the chip reaches approximately 150 °C or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is designed to protect the IC, the chip temperature should be provided with the thermal shutdown detection temperature of less than approximately 150 °C.

・OCP (Over Current Protection)
OCP is activated when the voltage between the drain and source (on-resistance × load current) of the P-ch POWER MOSFET when it is ON, exceeds the reference voltage which is internally set within the IC. This OCP is a self-return type. When OCP is activated, the duty will be small, and the output voltage will decrease. However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is connected).

・SCP (Short Circuit Protection) and SCP-LATCH
While OCP is operating, and if the output voltage falls below 70 %, SCP will be activated. When SCP is active, the output will be turned OFF after a period of 1024 pulse. It extends the time that the output is OFF to reduce the average output current. In addition, during start-up of the IC, this feature is masked until it reaches a certain output voltage to prevent the wrong triggering of SCP.

・UVLO (Under Voltage Lock-Out)
UVLO is a protection circuit that prevents low voltage malfunction. It prevents malfunction of the internal circuit from sudden rise and fall of power supply voltage. It monitors the V_{IN} power supply voltage and the internal regulator voltage. If V_{IN} is less than the threshold voltage 3.24 V (Typ), the Pch POWER MOS FET output is OFF and the soft-start circuit will be restarted. This threshold voltage has a hysteresis of 280 mV (Typ).

・DRV (Driver)
This circuit drives the gate electrode of the Pch POWER MOS FET output. It reduces the increase of the Pch POWER MOS FET’s on-resistance by switching the driving voltage when the power supply voltage drop.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{IN}、PV_{IN}	42	V
SW Pin Voltage	V_{SW}	V_{IN}	V
EN / SYNC Pin Voltage	$V_{EN\ /\ SYNC}$	V_{IN}	V
RT, VC, FB Pin Voltage	V_{RT}, V_{VC}, V_{FB}	7	V
Power Dissipation (Note 1)	Pd_{EFJ}	3.75	W
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) Reduce by 30 mW / °C, when mounted on 4-layerPCB of 70mm × 70mm × 1.6mm
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter		Symbol	Limits		Unit
			Min	Max	
Operating Power Supply Voltage (Note 1)		V_{IN}, PV_{IN}	3.5	36	V
Operating Temperature Range		Topr	-40	+125	°C
Output Switch Current (Note2)	BD90640EFJ-C	$I_{SWopr40}$	-	4	A
	BD90620EFJ-C	$I_{SWopr20}$	-	2.5	A
	BD90610EFJ-C	$I_{SWopr10}$	-	1.25	A
Output Voltage		V_O	0.8	V_{IN}	V
Min Pulse Width		T_{ONMIN}	250	-	ns
Oscillation Frequency		f_{SW}	50	600	kHz
Oscillation Frequency Set Resistance		R_{RT}	22	330	kΩ
Synchronous Operation Frequency Range		f_{SYNC}	50	600	kHz
Synchronous Operation Frequency		$f_{SYNC\ -\ RT}$	-20	+20	%
External Clock Pulse Duty		D_{SYNC}	10	90	%

(Note 1) Initial startup is over 3.9 V.
(Note 2) The Limits include output DC current and output ripple current.

Electrical Characteristics (Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{IN} = 13.2 V, $V_{EN\ /\ SYNC}$ = 5 V)

Parameter		Symbol	Guaranteed Limit			Unit	Conditions
			Min	Typ	Max		
1chip							
Shutdown Circuit Current		I_{SDN}	-	0	5	μA	$V_{EN\ /\ SYNC}$ = 0 V, Ta < 105 °C
Circuit Current		I_{IN}	-	2.2	3.3	mA	Io = 0 A, V_{FB} = 2 V
SW Block							
POWER MOS FET ON Resistance		R_{ON}	-	0.16	0.32	Ω	I_{SW} = 30 mA
Operating Output Switch Current Of Overcurrent Protection	BD90640EFJ-C	$I_{SWLIMIT40}$	4.0	6.4	-	A	
	BD90620EFJ-C	$I_{SWLIMIT20}$	2.5	4.3	-	A	
	BD90610EFJ-C	$I_{SWLIMIT10}$	1.25	2.20	-	A	
Output Leak Current		I_{OLK}	-	0	5	μA	V_{IN} = 36 V, $V_{EN/SYNC}$ = 0 V, Ta < 105 °C
Error Amp Block							
Reference Voltage 1		V_{REF1}	0.792	0.800	0.808	V	V_{VC} = V_{FB}, Ta = 25 °C
Reference Voltage 2		V_{REF2}	0.784	0.800	0.816	V	V_{VC} = V_{FB}
Reference Voltage Input Regulation		ΔV_{REF}	-	0.5	-	%	3.5 V ≤ V_{IN} ≤ 36 V
Input Bias Current		I_B	-1.0	-	1.0	μA	
VC Sink Current		I_{VCSINK}	-76.5	-54.0	-31.5	μA	V_{VC} = 1.25 V, V_{FB} = 1.3 V
VC Source Current		$I_{VCSOURCE}$	31.5	54.0	76.5	μA	V_{VC} = 1.25 V, V_{FB} = 0.3 V
Trans Conductance		G_{EA}	135	270	540	μA / V	I_{VC} = ±10 μA, V_{VC} = 1.25 V
Soft Start Time		T_{SS}	1.13	1.38	1.63	ms	R_{RT} = 27 kΩ
Current Sense Part							
Trans Conductance		G_{CS}	-	5.2	-	A / V	
Oscillator Block							
Oscillating Frequency		f_{SW}	450	500	550	kHz	R_{RT} = 27 kΩ
Frequency Input Regulation		Δf_{SW}	-	1	-	%	3.5 V ≤ V_{IN} ≤ 36 V
Enable / Sync Input Block							
Threshold Voltage		$V_{EN\ /\ SYNC}$	0.8	1.9	2.6	V	
SYNC Current		$I_{EN\ /\ SYNC}$	-	23	50	μA	$V_{EN/SYNC}$ = 5 V
UVLO							
UVLO ON Mode Voltage		V_{UVLO_ON}	-	3.24	3.50	V	
UVLO OFF Mode Voltage		V_{UVLO_OFF}	-	3.52	3.90	V	
UVLO Hysteresis		V_{UVLO_HYS}	-	280	-	mV	

Typical Performance Curves

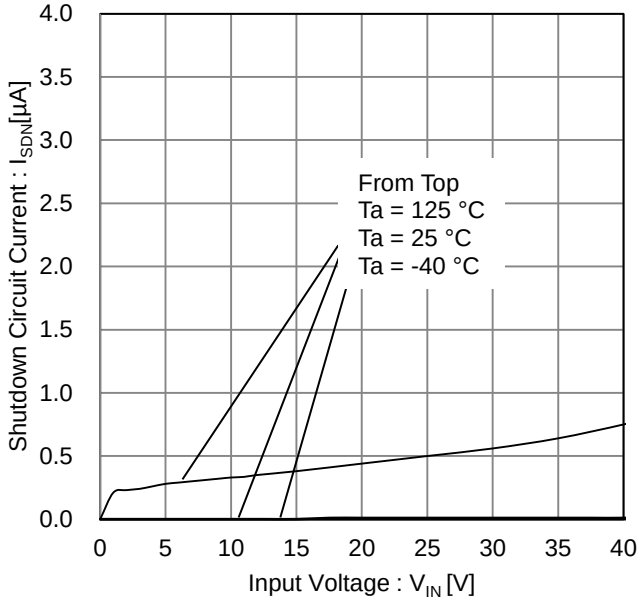


Figure 1. Shutdown Circuit Current vs Input Voltage

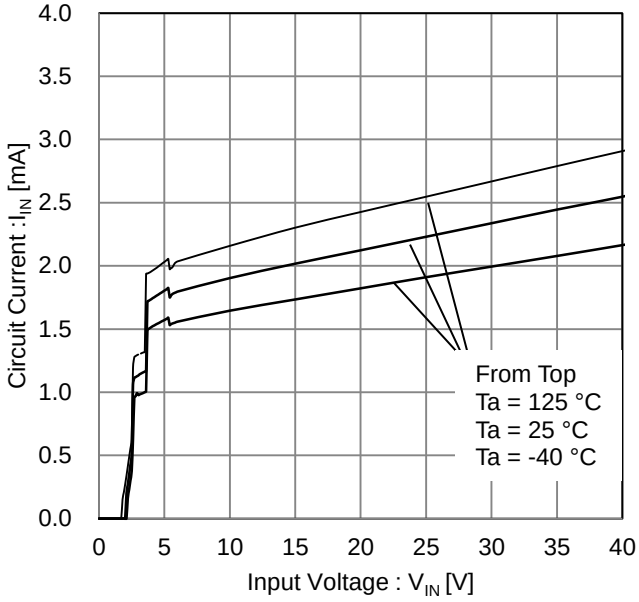


Figure 2. Circuit Current vs Input Voltage

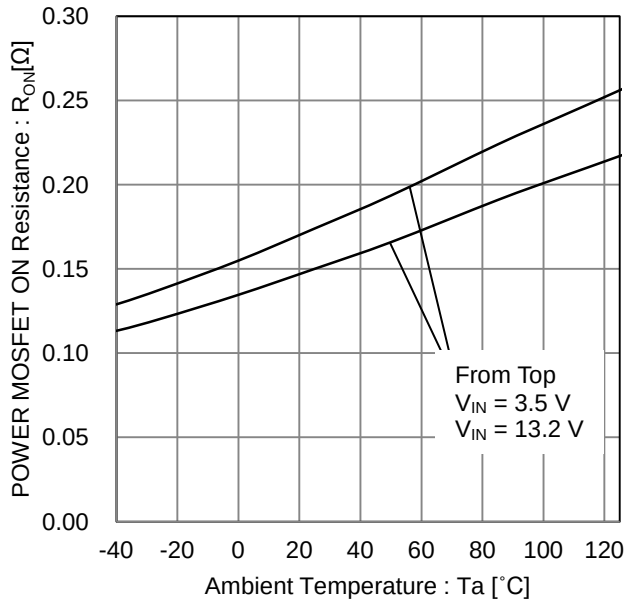


Figure 3. POWER MOSFET ON Resistance vs Ambient Temperature

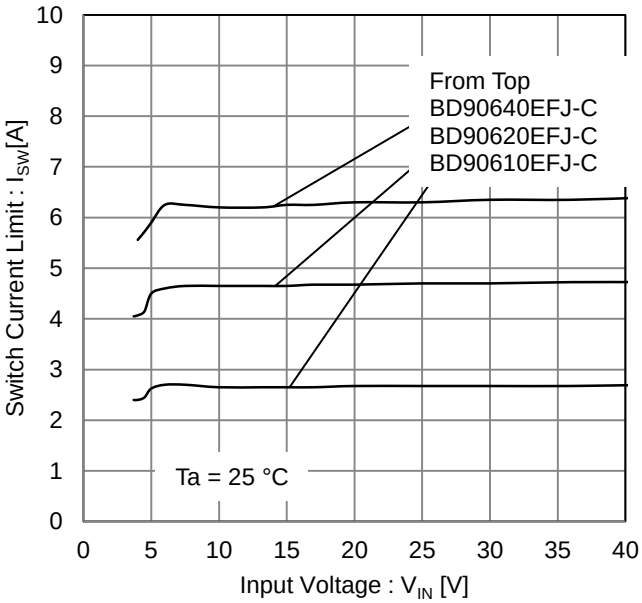


Figure 4. Switch Current Limit vs Input Voltage

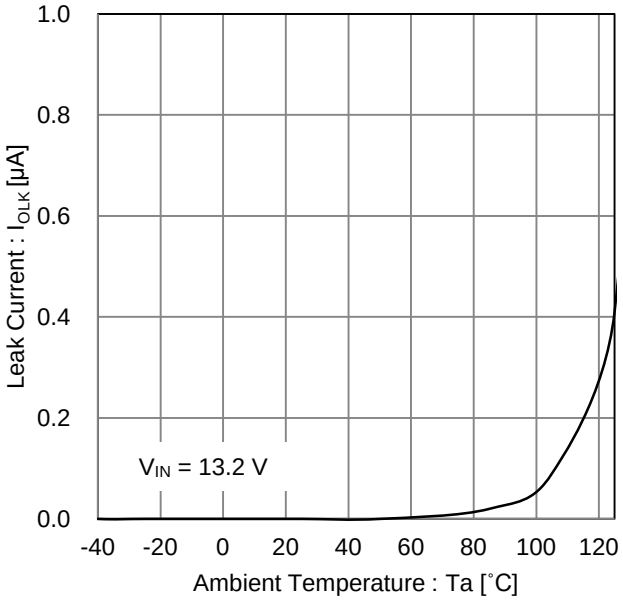


Figure 5. Leak Current vs Ambient Temperature

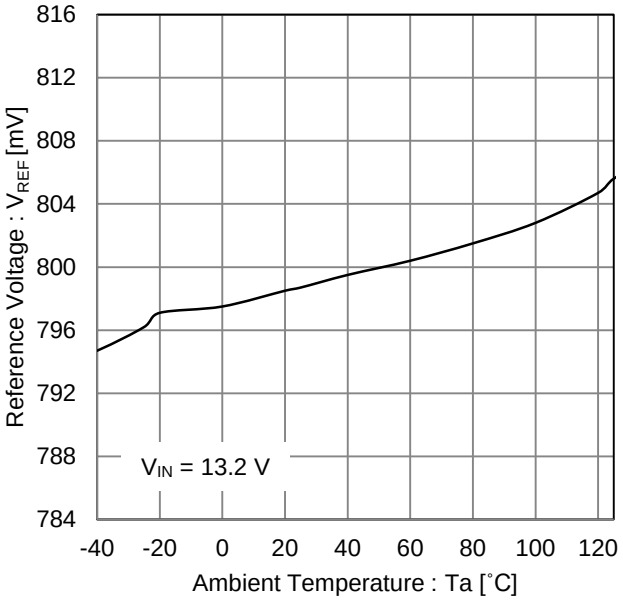


Figure 6. Reference Voltage vs Ambient Temperature

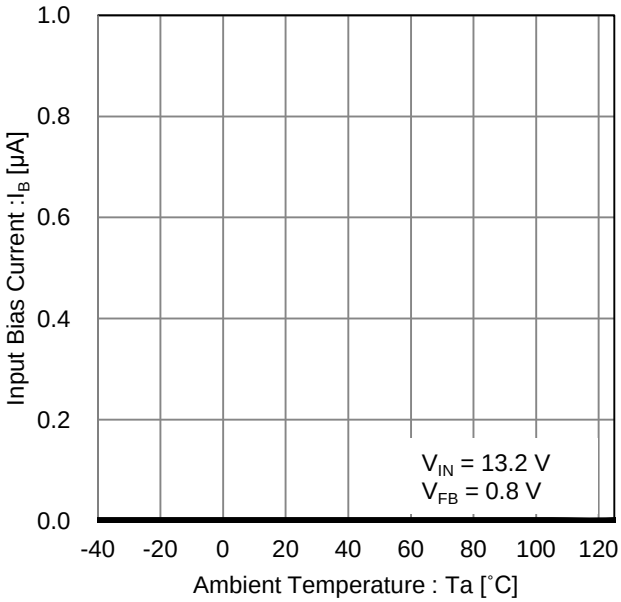


Figure 7. Input Bias Current vs Ambient Temperature

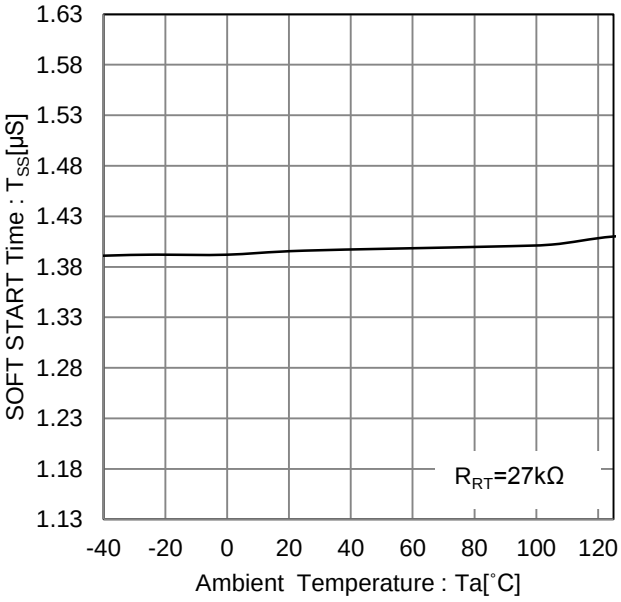


Figure 8. SS Time vs Ambient Temperature

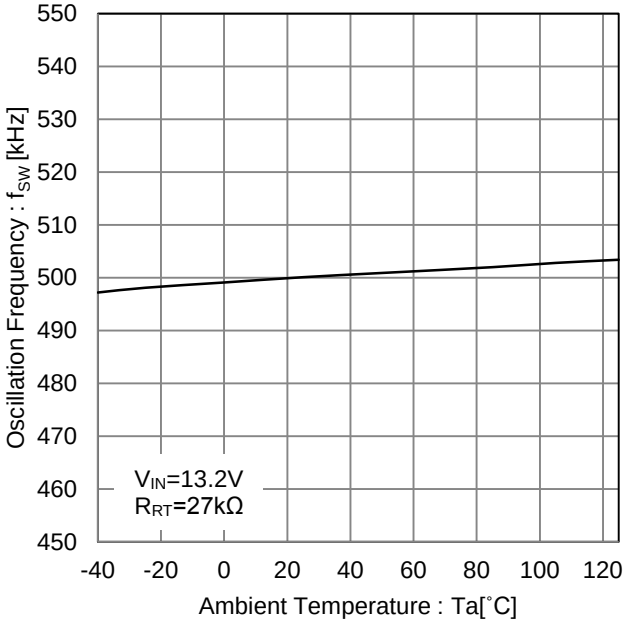


Figure 9. Oscillation Frequency vs Ambient Temperature

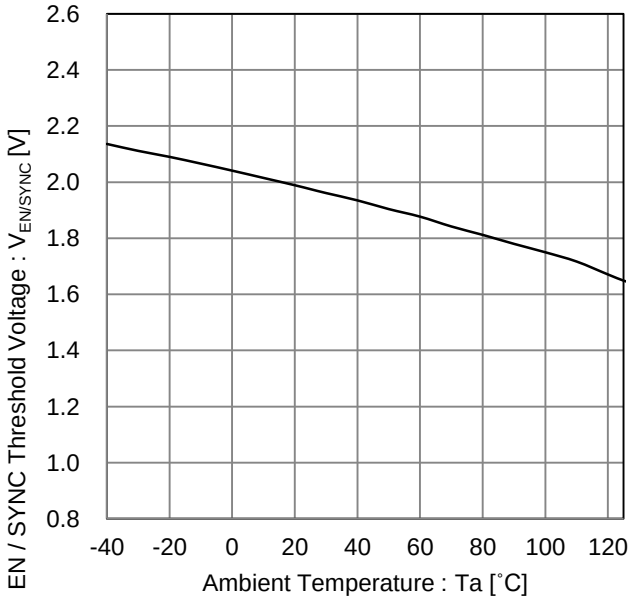


Figure 10. EN / SYNC Threshold Voltage vs Ambient Temperature

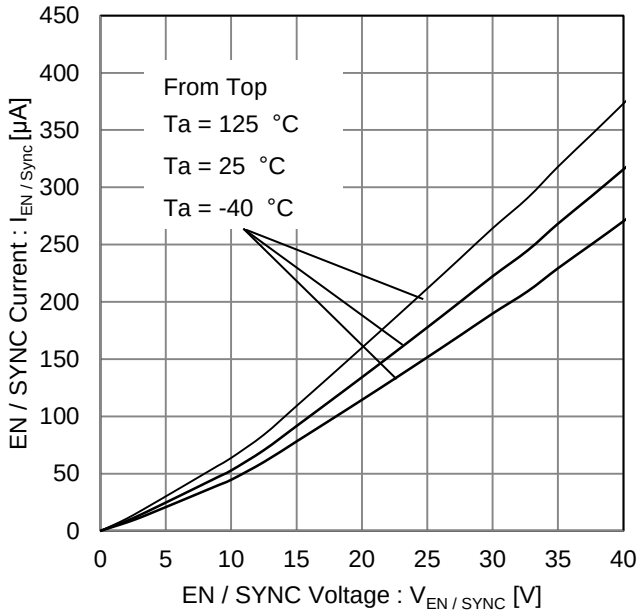


Figure 11. EN / SYNC Current vs EN / SYNC Voltage

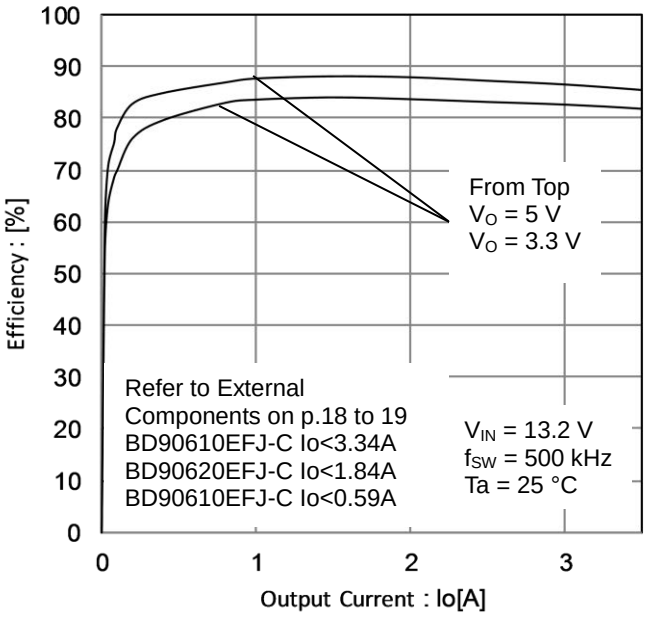
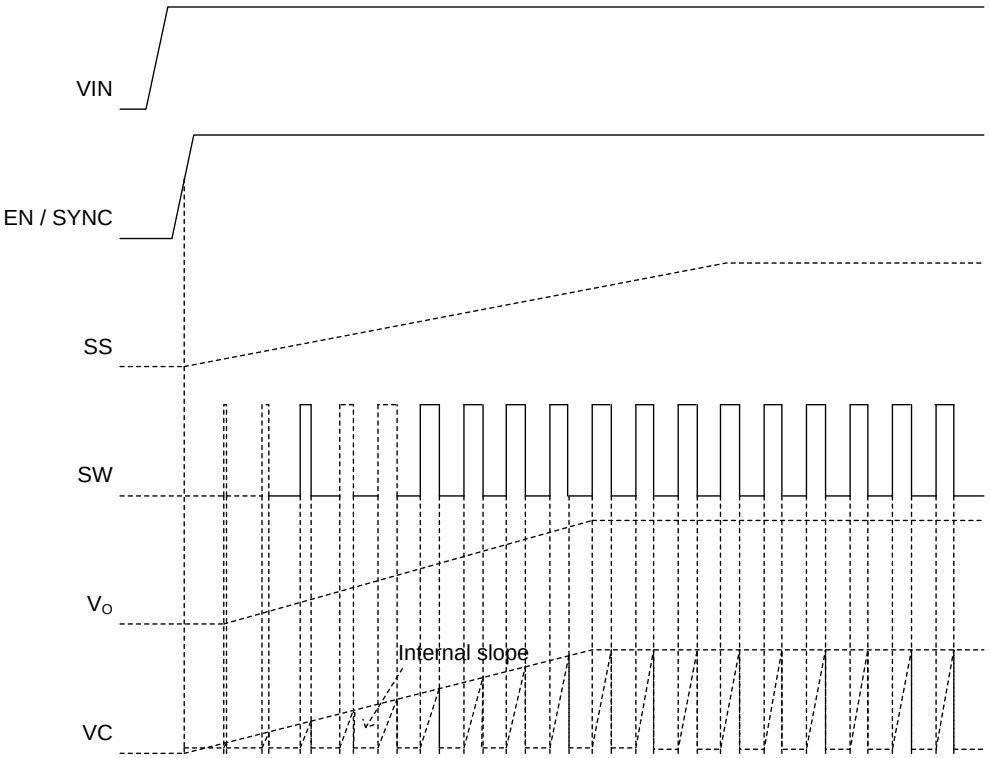


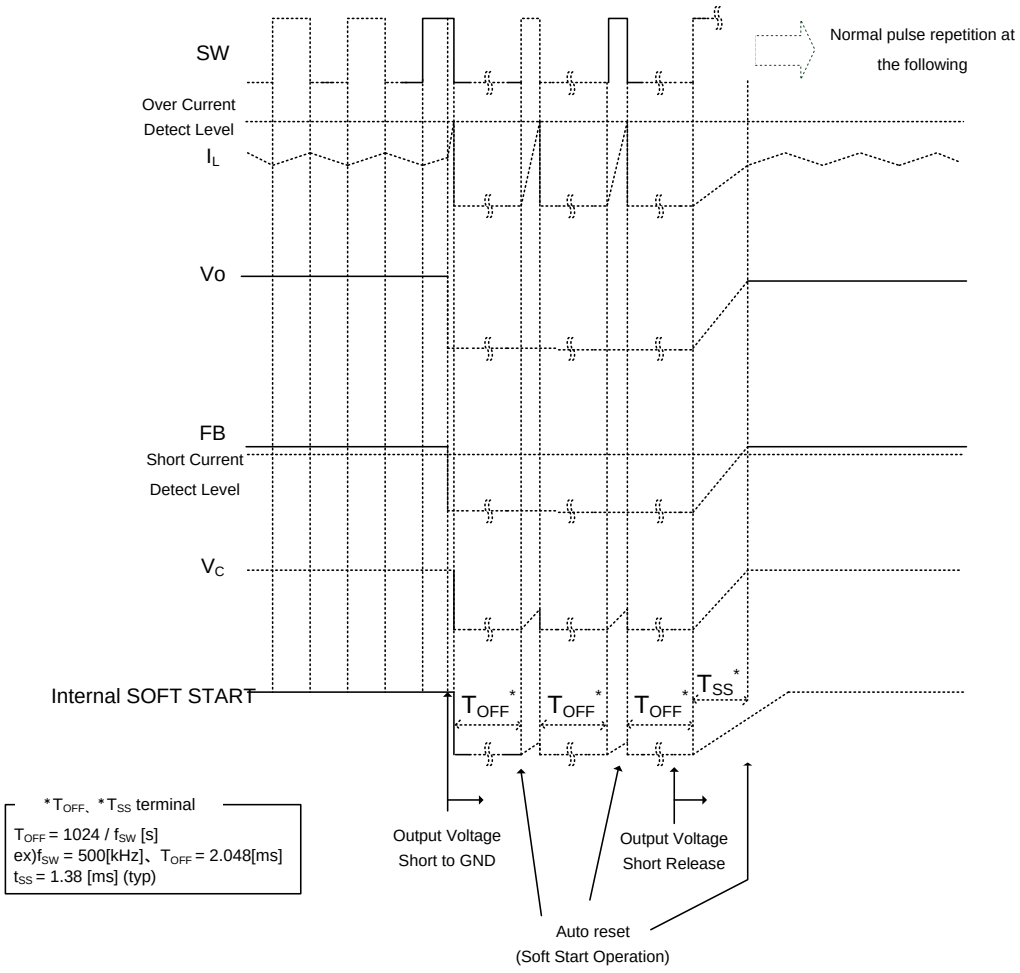
Figure 12. Efficiency vs Output Current

Timing Chart

・Basic Operation



・Over Current Protection Operation

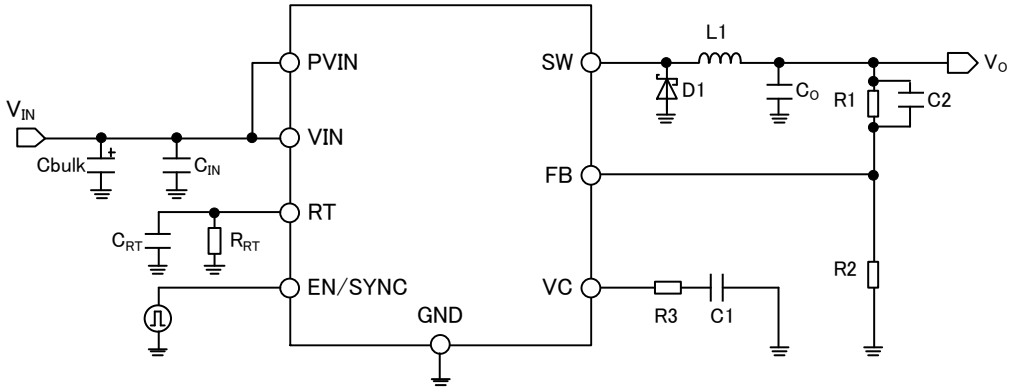


External Synchronizing Function

In order to activate the external synchronizing function, connect the frequency-setting resistor to the RT pin and then input a synchronizing signal to the EN / SYNC pin. For the synchronizing signal, input a pulse wave higher than the oscillation frequency.
The external synchronizing operation frequency is limited by the external resistance of R_{RT} pin. The allowable setting limit is within ±20 % of the oscillation frequency. (e.g. When R_{RT} 27 kΩ)

The external synchronous operation frequency limit is 400 kHz to 600 kHz because the oscillation frequency is 500 kHz. Furthermore, the pulse wave's LOW voltage should be under 0.8 V and the HIGH voltage over 2.6 V (when the HIGH voltage is over 11 V the EN / SYNC input current increases), and the slew rate (rise and fall) under 20 V / µS. The duty of External sync pulse should be configured between 10 % and 90%.

The frequency will synchronize with the external synchronizing operation frequency after three external sync pulses is sensed.

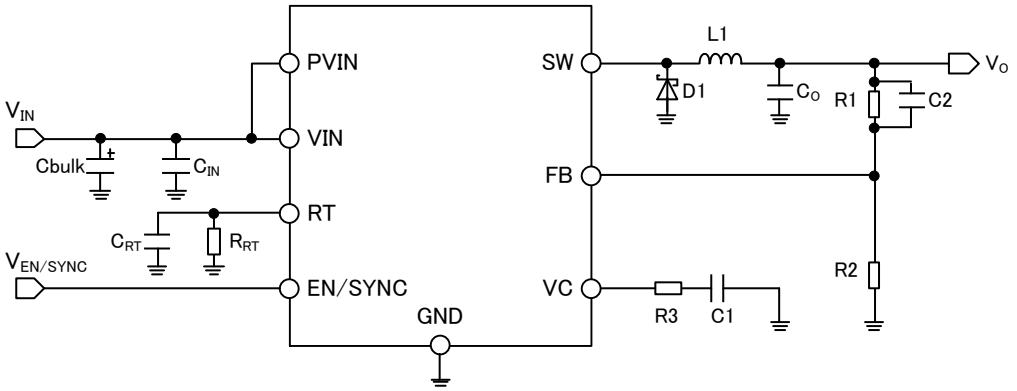


Eternal SYNC Sample Circuit

Selection of Components Externally Connected

Necessary parameters in designing the power supply are as follows:

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	6 V to 36 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mV_{p-p}
Input Range	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature Range	Topr	-40 °C to +105 °C



Application Sample Circuit

(1) Setting the output L constant

When the switching regulator supplies electric current continuously to the load, the LC filter is necessary for the smoothness of the output voltage. The ΔI_L that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple also becomes small. It is the trade-off between the size and the cost of the inductor.

The inductance value of the inductor is shown in the next expression:

$$L = \frac{(V_{IN(MAX)} - Vo) \times Vo}{V_{IN(MAX)} \times f_{SW} \times \Delta I_L} \quad [H]$$

Where:

$V_{IN\,(MAX)}$ is the maximum input voltage

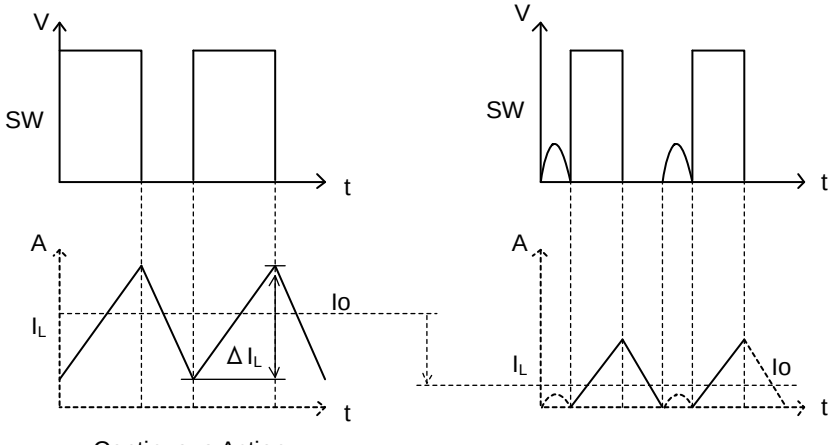
ΔI_L is the Inductor ripple current

ΔI_L is set to approximately 30 % of I_O. If avoid discontinuous operation, ΔI_L is set to make SW continuously pulsing (I_L keeps continuously flowing) usually. The condition of the continuous operation is shown in the next expression:

$$I_O > \frac{(V_{IN(MAX)} - V_O) \times V_O}{2 \times V_{IN(MAX)} \times f_{SW} \times L} \quad [A]$$

Where:

I_O is the Load Current



Continuous Action

Discontinuous Action

The smaller the ΔI_L, the Inductor core loss (iron loss) and loss due to ESR of the output capacitor, the smaller ΔV_{PP} will be. ΔV_{PP} is shown in the next expression.

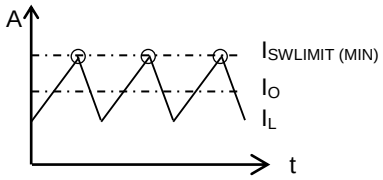
$$\Delta V_{PP} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_O \times f_{SW}} \quad [V] \quad \cdots\cdots \text{(a)}$$

Where:
ESR is the equivalent series resistance of output capacitor
C_O is the output condenser capacity

The maximum output electric current is limited to the overcurrent protection working current as shown in the next expression.

$$I_{O(MAX)} = I_{SWLIMIT(MIN)} - \frac{\Delta I_L}{2} \quad [A]$$

Where:
$I_{O\,(MAX)}$ is the maximum output current
$I_{SWLIMIT\,(MIN)}$ is the OCP operation current (Min)



I_L peak

In current mode control, when the IC is operating in Duty ≥ 50 % and in the condition of continuous operation, it is possible that sub-harmonic oscillation may occur. The slope compensation circuit is integrated into the IC in order to prevent sub-harmonic oscillation. Sub-harmonic oscillation depends on the rate of increase of output switch current IC. If the inductor value is small, the possibility of sub-harmonic oscillation is increased. And if the inductor value is large, it is possible that the IC will not operate in. The inductor value which prevents sub-harmonic oscillation is shown in the next expression.

$$\mathrm{L} \geq \frac{2\mathrm{D}-1}{2(1-D)} \times Rs \times \frac{V_{IN\,(MIN)} - V_O}{m} \quad [H]$$

$$\mathrm{D} = \frac{V_O}{V_{IN(MIN)}}$$

$$m = 6 \times f_{SW} \times 10^{-6}$$

Where:
D is the switching pulse Duty.
Rs is the coefficient of current sense（4.0 μA / A）
m is the inclination of slope compensator current

The shielded type (closed magnetic circuit type) is the recommended type of inductor. Open magnetic circuit type can be used for low cost applications and if noise issues are not concerned. But in this case, there is magnetic field radiation between the parts and there should be enough spacing between the parts.

For ferrite core inductor type, please note that magnetic saturation may occur. It is necessary not to saturate the core in all cases. Precautions must be taken into account on the given provisions of the current rating because it differs according to each manufacturer.

Please confirm the rated current at the maximum ambient temperature of the application to the manufacturer.

(2) Set of output Capacitor C_O constant

The output capacitor is selected on the basis of ESR that is required from the expression (a). ΔV_{PP} can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. The ceramic capacitor contributes to the size reduction of the set because it has small ESR. Please confirm frequency characteristic of ESR from the datasheet of the manufacturer, and consider ESR value is low in the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is remarkable. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R and X5R or more is recommended. Because the voltage rating of a mass ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, please select electrolytic capacitor. Please consider having a voltage rating of 1.2 times or more of the output voltage when using electrolytic capacitor. Electrolytic capacitors have a high voltage rating, large capacity, small amount of DC biasing characteristic, and are generally cheap. Because main failure mode is OPEN, it is effective to use electrolytic capacitor for applications when reliability is required such as in-vehicle. But there are disadvantages such as, ESR is relatively high, and decreases capacitance value at low temperatures. In this case, please take note that ΔV_{PP} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor because there is a possibility for it to dry up.

These capacitors are rated in ripple current. The RMS values of the ripple electric current obtained in the next expression must not exceed the ratings ripple electric current.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad [A]$$

Where:
$I_{CO\ (RMS)}$ is the value of the ripple electric current

In addition, with respect to C_O, choose capacitance value less than the value obtained by the following equation.

$$C_{O(MAX)} = \frac{T_{SS(MIN)} \times (I_{OLIMIT(MIN)} - I_{OSTART(MAX)})}{V_O} \quad [F]$$

Where:
$I_{SWLIMIT\ (MIN)}$ is the OCP operation switch current (Min)
$T_{SS\ (MIN)}$ is the Soft Start Time (Min)
$I_{SWSTART\ (MAX)}$ is the maximum output current of boot

There is a possibility that boot failure happens when the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup, and the output does not start. Please confirm this on the actual circuit. For stable transient response, the loop is dependent on the C_O. Please select after confirming the setting of the phase compensation circuit.

(3) Setting constant of capacitor C_{IN} / Cbulk input

The input capacitor is usually required for two types of decoupling: capacitors C_{IN} and bulk capacitors Cbulk. Ceramic capacitors with values 1 µF to 10 µF are necessary for the decoupling capacitor. Ceramic capacitors are effective by being placed as close as possible to the VIN pin. Voltage rating is recommended to more than 1.2 times the maximum input voltage, or twice the normal input voltage. The bulk capacitor prevents the decrease in the line voltage and serves a backup power supply to keep the input potential constant. The low ESR electrolytic capacitor with large capacity is suitable for the bulk capacitor. It is necessary to select the best capacitance value as per set of application. When impedance on the input side is high because of wiring from the power supply to VIN is long, etc., and then high capacitance is needed. In actual conditions, it is necessary to verify that there is no problem when IC operation turns off the output due to the decrease in V_{IN} at transient response. In that case, please consider not to exceed the rated ripple current of the capacitor. The RMS value of the input ripple electric current is obtained in the next expression.

$$I_{CIN(RMS)} = I_{O(MAX)} \cdot \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \quad [A]$$

Where:
$I_{CIN\ (RMS)}$ is the RMS value of the input ripple electric current

In addition, in automotive and other applications requiring high reliability, it is recommended that capacitors are connected in parallel to accommodate a multiple of electrolytic capacitors to minimize the chances of drying up. It is recommended by making it into two series + two parallel structures to decrease the risk of ceramic capacitor destruction due to short circuit conditions. The line has been improved to the summary respectively by 1pack in each capacitor manufacturer and confirms two series and two parallel structures to each manufacturer.

(4) Setting output voltage

Output voltage is governed by the following equation.

$$V_O = 0.8 \times \frac{R_1+R_2}{R_2} \quad [V]$$

Please set feedback resistor R2 below 30 kΩ to reduce the error margin by the bias current. In addition, since power efficiency is reduced with a small R1 + R2, please set the current flowing through the feedback resistor to be small as possible than the output current I_O.

(5) Selection of the schottky barrier diode

The schottky barrier diode that has small forward voltage and short reverse recovery time is used for D1. The important parameters for the selection of the schottky barrier diode are the average rectified current and direct current inverse-direction voltage. Average rectified current $I_{F\,(AVG)}$ is obtained in the next expression:

$$I_{F(AVG)} = I_{O(MAX)} \times \frac{V_{IN(MAX)}-V_O}{V_{IN(MAX)}} \quad [A]$$

Where:

$I_{F\,(AVE)}$ is the average rectified current

The absolute maximum rating of the schottky barrier diode rectified current average is more than 1.2 times $I_{F(AVG)}$ and the absolute maximum rating of the DC reverse voltage is greater than or equal to 1.2 times the maximum input voltage. The loss of D1 is obtained in the next expression:

$$P_{Di} = I_{O(MAX)} \times \frac{V_{IN(MAX)}-V_O}{V_{IN(MAX)}} \times VF \quad [W]$$

Where:

VF is the forward voltage in $I_{o\,(MAX)}$ condition

Selecting a diode that has small forward voltage, and short reverse recovery time is highly effective. Please select a diode with 0.6 V Max of forward voltage. Please note that there is possibility of internal element destruction when a diode with a larger VF than this is used. Because the reverse recovery time of the schottky barrier diode is so short, that it is possible to disregard, the switching loss can be disregarded. When it is necessary for the diode to endure the state of output short-circuit, power dissipation ratings and the heat radiation ability are needed to be considered. The rated current that is required is about 1.5 times the overcurrent detection value.

(6) Setting the oscillating frequency

The internal oscillating frequency can be set by connecting a resistor to RT.
The range that can be set is 50 kHz to 600 kHz, and the relation between resistance and the oscillation frequency is decided as shown in the figure below. When setting beyond this range, there is a possibility that there is no oscillation and IC operation cannot be guaranteed.

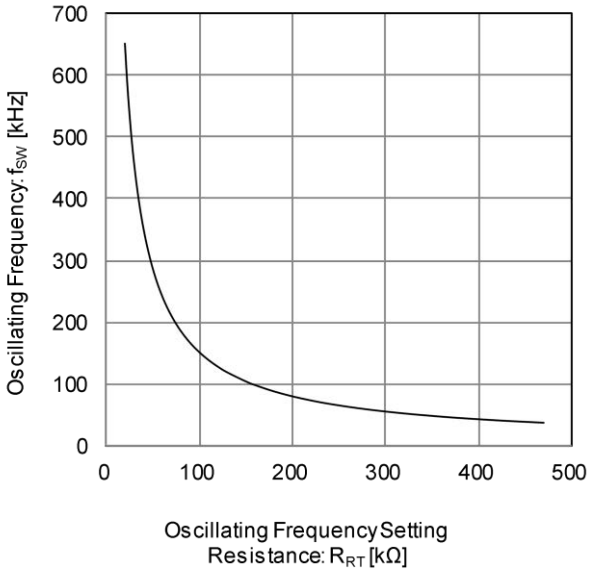


Figure 13. R_{RT} vs f_{SW}

R_{RT} [kΩ]	f_{SW} [kHz]
22	599
24	555
27	500
30	455
33	418
36	386
39	359
43	329
47	303
51	281
56	258
62	235
68	216
75	197
82	182
91	165

R_{RT} [kΩ]	f_{SW} [kHz]
100	151
110	139
120	128
130	119
150	104
160	98.
180	88
200	80
220	73
240	68
270	61
300	55
330	51

R_{RT} vs f_{SW}

(7) Setting the phase compensation circuit

A good high frequency response performance is achieved by setting the 0 dB crossing frequency, fc, (frequency at 0 dB gain) high. However, you need to be aware of the relationship trade-off between speed and stability. Moreover, DC / DC converter application is sampled by switching frequency, so the gain of this switching frequency must be suppressed. It is necessary to set the 0 dB crossing frequency to 1 / 10 or less of the switching frequency. In summary, target these characteristics as follows:

- When the gain is 1 (0 dB), phase lag is less than or equal to 135 ˚(More than 45 ˚ phase margin).
- 0 dB crossing frequency is 1 / 10 times or less of the switching frequency. To improve the responsiveness, higher the phase compensation is set by the capacitor and resistor which are connected in series to the VC pin.

Achieving stability by using the phase compensation is done by cancelling the fp_1 and fp_2 (error amp pole and power stage pole) of the regulation loop by use of fz_1. fp_1, fp_2 and fz_1 are determined in the following equations.

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} \quad [\mathrm{Hz}]$$

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_O} \quad [\mathrm{Hz}]$$

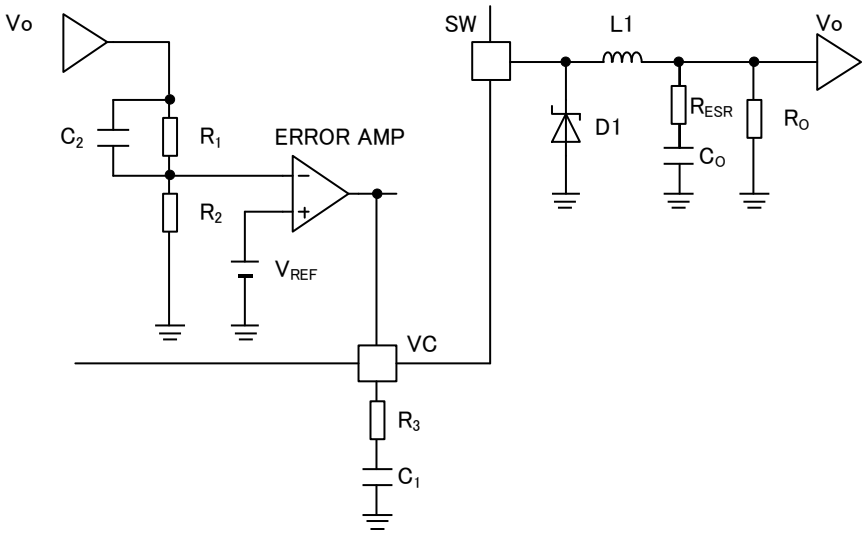
$$f_{P2} = \frac{G_{EA}}{2\pi \times C_1 \times A_V} \quad [\mathrm{Hz}]$$

Also, by inserting a capacitor in C2, phase lead fz2 can be added.

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C2} \quad [\mathrm{Hz}]$$

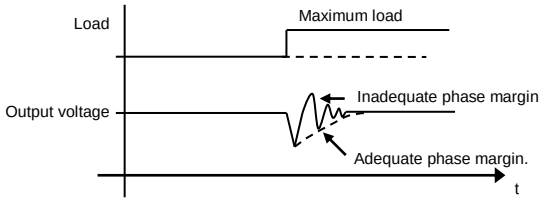
Where:

G_{EA} is the Error Amp trans conductance (270 µA / V)
A_V is the Error Amp Voltage Gain (78 dB)



Setting Phase Compensation Circuit

Actually, the changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and layout of the PCB.
Please confirm stability and responsiveness in actual equipment.
To check the actual frequency characteristics, use a FRA or a gain-phase analyzer. Moreover, the method of observing the degree of change by the loading response can be performed when these measuring instruments are not available. The phase margin degree is said to be low when there are lots of variation quantities after the output is made to change under no load to maximum load. It can also be observed that the phase margin degree is low when there is a lot of ringing frequencies after the transition of no load to maximum load, usually two times or more ringing than the standard. However, a quantitative phase margin degree cannot be confirmed.



Measurement of Frequency Characteristic

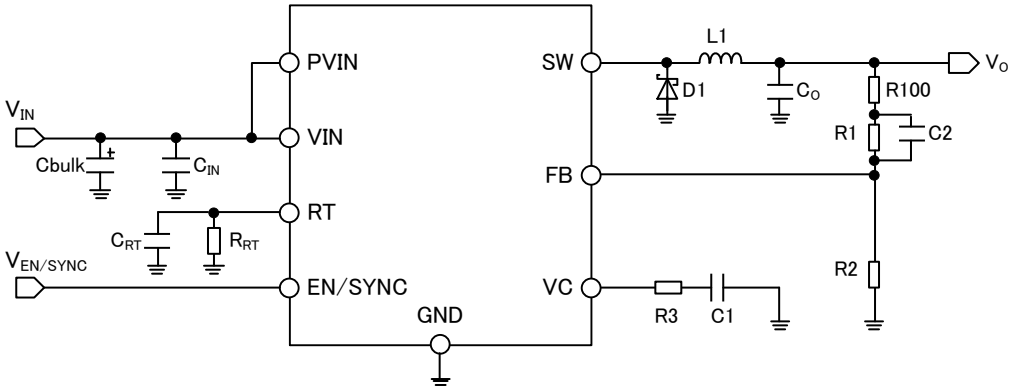
(8) Setting of soft start time (T_{SS})
The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at startup.
T_{SS} will be changed by setting the oscillating frequency.
The production tolerance of T_{SS} is 18.1%.T_{SS} can be calculated by using the equation.

$$T_{SS} = \frac{690.8}{f_{SW}} \quad [s]$$

Application Examples

Parameter	Symbol	Specification case
Product Name	IC	BD90640EFJ-C
Input Voltage	V_{IN}	6 V to 36 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C to 105°C

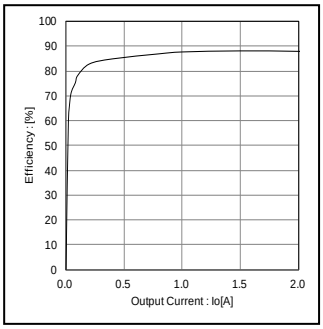
Specification Example 1



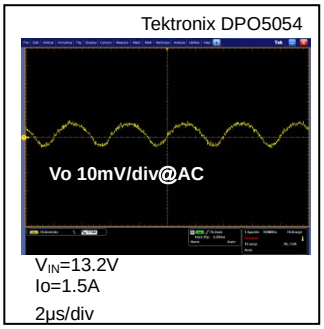
Reference Circuit 1

No	Package	Parameters	Part name(series)	Type	Manufacturer
R1	1608	43 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R2	1608	8.2 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R3	1608	33 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
C1	1608	3300 pF, R, 50 V	GCM series	Ceramic capacitors	MURATA
C2	-	OPEN	-	-	-
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitors	MURATA
C_{IN}	3216	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitors	MURATA
C_O	3216	22 µF, X7R, 10 V × 2	GCM series	Ceramic capacitors	MURATA
Cbulk	-	220 µF, 50 V	CD series	Electrolytic capacitors	NICHICON
L1	W 9.7 x H 4.5 x L 10 mm^3	4.7 µH	CLF10040 series	Coil	TDK
D1	PMDS	Average I = 3 A Max	RB050L-40	Schottky Diodes	ROHM

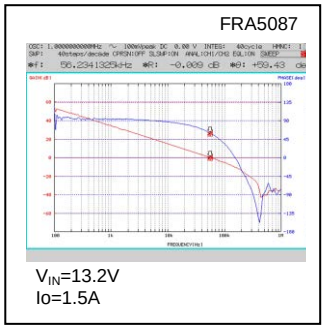
Parts List 1



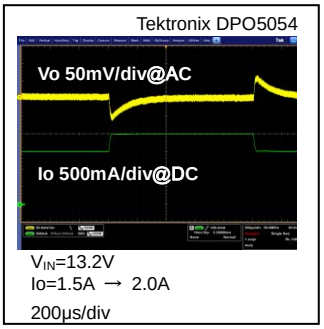
Conversion Efficiency



Output Ripple Voltage



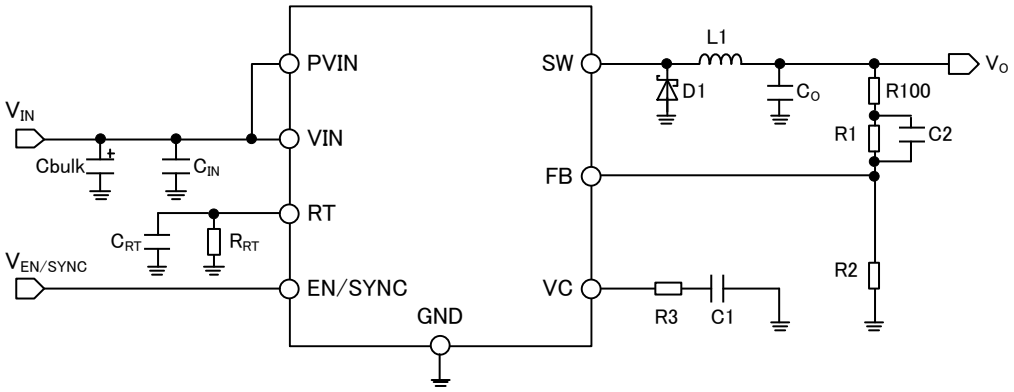
Frequency Character



Load Change

Parameter	Symbol	Specification case
Product Name	IC	BD90640EFJ-C
Input Voltage	V_{IN}	3.5 V to 20 V
Output Voltage	V_O	3.3 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C to 125 °C

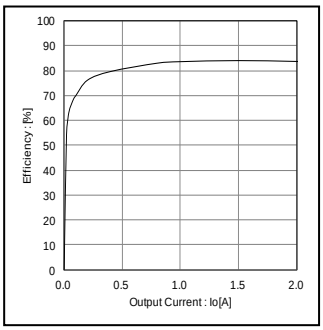
Specification Example 2



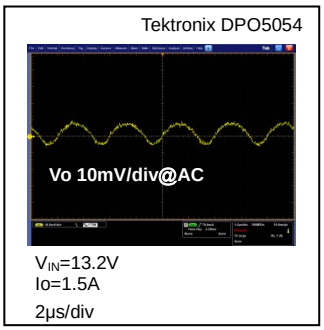
Reference Circuit 2

No	Package	Parameters	Part name(series)	Type	Manufacturer
R1	1608	47 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R2	1608	15 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R3	1608	6.8 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 16 W	MCR01 series	Chip resisters	ROHM
C1	1608	3300 pF, R, 50 V	GCM series	Ceramic capacitors	MURATA
C2	-	OPEN	-	-	-
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitors	MURATA
C_{IN}	3216	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitors	MURATA
C_O	3216	22 µF, X7R, 10 V × 2	GCM series	Ceramic capacitors	MURATA
Cbulk	-	220 µF, 50 V	CD series	Electrolytic capacitors	NICHICON
L1	W 9.7 x H 4.5 x L 10 mm^3	4.7 µH	CLF10040 series	Coil	TDK
D1	PMDS	Average I = 3 A Max	RB050L-40	Schottky Diodes	ROHM

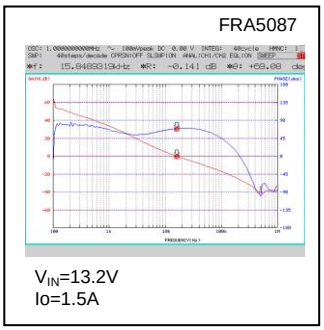
Parts List 2



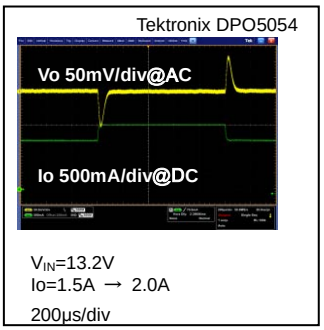
Conversion Efficiency



Output Ripple Voltage



Frequency Characteristics



Load Change

Input Filter

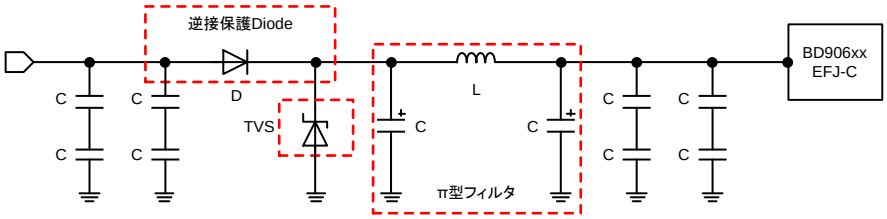


Figure 14. Filter Circuit

The input filter circuit for EMC measures is depicted in the above Figure 14.

The π type filters are the three-element LC filters. When the decoupling capacitor for high frequency is insufficient, it uses π type filters.

Because a large attenuation characteristic is obtained, an excellent characteristic can be obtained using an EMI filter. TVS (Transient Voltage Suppressors) are used for the first protection of the in-vehicle power supply line. Because it is necessary to endure high energy when the load is connected, a general zener diode is insufficient. The following are recommended. To protect it when the power supply such as BATTERY is accidentally connected in reverse, reverse polarity protection diode is needed.

Device	Part name(series)	Manufacturer
L	CLF series	TDK
L	XAL series	Coilcraft
C	CJ series	NICHICON
C	CZ series	NICHICON
TVS	SM8 series	VISHAY
D	S3A thru S3M series	VISHAY

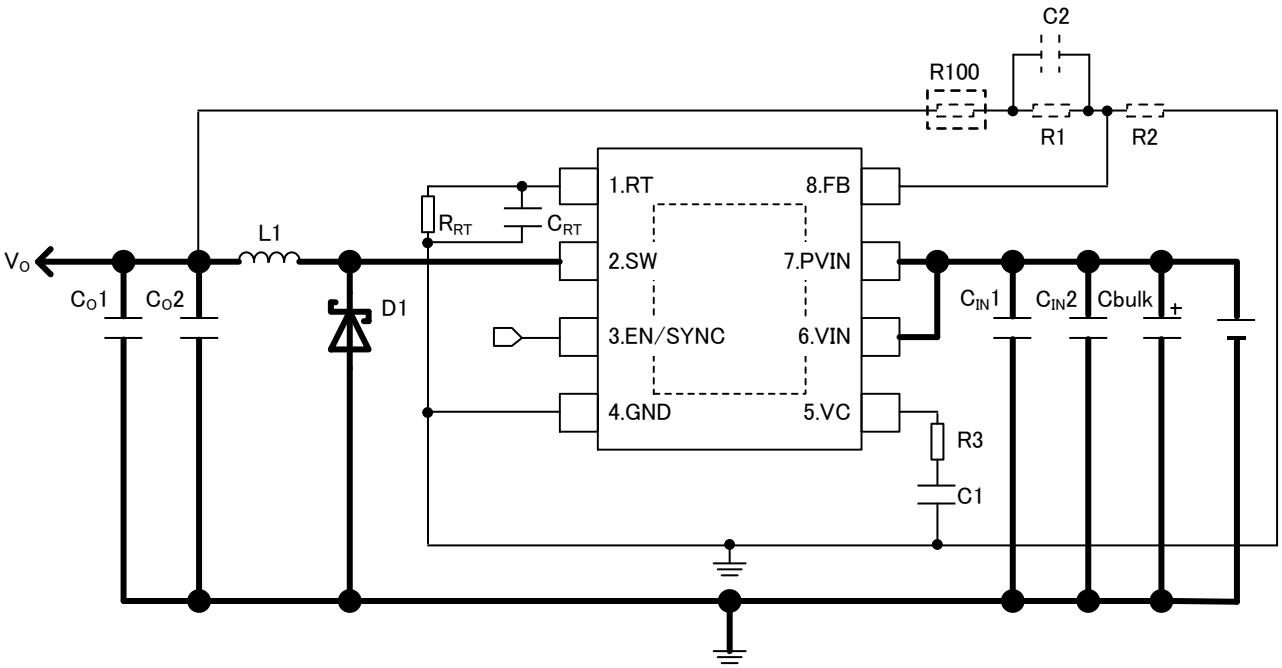
Parts of Filter Circuit

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Device	Type	Manufacturer	URL
C	Electrolytic capacitors	NICHICON	www.nichicon.com
C	Ceramic capacitors	MURATA	www.murata.com
L	Coils	TDK	www.global.tdk.com
L	Coils	Coilcraft	www.coilcraft.com
L	Coils	Sumida	www.sumida.com
D	Diodes	VISHAY	www.vishay.com
D	Diodes/Resisters	ROHM	www.rohm.com

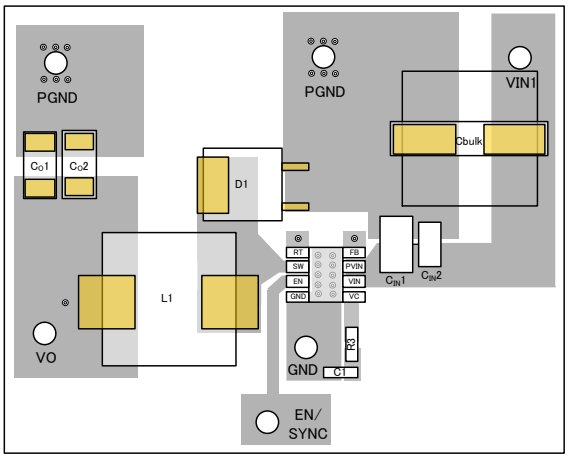
Directions for Pattern Layout of PCB



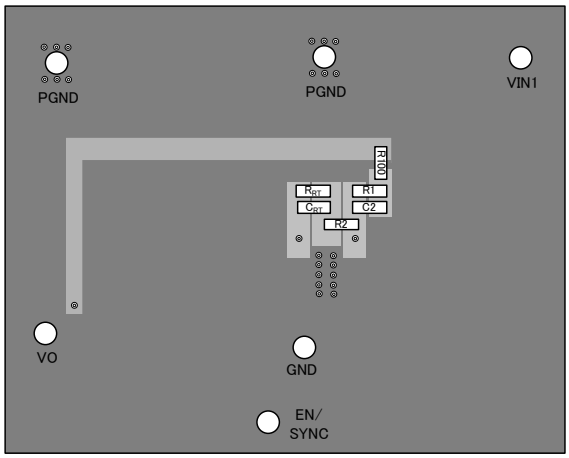
Exposed die pad is needed to be connected to GND.

Application Circuit

① Arrange the wirings of the wide lines, shown above, as short as possible in a broad pattern.
② Locate the input ceramic capacitor C_{IN} as close to the VIN - GND pin as possible.
③ Locate R_{RT} as close to the RT pin as possible.
④ Locate R1 and R2 as close to the FB pin as possible, and provide the shortest wiring from the R1 and R2 to the FB pin.
⑤ Locate R1 and R2 as far away from the L1 as possible.
⑥ Separate Power GND (schottky diode, I/O capacitor`s GND) and Signal GND (R_T, VC), so that SW noise does not have an effect on SIGNAL GND at all.
⑦ The feedback frequency characteristics (phase margin) can be measured using FRA by inserting a resistor at the location of R100. However, this should be shorted during normal operation. R100 is option pattern for measuring the feedback frequency characteristics.



Reference Layout Pattern (Top View)



Reference Layout Pattern (Bottom View)

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

①To obtain Tj from the IC surface temperature Tc in actual use

$$Tj = Tc + \theta jc \times W$$

②To obtain Tj from the ambient temperature Ta

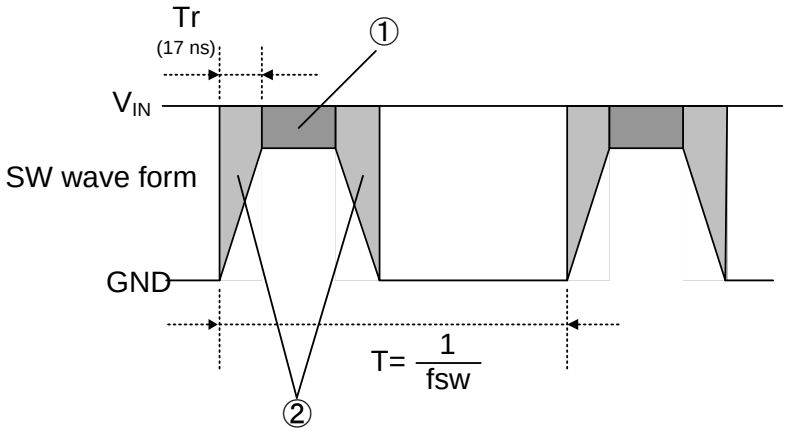
$$Tj = Ta + \theta ja \times W$$

<Reference Value> θja : HTSOP-J8
249.5 °C / W Single piece of IC
153.2 °C / W 1-layer PCB
113.6 °C / W 2-layer PCB (Copper foil area on the front side of PCB: 15mm x 15mm)
59.2 °C / W 2-layer PCB (Copper foil area on the front side of PCB: 70mm x 70mm)
33.3 °C / W 4-layer PCB (Copper foil area on the front side of PCB : 70mm x 70mm)
PCB Size: 70mm x 70mm x 1.6mm (PCB incorporates thermal via)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ON} \times {I_O}^2 \times \frac{V_O}{V_{IN}} + V_{IN} \times I_{CC} + Tr \times V_{IN} \times I_O \times fsw$$

Where:
R_{ON} is the ON Resistance of IC (Refer to page 7) [Ω]
I_O is the Load Current [A]
V_O is the Output Voltage [V]
V_{IN} is the Input Voltage [V]
I_{CC} is the Circuit Current (Refer to page 7) [A]
Tr is the Switching Rise Time [S]
fsw is the Oscillating Frequency [Hz]



SW Wave Form

$$①\ R_{ON} \times {I_O}^2$$

$$②\ 2 \times \frac{1}{2} \times Tr \times V_{IN} \times I_O \times \frac{1}{T}$$

$$= Tr \times V_{IN} \times I_O \times fsw$$

Thermal reduction characteristics

HTSOP-J8

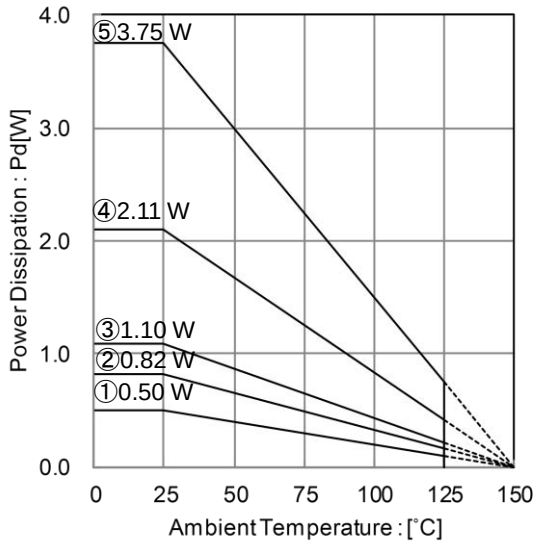


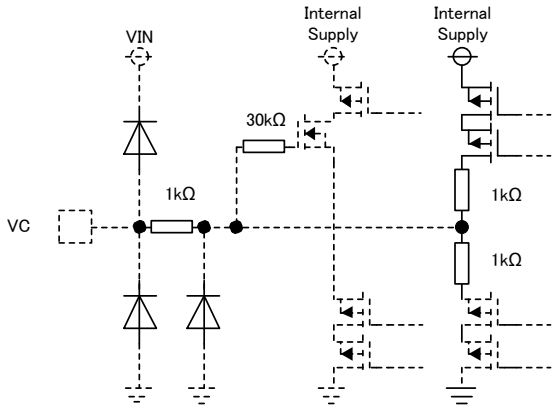
Figure 15. Thermal Reduction Characteristics

① Standalone IC
② Mounted on ROHM standard board (1-layer PCB)
③ Mounted on ROHM standard board (2-layer PCB Copper foil area on the front side of PCB: 15 mm × 15 mm)
④ Mounted on ROHM standard board (2-layer PCB Copper foil area on the front side of PCB: 70 mm × 70 mm)
⑤ Mounted on ROHM standard board (4-layer PCB Copper foil area on the front side of PCB: 70 mm × 70 mm)

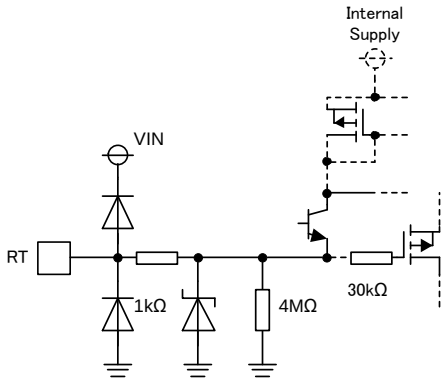
PCB Size: 70mm×70mm×1.6mm (PCB incorporates thermal via)

I/O Equivalent Circuit

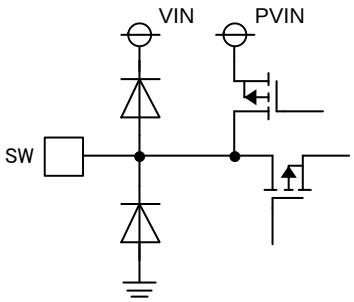
VC



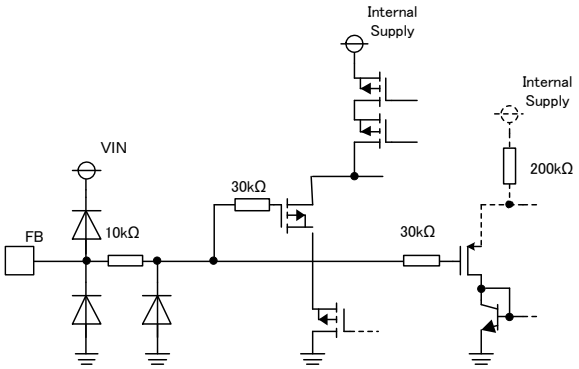
RT



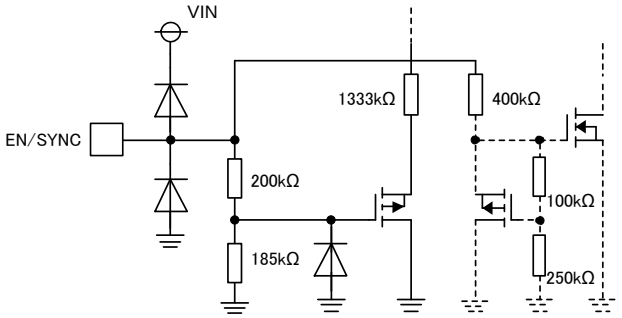
SW



FB



EN / SYNC



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

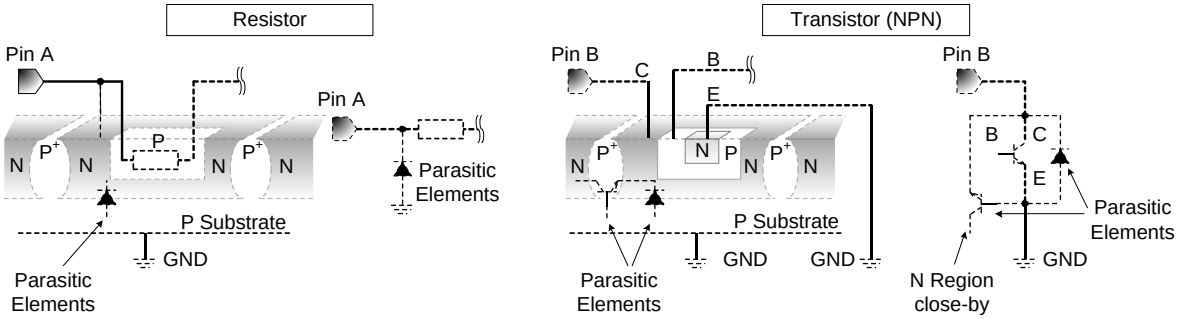
Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

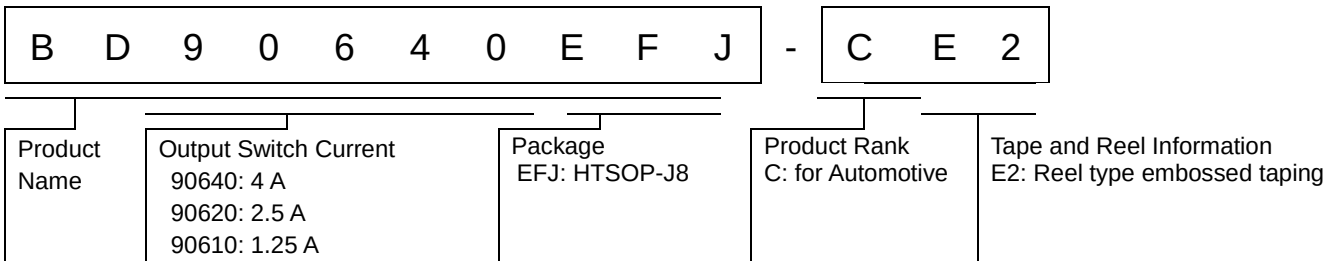
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

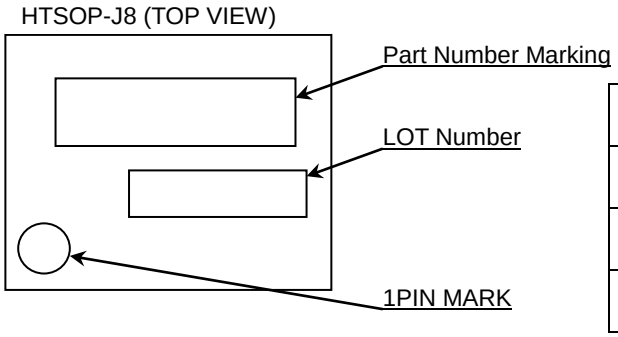
16. Over Current Protection Circuit (OCP)

This IC has a built-in overcurrent protection circuit that activates when the output is accidentally shorted. However, it is strongly advised not to subject the IC to prolonged shorting of the output.

Ordering Information



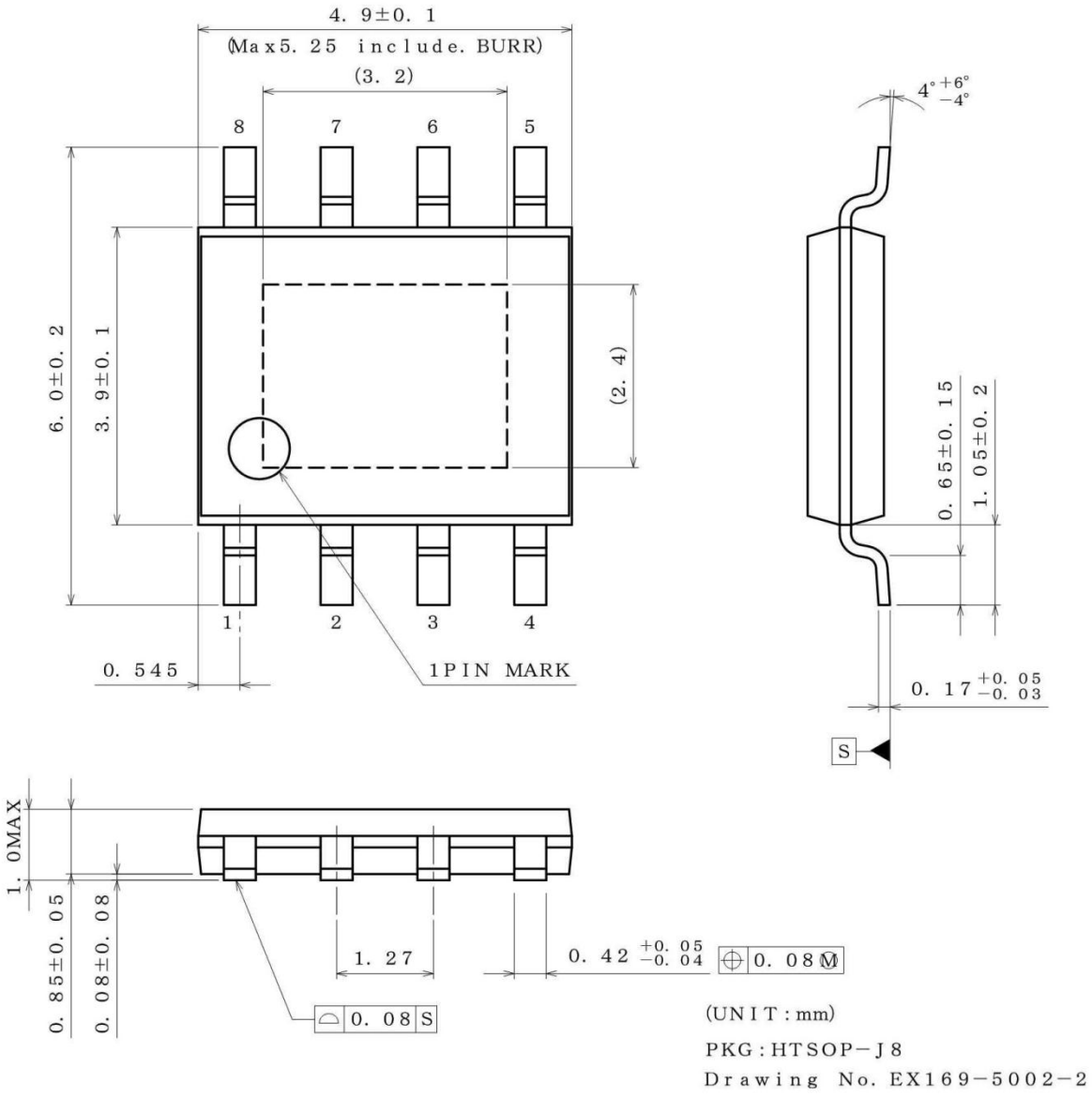
Marking Diagram



Output Switch Current	Part Number Marking
4 A	D90640
2.5 A	D90620
1.25 A	D90610

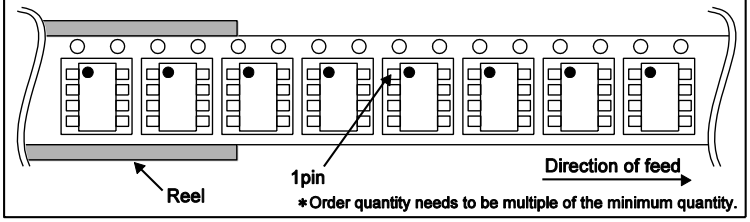
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
06.Jan.2014	001	New Release
07.Apr.2014	002	P.4 Description of OCP remove sentence “Furthermore ~” P.6 Operating Output Switch Current Of Overcurrent Protection symbol change $I_{SWLIMIT}$. P.18 Parts List D1 Package change “PMDS” P.19 Parts List C2 change “open” P.21 About Directions for Pattern Layout of PCB ⑥ change “～and Signal GND (R_T, VC,),～”

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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