

## Revision History

### Version 0.0 (June 1998)

- The 4th. generation of 16M DRAM components are applied for this module.

## KMM466F104CT1-L & KMM466F124CT1-L EDO Mode

1M x 64 DRAM SODIMM using 1Mx16, 1K/4K Refresh 3.3V, Low power/Self-Refresh

### GENERAL DESCRIPTION

The Samsung KMM466F10(2)4CT1-L is a 1Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F10(2)4CT1-L consists of four CMOS 1Mx16bits DRAMs in TSOP 400mil packages and 1K or 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F10(2)4CT1-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

### PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-L5	50ns	15ns	84ns	20ns
-L6	60ns	17ns	104ns	25ns

### FEATURES

- Part Identification
  - KMM466F104CT1-L(4096 cycles/128ms, TSOP, L-ver)
  - KMM466F124CT1-L(1024 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- CAS-before-RAS Refresh capability
- Self -refresh capability
- RAS-only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

### PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	W	68	RFU	115	CAS2	116	CAS6
21	Vss	22	Vss	69	RAS0	70	RFU	117	CAS3	118	CAS7
23	CAS0	24	CAS4	71	NC	72	RFU	119	Vss	120	Vss
25	CAS1	26	CAS5	73	OE	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	**SDA	142	**SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

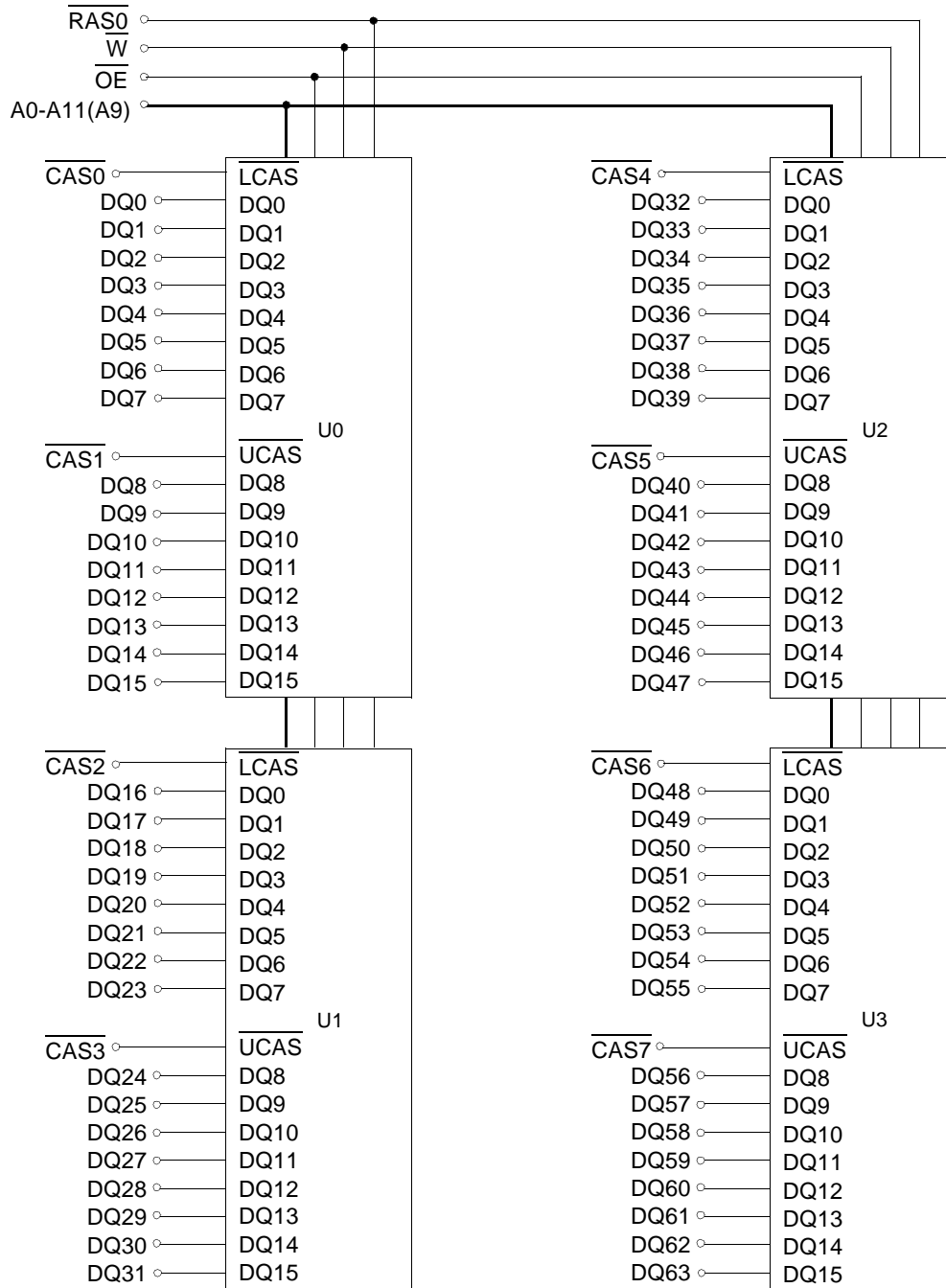
Note : A11 & A10 are used for only KMM466F104CT1-L (4K ref.)

### PIN NAMES

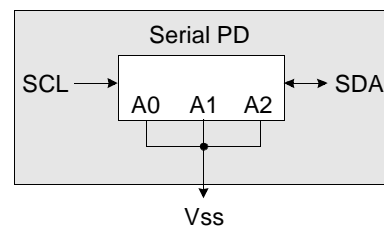
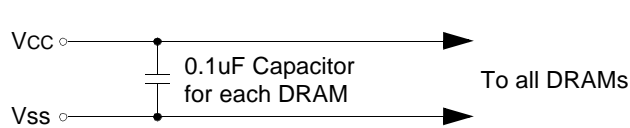
Pin Name	Function
A0 to 11	Address Inputs (4K ref.)
A0 to A9	Address Inputs (1K ref.)
DQ0 - DQ63	Data In/Out
W	Read/Write Enable
OE	Output Enable
RAS0	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
**SDA	Serial Address / Data I/O
**SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

- \* These pins are not used in this module.
- \*\* These pins should be NC in the system which does not support SPD.

## FUNCTIONAL BLOCK DIAGRAM



\* A10 & A11 are used for only KMM466F104CT1-L (4K ref.)



## ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to +4.6	V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C
Power Dissipation	P <sub>D</sub>	4	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V<sub>SS</sub>, T<sub>A</sub> = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3* <sup>1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.3* <sup>2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+1.3V at pulse width ≤15ns, which is measured at V<sub>CC</sub>.

\*2 : -1.3V at pulse width ≤15ns, which is measured at V<sub>SS</sub>.

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F104CT1-L		KMM466F124CT1-L		Unit
		Min	Max	Min	Max	
I <sub>CC1</sub>	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I <sub>CC2</sub>	Don't care	-	4	-	4	mA
I <sub>CC3</sub>	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I <sub>CC4</sub>	-L5	-	400	-	400	mA
	-L6	-	360	-	360	mA
I <sub>CC5</sub>	Don't care	-	0.8	-	0.8	mA
I <sub>CC6</sub>	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I <sub>CC7</sub>	Don't care	-	1.2	-	0.8	mA
I <sub>CC8</sub>	Don't care	-	0.6	-	0.6	mA
I <sub>I(L)</sub> I <sub>O(L)</sub>	Don't care	-20	20	-20	20	uA
		-5	5	-5	5	uA
V <sub>OH</sub> V <sub>OL</sub>	Don't care	2.4	-	2.4	-	V
		-	0.4	-	0.4	V

I<sub>CC1</sub>: Operating Current \* (R<sub>AS</sub>, C<sub>AS</sub>, Address cycling @t<sub>RC</sub>=min)

I<sub>CC2</sub>: Standby Current (R<sub>AS</sub>=C<sub>AS</sub>=W=V<sub>IH</sub>)

I<sub>CC3</sub>: R<sub>AS</sub> Only Refresh Current \* (C<sub>AS</sub>=V<sub>IH</sub>, R<sub>AS</sub> cycling @t<sub>RC</sub>=min)

I<sub>CC4</sub>: Extended Data Out Mode Current \* (R<sub>AS</sub>=V<sub>IL</sub>, C<sub>AS</sub> cycling : t<sub>HPC</sub>=min)

I<sub>CC5</sub>: Standby Current (R<sub>AS</sub>=C<sub>AS</sub>=W=V<sub>CC</sub>-0.2V)

I<sub>CC6</sub>: C<sub>AS</sub>-Before-R<sub>AS</sub> Refresh Current \* (R<sub>AS</sub> and C<sub>AS</sub> cycling @t<sub>RC</sub>=min)

I<sub>CC7</sub>: Battery back-up current. Average power supply, Battery back-up mode.

Input high voltage(V<sub>IH</sub>)=V<sub>CC</sub>-0.2V, Input low voltage(V<sub>IL</sub>)=0.2V, UC<sub>AS</sub>, LC<sub>AS</sub>=0.2V,

DQ=Don't care, t<sub>RC</sub>=31.25us, t<sub>RAS</sub>=t<sub>RASmin</sub>~300ns

I<sub>CC8</sub>: Self Refresh Current, R<sub>AS</sub>=UC<sub>AS</sub>=LC<sub>AS</sub>=V<sub>IL</sub>, W=OE=A0~A1=V<sub>CC</sub>-0.2V or 0.2V, DQ~DQ63=V<sub>CC</sub>-0.2V or Open

I<sub>I(L)</sub> : Input Leakage Current (Any input 0 ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>+0.3V, all other pins not under test=0 V)

I<sub>O(L)</sub>: Output Leakage Current(Data Out is disabled, 0V ≤ V<sub>OUT</sub> ≤ V<sub>CC</sub>)

V<sub>OH</sub>: Output High Voltage Level (I<sub>OH</sub> = -2mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 2mA)

\* NOTE : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while R<sub>AS</sub>=V<sub>IL</sub>. In I<sub>CC4</sub>, address can be changed maximum once within one page mode cycle, t<sub>HPC</sub>.

# DRAM MODULE

**KMM466F104CT1-L**  
**KMM466F124CT1-L**

## CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A9)]	CIN1	-	30	pF
Input capacitance[W, OE]	CIN2	-	38	pF
Input capacitance[RAS0]	CIN3	-	38	pF
Input capacitance[CAS0 - CAS7]	CIN4	-	17	pF
Input/Output capacitance[DQ0 - 63]	CDQ	-	17	pF

## AC CHARACTERISTICS (0°C≤TA≤70°C, See notes 1,2.)

Test condition : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	130		155		ns	
Access time from RAS	tRAC		50		60	ns	
Access time from CAS	tCAC		15		17	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
CAS to output in Low-Z	tCLZ	3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	15	ns	3,11
Transition time(rise and fall)	tT	2	50	2	50	ns	2
RAS precharge time	tRP	30		40		ns	
RAS pulse width	tRAS	50	10K	60	10K	ns	
RAS hold time	tRSH	15		17		ns	
CAS hold time	tCSH	40		50		ns	
CAS pulse width	tCAS	8	10K	10	10K	ns	
RAS to CAS delay time	tRCD	20	35	20	43	ns	4
RAS to column address delay time	tRAD	15	25	15	30	ns	9
CAS to RAS precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	12
Column address hold time	tCAH	8		10		ns	12
Column address to RAS lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		ns	7
Read command hold referenced to RAS	tRRH	0		0		ns	7
Write command set-up time	tWCS	0		0		ns	6
Write command hold time	tWCH	10		10		ns	6
Write command pulse width	tWP	10		10		ns	
Write command to RAS lead time	tRWL	13		15		ns	
Write command to CAS lead time	tCWL	8		10		ns	15
Data set-up time	tDS	0		0		ns	8
Data hold time	tDH	8		10		ns	8
Refresh period	tREF		128		128	ms	
CAS to W delay time	tCWD	38		42		ns	6,14
RAS to W delay time	tRWD	73		85		ns	6

## AC CHARACTERISTICS (Continued)

Test condition :  $V_{CC}=3.3V\pm 0.3V$ ,  $V_{ih}/V_{il}=2.2/0.7V$ ,  $V_{oh}/V_{ol}=2.0/0.8V$ , output loading  $CL=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	tAWD	48		55		ns	6
CAS precharge to $\overline{W}$ delay time	tCPWD	53		60		ns	6
CAS setup time (CAS-before-RAS refresh)	tCSR	5		5		ns	16
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		ns	
RAS to CAS precharge time	trPC	5		5		ns	
Access time from CAS precharge	tCPA		28		35	ns	3
Hyper page mode cycle time	tHPC	20		25		ns	10
Hyper page mode read-modify write cycle time	tHPRWC	68		77		ns	10
CAS precharge time (Hyper page cycle)	tCP	8		10		ns	13
RAS pulse width (Hyper page cycle)	trASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	trHCP	30		35		ns	
$\overline{OE}$ access time	toEA		13		15	ns	3
$\overline{OE}$ to data delay	toED	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	toEZ	3	13	3	15	ns	
$\overline{OE}$ command hold time	toEH	13		15		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	treZ	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	twez	3	13	3	15	ns	
$\overline{W}$ to data delay	twED	15		15		ns	
$\overline{OE}$ to CAS hold time	toCH	5		5		ns	
CAS hold time to $\overline{OE}$	tCHO	5		5		ns	
$\overline{OE}$ precharge time	toEP	5		5		ns	
$\overline{W}$ pulse width	twPE	5		5		ns	
RAS pulse width (C-B-R self refresh)	trASS	100		100		us	17,18,19
RAS precharge time (C-B-R self refresh)	trPS	90		110		ns	17,18,19
CAS hold time (C-B-R self refresh)	tCHS	-50		-50		ns	17,18,19

## NOTES

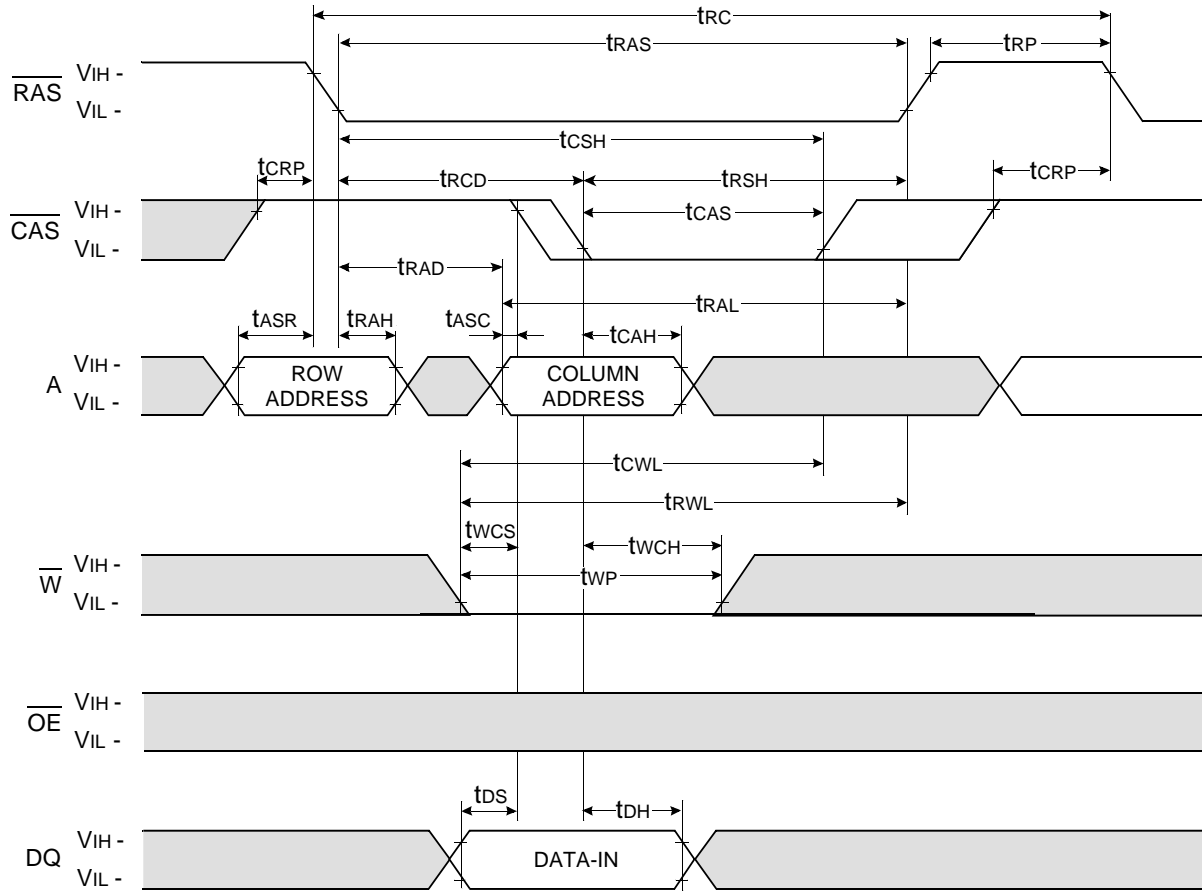
1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
6.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CPWD} \geq t_{CPWD}(\min)$ . The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
7. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
8. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles.
9. Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit access time is controlled by  $t_{AA}$ .
10.  $t_{ASC} \geq 6ns$ , Assume  $t_T = 2.0ns$
11. If  $\overline{RAS}$  goes high before  $\overline{CAS}$  high going, the open circuit condition of the output is achieved by CAS high going. If  $\overline{CAS}$  goes high before  $\overline{RAS}$  high going, the open circuit condition of the output is achieved by RAS going.
12.  $t_{ASC}$ ,  $t_{CAH}$  are referenced to the earlier  $\overline{CAS}$  falling edge.
13.  $t_{CP}$  is specified from the last  $\overline{CAS}$  rising edge in the previous cycle to the first  $\overline{CAS}$  falling edge in the next cycle.
14.  $t_{CWD}$  is referenced to the later  $\overline{CAS}$  falling edge at word read-modify-write cycle.
15.  $t_{CWL}$  is specified from  $\overline{W}$  falling edge to the earlier  $\overline{CAS}$  rising edge.
16.  $t_{CSR}$  is referenced to earlier  $\overline{CAS}$  falling low before  $\overline{RAS}$  transition low.
17. If  $t_{RASS} \geq 100us$ , then  $\overline{RAS}$  precharge time must use  $t_{RPS}$  instead of  $t_{RP}$ .
18. For  $\overline{RAS}$ -only refresh and burst  $\overline{CAS}$ -before- $\overline{RAS}$  refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
19. For distributed  $\overline{CAS}$ -before- $\overline{RAS}$  with 15.6us interval  $\overline{CAS}$ -before- $\overline{RAS}$  should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.





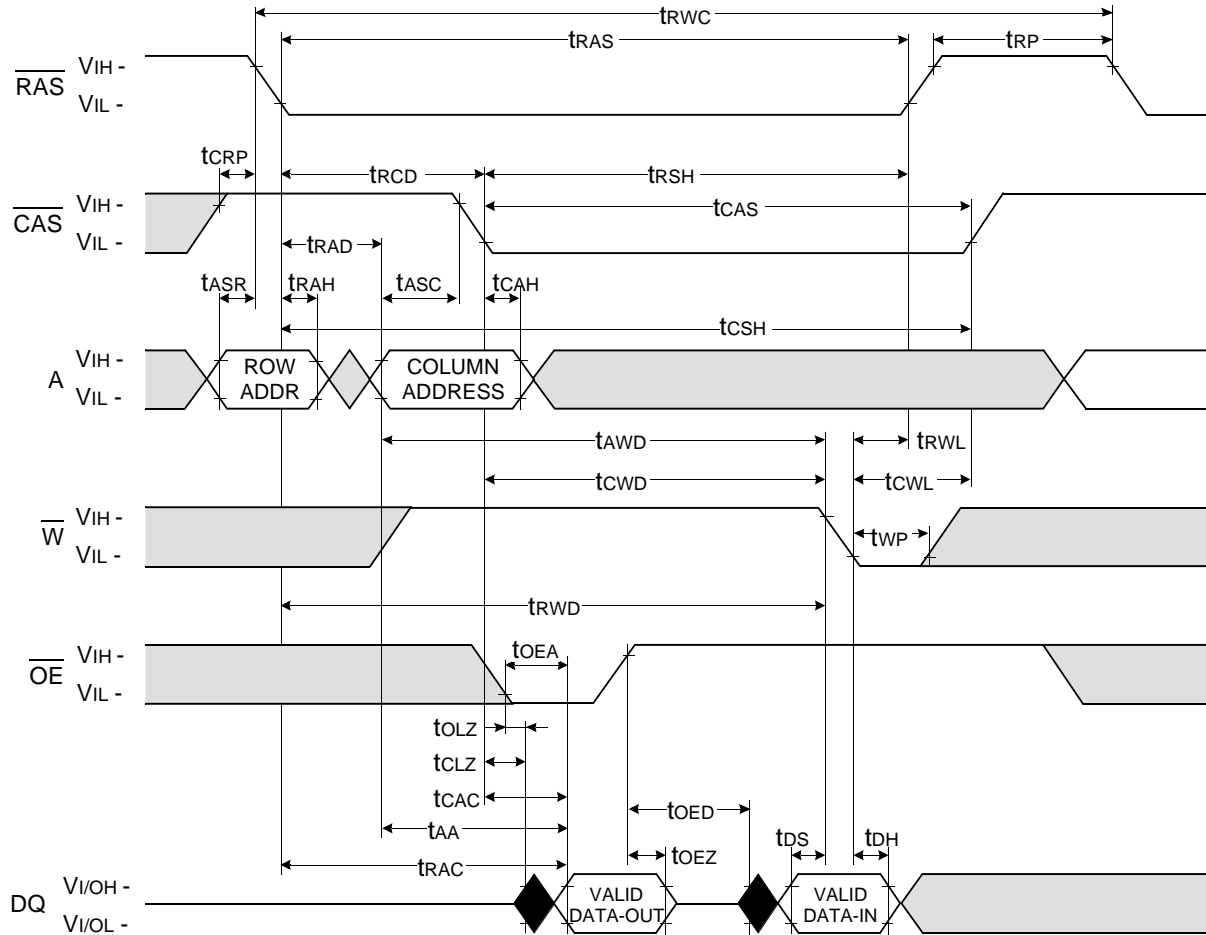
WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN





READ - MODIFY - WRITE CYCLE

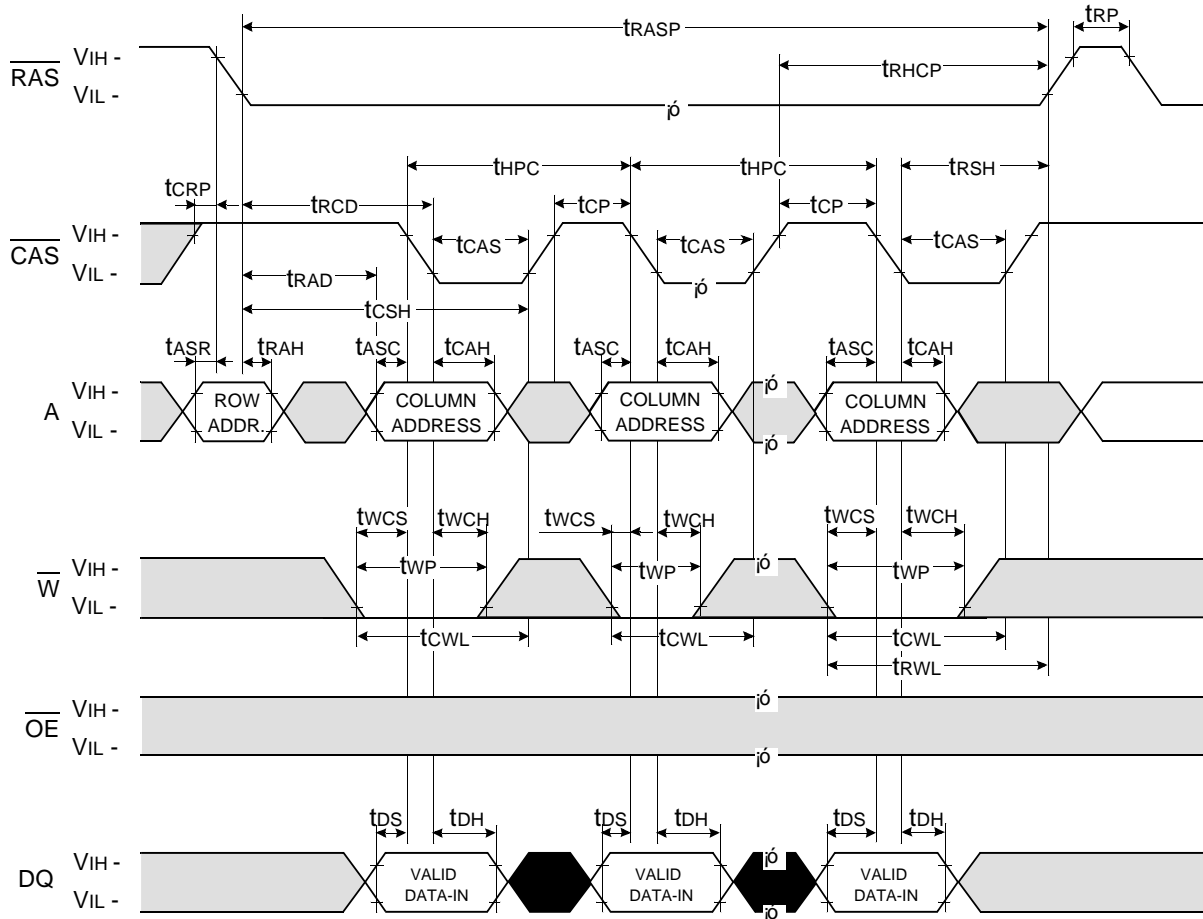


Don't care  
 Undefined



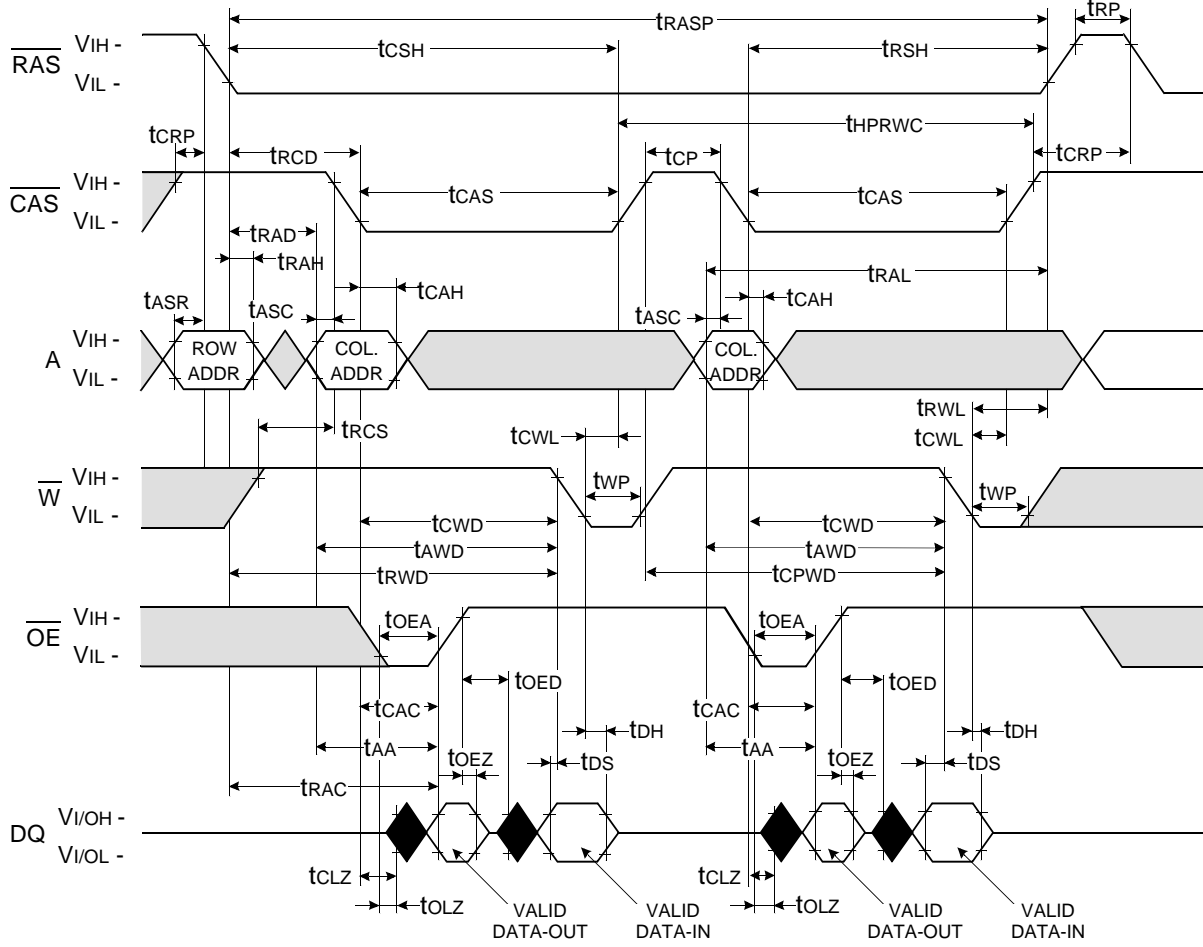
HYPER PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

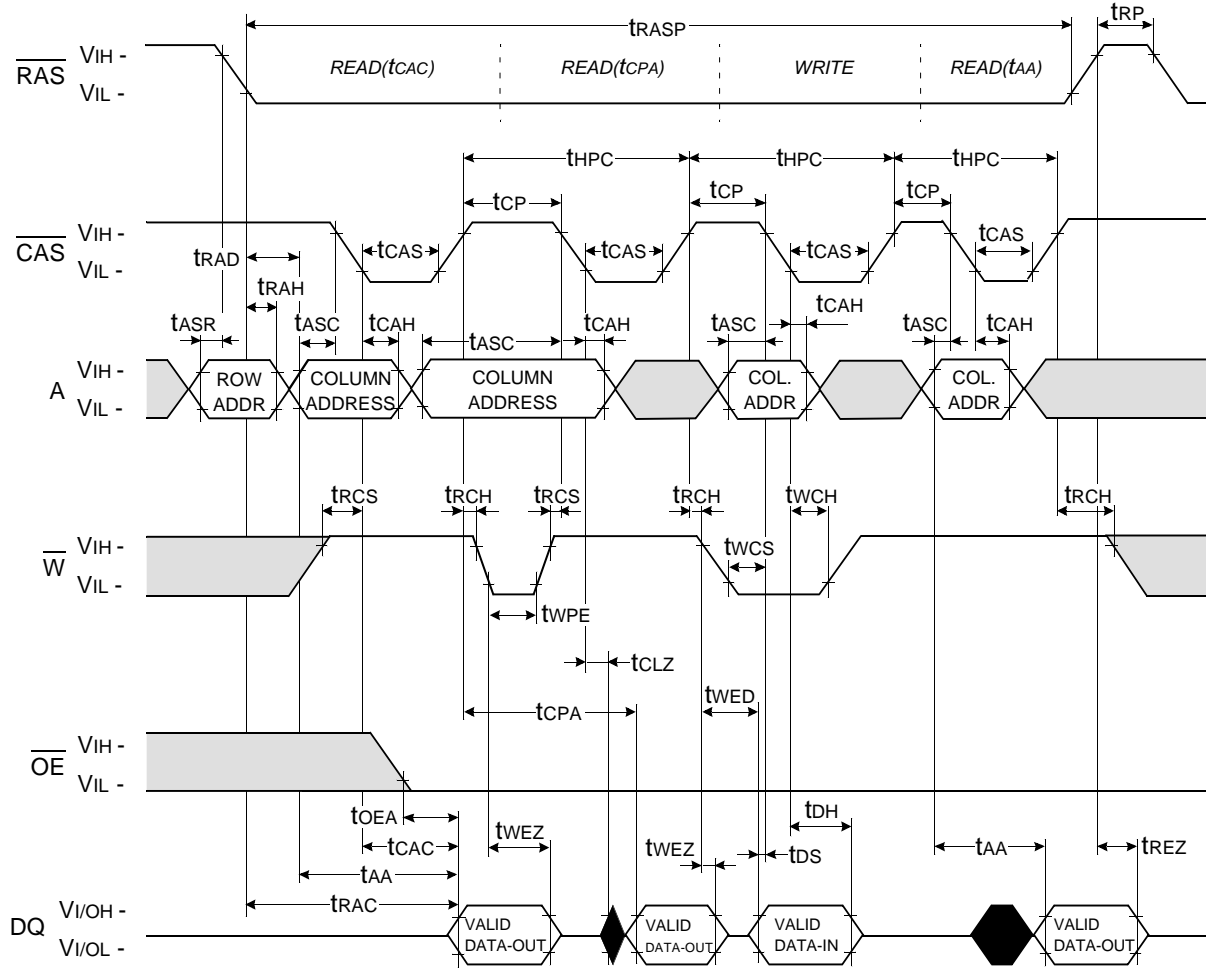


□ Don't care  
■ Undefined

HYPER PAGE READ-MODIFY-WRITE CYCLE



HYPER PAGE READ AND WRITE MIXED CYCLE

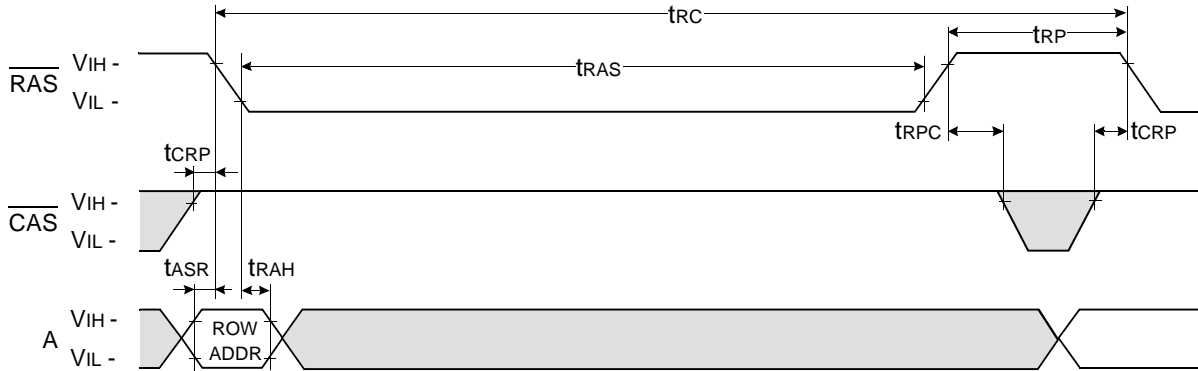


Don't care  
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**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE\***

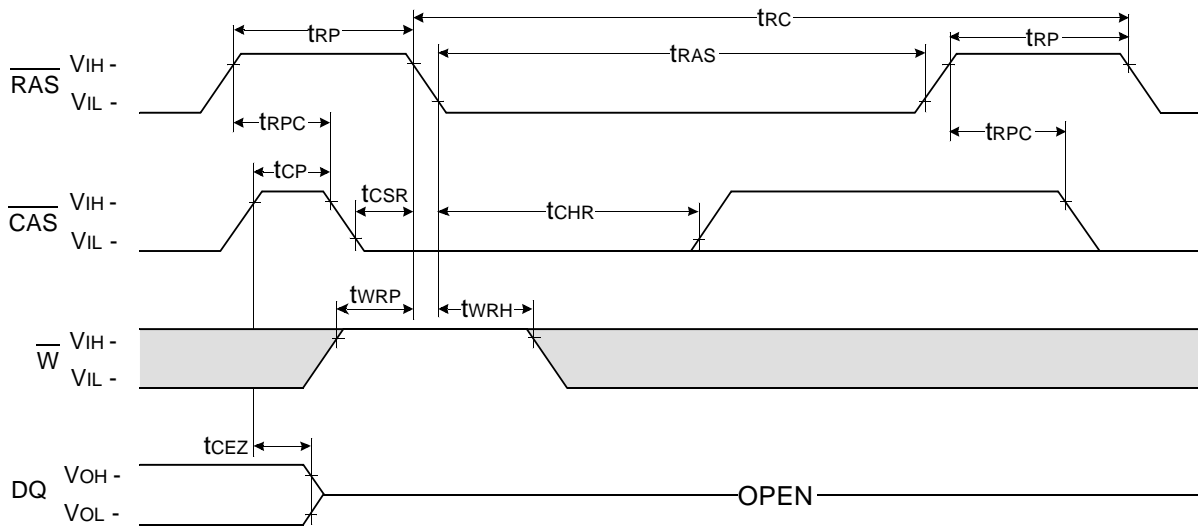
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ ,  $\text{DIN}$  = Don't care

$\text{DOUT}$  = OPEN



**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ ,  $\text{A}$  = Don't care

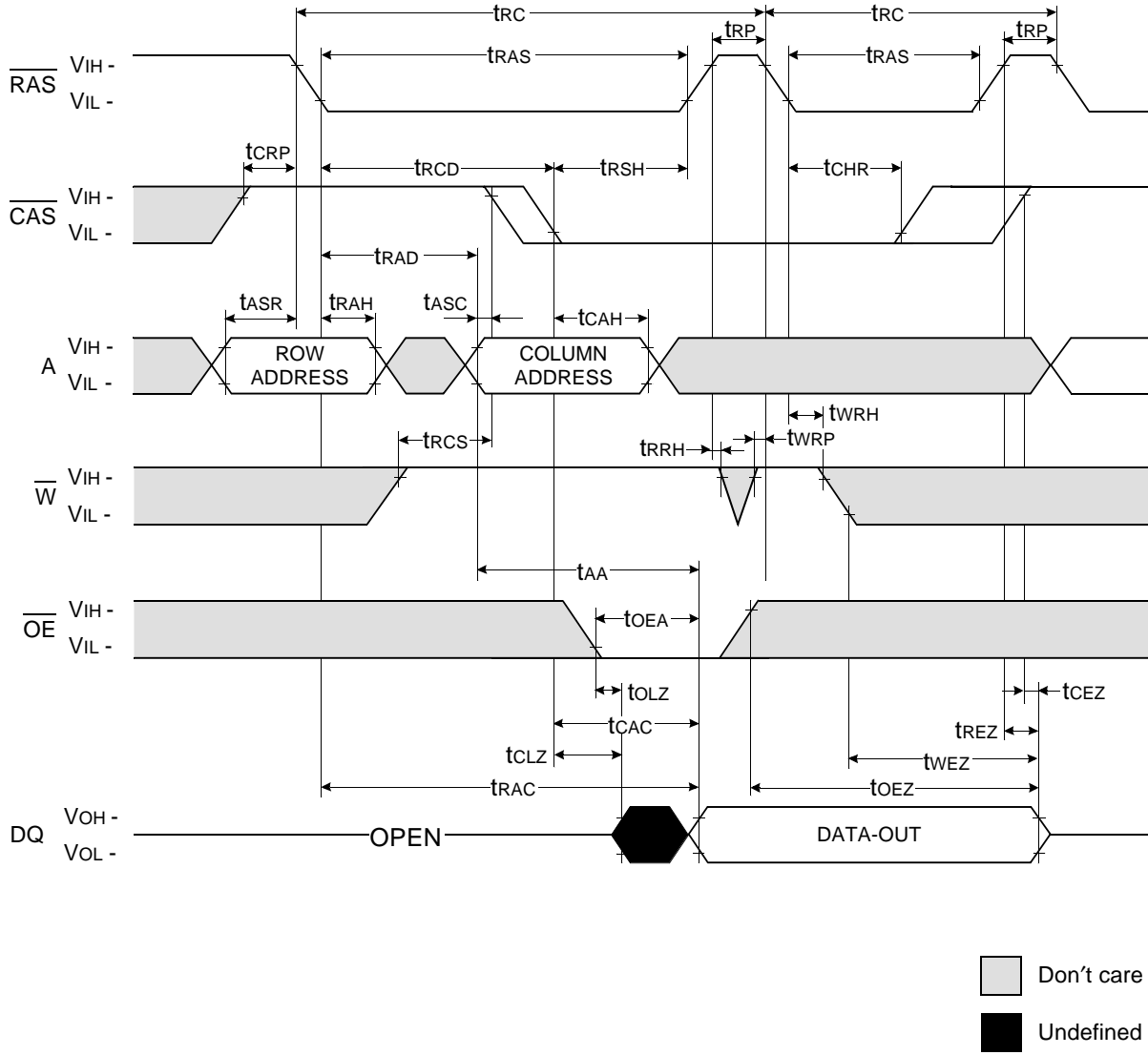


□ Don't care  
■ Undefined

\* In  $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when  $\overline{\text{CAS}}$  signal transits from Low to High, the valid data may be cut off.

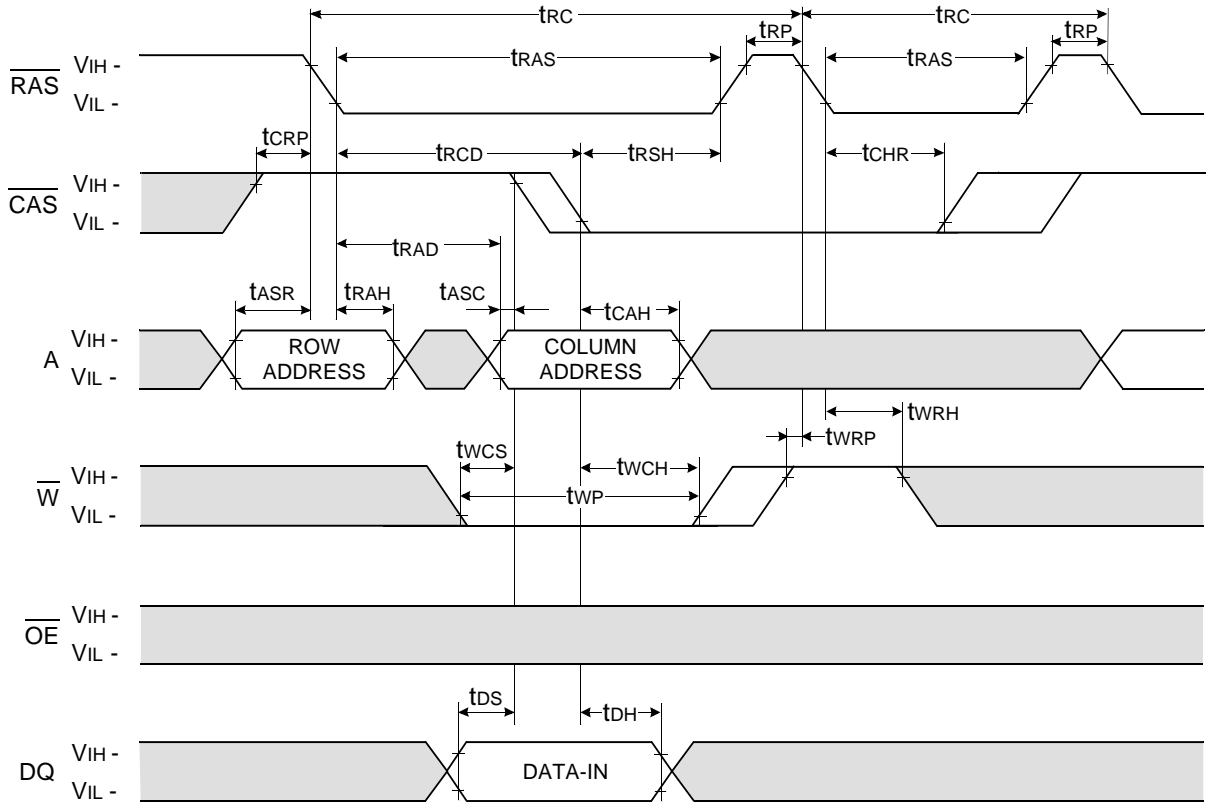


HIDDEN REFRESH CYCLE ( READ )



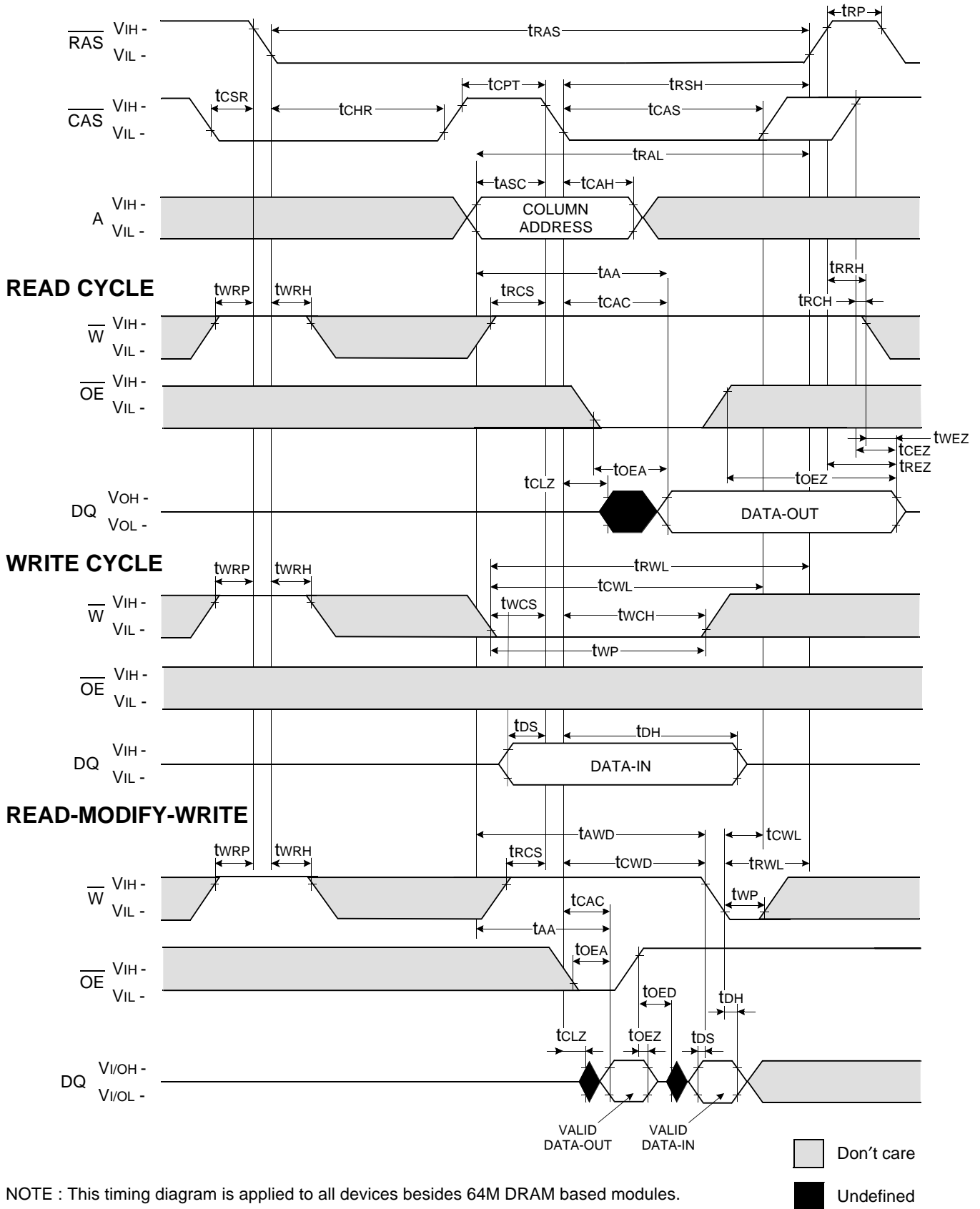
## HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



Don't care  
 Undefined

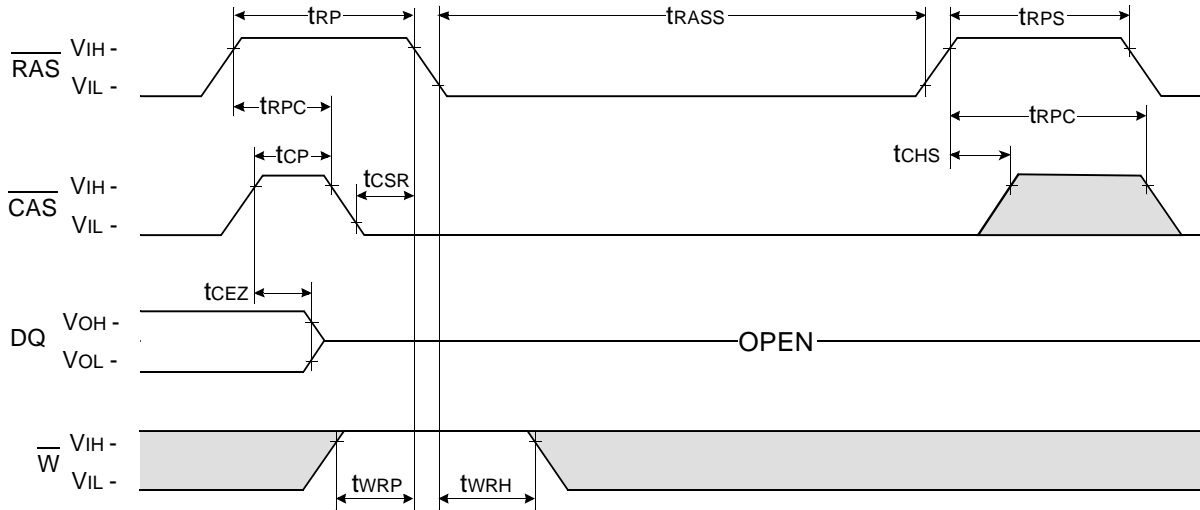
**CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE**



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

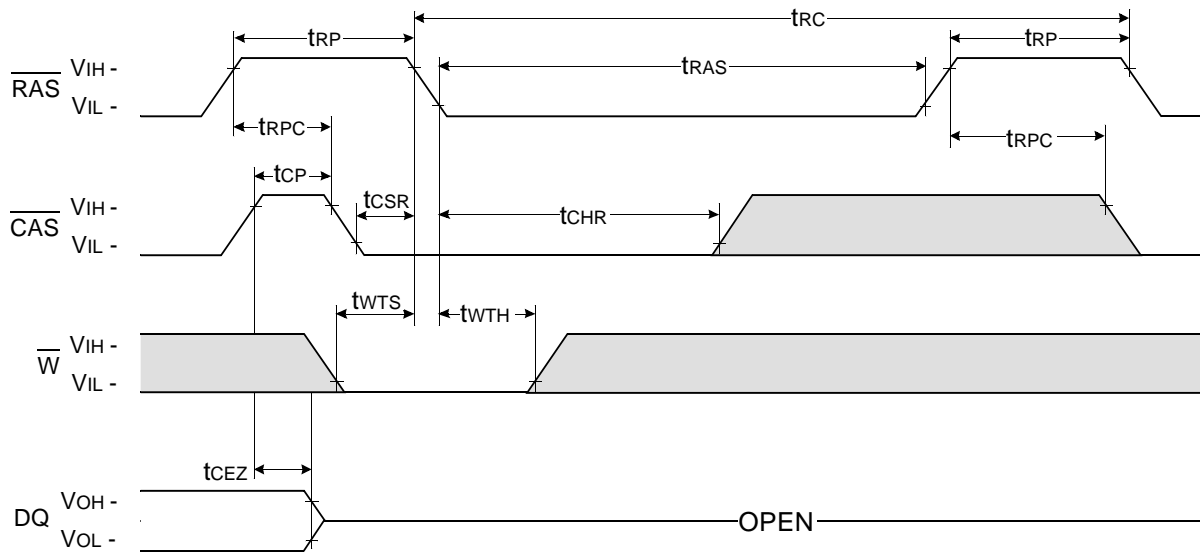
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



□ Don't care  
■ Undefined

