

256 K (262, 144-bit)  
32 K X 8 CMOS SRAM

- BYTEWYDE™ 32K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 70, 120NS MAX.
- LOW V<sub>CC</sub> DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- JEDEC STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC DIP

### DESCRIPTION

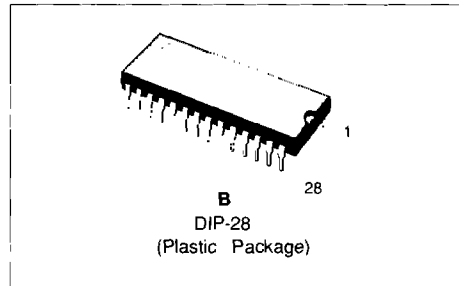
The MK4832 is a 256K (262,144-bit) CMOS SRAM, organized as 32,768 words x 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

### OPERATIONAL MODES

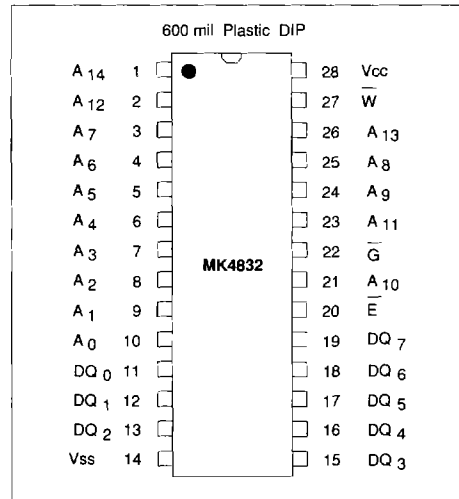
The MK4832 has a Chip Enable power down feature which sustains an automatic standby mode whenever Chip Enable (E) goes inactive high. An Output Enable (G) pin provide as high speed tri-state control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs W, G and E, as summarized in the thruth table.

### PIN NAMES

A0-A14	Address Inputs
DQ0-DQ7	Data In/Data Out
E	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write/Read Enable
V <sub>CC</sub>	+ 5V
V <sub>SS</sub>	GROUND



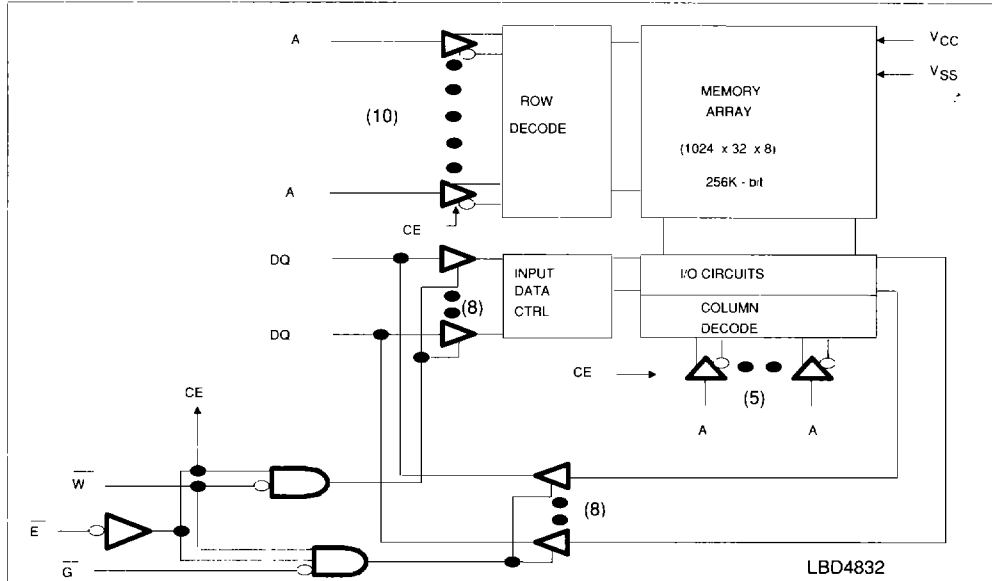
### PIN CONNECTIONS



### MK4832 THRUTH TABLE

E	W	G	MODE	DQ	POWER
H	X	X	Deselect	Hi-Z	Standby
L	H	H	Read	Hi-Z	Active
L	H	L	Read	D <sub>OUT</sub>	Active

FIGURE 1 : MK4832 BLOCK DIAGRAM



**READ MODE**

The MK4832 is in the Read mode whenever Write Enable (W) is high with Output Enable (G) low, and Chip Enable (E) is active low. This provides access to data from eight of 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight Output pins

within  $t_{AVQV}$  after the last stable address, providing G is low, and E is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ( $t_{ELQV}$ , or  $t_{GLQV}$ ) rather than the address. Data out may be indeterminate at  $t_{ELQX}$ , and  $t_{GLQX}$ , but data lines will always be valid at  $t_{AVQV}$ .

**AC ELECTRICAL CHARACTERISTICS (READ CYCLE) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ,  $V_{CC} = 5. V \pm 10\%$ )**

SYMBOL	PARAMETER	4832-70/70L		4832-120/120L		UNIT	NOTE
		MIN	MAX	MIN	MAX		
$t_{ELQX}$	Chip Enable to Q Low-Z	10		10		ns	5
$t_{AXQX}$	Output Hold from Address Change	10		10			4
$t_{GLQX}$	Output Enable Access Time	5		5			5
$t_{AVAV}$	Read Cycle Time	70		120			
$t_{AVQV}$	Address Access Time		70		120		4
$t_{ELQV}$	Chip Enable Access Time		70		120		4
$t_{GLQV}$	Output Enable Access Time		35		60		4
$t_{EHQZ}$	Chip Enable (E) to Q High-Z	0	30	0	35		5
$t_{GHOZ}$	Output Disable (G) to Q High-Z	0	30	0	35		5

FIGURE 2 : READ TIMING N°.1 ( ADDRESS ACCESS)

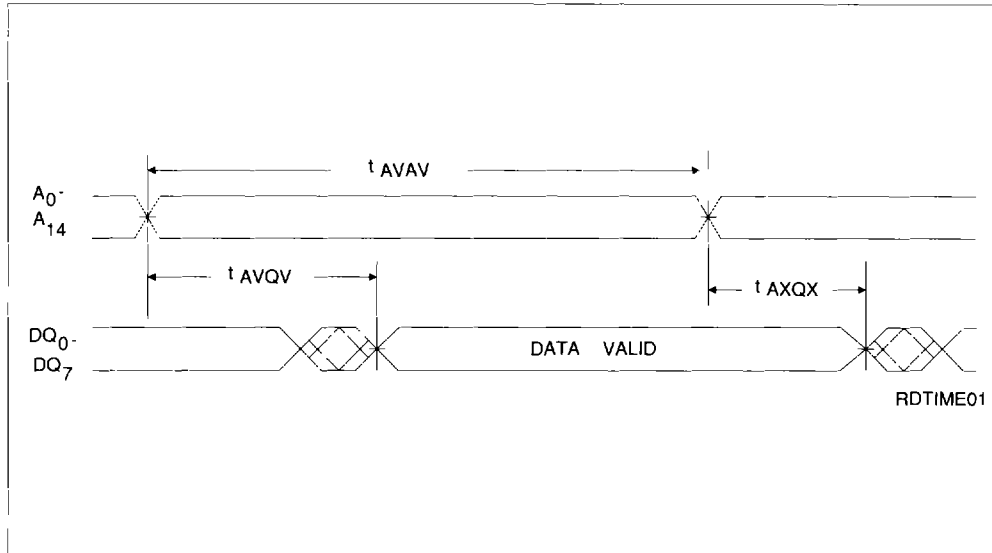
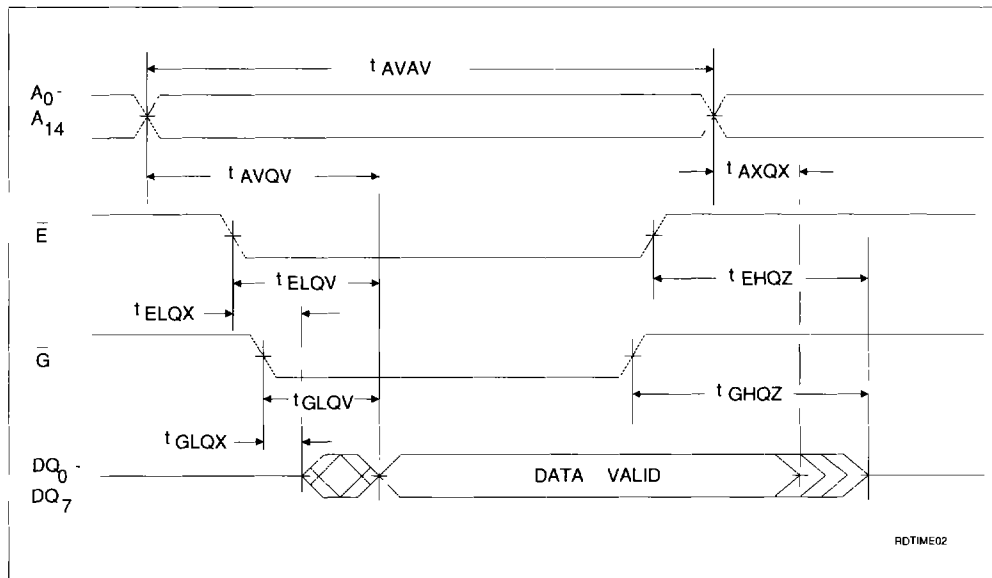


FIGURE 3 : READ TIMING N°.2



**WRITE MODE**

The MK4832 is in the Write mode whenever the  $\overline{W}$  and E pins are low. Either Chip Enable or  $\overline{W}$  must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with  $\overline{W}$  low. Therefore, address setup times are referenced to Write Enable and Chip Enable as  $t_{AVWL}$ , and  $t_{AVEL}$  respectively, and is determined to the latter occurring edge. The Write cycle can be

terminated by the earlier rising edge of  $\overline{W}$  or Chip Enable (E).

If the Output is enabled ( $\overline{E}$  = low,  $\overline{G}$  = low), then  $\overline{W}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for  $t_{DVWH}$  to the rising edge of Write Enable, or to the rising edge of E, whichever occurs first, and remain valid  $t_{WHDX}$ .

**AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)**

SYMBOL	PARAMETER	MK4832-70/70L		MM4832-120/120L		UNITS	NOTES
		MIN	MAX	MIN	MAX		
$t_{AVAV}$	Write Cycle Time	70		120		ns	
$t_{AVWL}$	Address Set-up Time to $\overline{W}$ Low	0		0			
$t_{AVEL}$	Address Set-up Time to $\overline{E}$ Low	0		0			
$t_{AVWH}$	address valid to $\overline{W}$ High	60		85			
$t_{WLWH}$	Write Pulse Width	45		65			
$t_{WHAX}$	Address Hold After End Of Write	5		5			
$t_{ELEH}$	Chip Enable Active To End Of Write	60		85			
$t_{EHAX}$	Address Hold Time From Chip Enable	5		5			
$t_{DVWH}$	Data Valid To End Of Write	25		45			
$t_{WHDX}$	Data Hold Time	0		0			
$t_{WHQX}$	$\overline{W}$ High to Q Active	5		5			5
$t_{WLQZ}$	$\overline{W}$ Low to Q High-Z	0	40	0	40		5

FIGURE 4 : WRITE CONTROL CYCLE TIMING

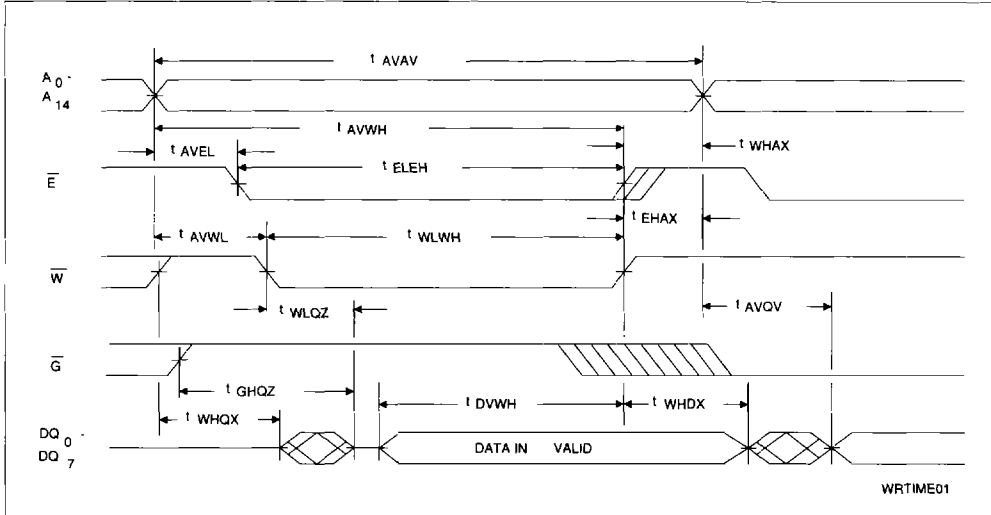
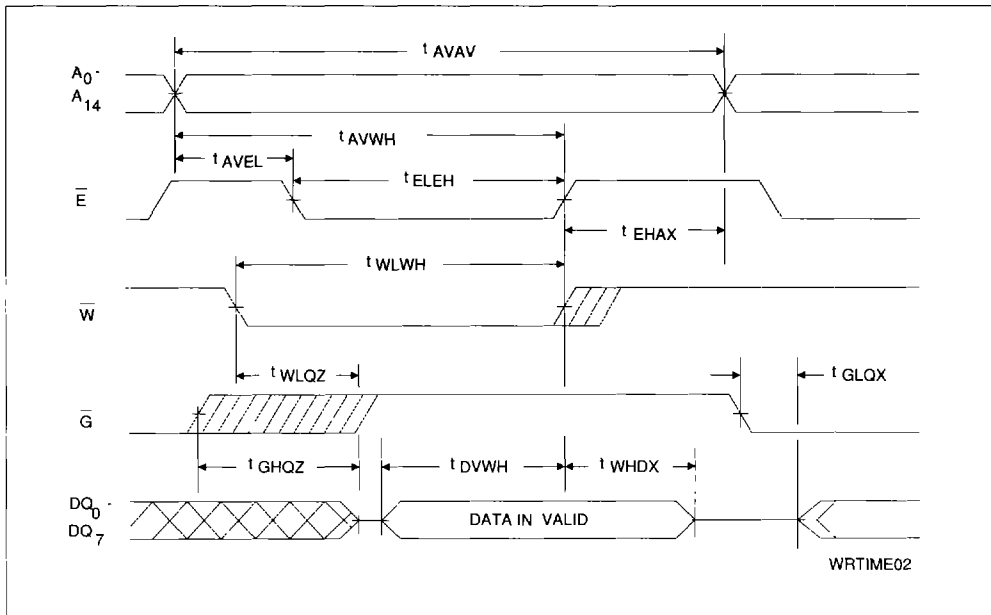


FIGURE 5 : CHIP ENABLE CONTROL WRITE CYCLE TIMING

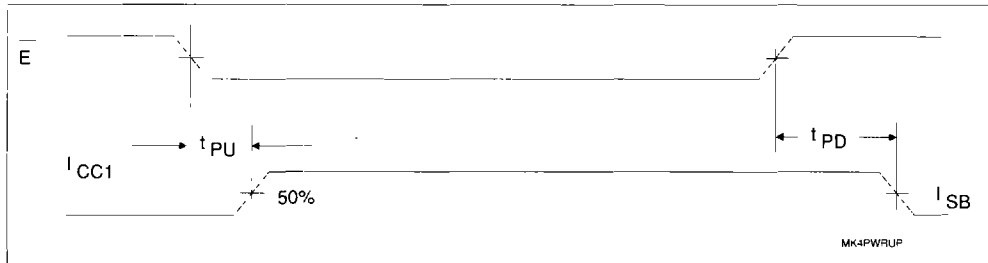


**STANDBY MODE CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ +70°C, V<sub>CC</sub> = 5.0V ± 10%)

SYMBOL	PARAMETERS	MK4832/4832L- 70		MK4832/4832L-120		UNITS
		MAX	MIN	MAX	MIN	
t <sub>PU</sub>	Chip Enable to Power-Up	0		0		ns
t <sub>PD</sub>	Chip Enable to Power-Down		70		120	ns

**FIGURE 6 : STANDBY MODE TIMING**

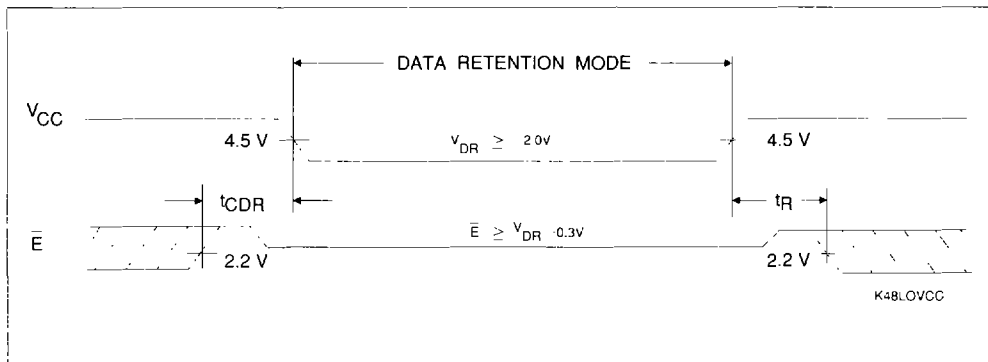


**LOW V<sub>CC</sub> DATA RETENTION CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ +70°C, V<sub>CC</sub> = 5.0 ± 10%)

SYMBOL	PARAMETERS	MAX	MAX	UNIT	NOTE
V <sub>DR</sub>	V <sub>CC</sub> Data Retentionmode	2.0		V	9
I <sub>ccDR</sub> <sup>(1)</sup>	Data Retention Pwr.supply Current Test Condition: V <sub>cc</sub> = 3.0	MK4832	500	μA	9
		MK4832L	20	μA	9
t <sub>CDR</sub>	Chip Deselect To Data Retention Mode	0		nS	9
t <sub>R</sub>	Operation Recovery Time	t <sub>AVAV</sub> <sup>(2)</sup>		nS	9

**FIGURE 7 : LOW V<sub>CC</sub> DATA RETENTION**



**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	VALUE	UNIT
V <sub>I</sub>	Voltage On Any Pin Relative to Ground	-0.5 to +7.0	V
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1	Watt
I <sub>O</sub>	Output Current <sup>(1)</sup>	50	mA

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effect reliability.  
 (1) Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second

**RECOMMENDED DC OPERATING CONDITIONS**(0°C ≤ T<sub>A</sub> ≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.5	V	1
V <sub>SS</sub>	Supply Voltage	0	0	0	V	1
V <sub>IH</sub>	Logic "1" Voltage All Inputs	2.2		V <sub>CC</sub> + 0.3v	V	1
V <sub>IL</sub>	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

**DC ELECTRICAL CHARACTERISTICS**(0°C ≤ T<sub>A</sub> ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I <sub>CC1</sub>	Average V <sub>CC</sub> Power Supply Current		70	mA	6
I <sub>SB</sub>	TTL Standby Current ( $\bar{E} = V_{IH}$ )		3	mA	7
I <sub>SB1</sub>	CMOS Standby Current ( $\bar{E} = V_{CC} - 0.2v$ )	MK4832	1	mA	8
		MK4832L	50	μA	8
I <sub>LI</sub>	Input Leakage Current (Any Input)	-1	+1	μA	2
I <sub>LO</sub>	Output Leakage Current	-2	+2	μA	2
V <sub>OH</sub>	Output Logic "1" Voltage ( I <sub>OUT</sub> = -4.0 mA )	2.4		V	1
V <sub>OL</sub>	Output Logic "0" Voltage ( I <sub>OUT</sub> = +8.0 mA )		0.4	V	1

## NOTES :

- All voltages referenced to GND
- Negative spikes of -1.0 volts allowed for up to 10 nS once per Cycle.
- I<sub>CC1</sub> measured with outputs open.
- 1 mA typical
- Measured with V<sub>CC</sub> ≥ V<sub>I</sub> ≥ GND and outputs deselected.

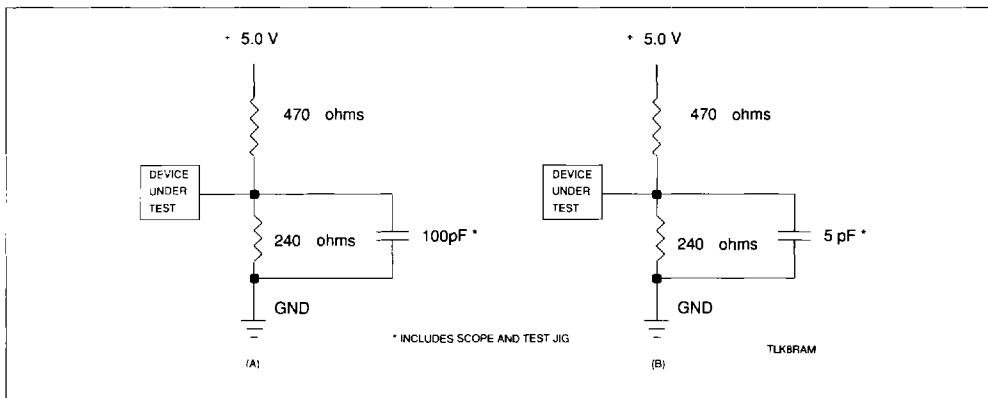
**AC TEST CONDITIONS**

Inputs Levels. . . . .0.0v to 3.0v

Transition Time . . . . .5ns

Input And Output TimingReference Levels . . . . .1.5v

**FIGURE 8 : OUPUT LOAD DIAGRAM**





**CAPACITANCE**(T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETERS	MAX	UNITS	NOTES
CI	capacitance on all pins (except dQ)	8.0	pF	10
CDQ	capacitance on DQ pins	10.0	pF	3,10

**ORDERING INFORMATION**

PART NUMBER	ACCESS TIME	PACKGE TYPE	TEMPERATURE RANGE
MK4832N-70	70ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK4832N-120	120ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK4832LN-70	70ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK4832LN-120	120ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C

<b>MK</b> _____	SGS-THOMSON PREFIX
<b>4832</b> _____	DEVICE IDENTIFICATION NUMBER
<b>L</b> _____	LOW POWER
<b>N</b> _____	PLASTIC PACKAGE
<b>70/120</b> _____	SPEED GRADE

FIGURE 9 : PACKAGE MECHANICAL DATA

