Elektronische Bauelemente

SSU04N65

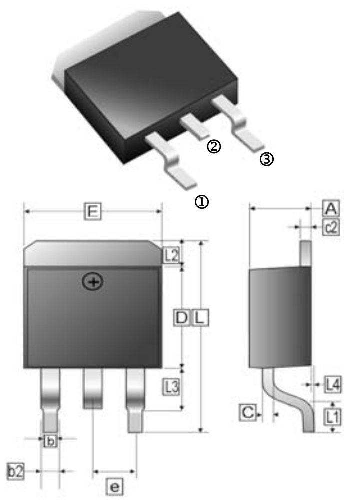
4A , 650V , $R_{DS(ON)}$ 2.6Ω
N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSU04N65 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

TO-263

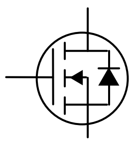


FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING

4N65
□□□□ ← Date Code



REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	4.00	4.85	c2	1.10	1.45
b	0.68	1.00	b2	1.34 REF	
L4	0.00	0.30	D	8.0	9.15
C	0.36	0.53	e	2.54 REF	
L3	1.50 REF		L	14.6	15.85
L1	2.29	2.79	L2	1.27 REF	
E	9.60	10.45			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25°C	I_D	4	A
	T_C=100°C		2.6	A
Pulsed Drain Current [2]		I_{DM}	8	A
Total Power Dissipation [4]	T_C=25°C	P_D	112	W
	T_A=25°C		2	
Single Pulse Avalanche Energy [3]		E_{AS}	2.36	mJ
Single Pulse Avalanche Current		I_{AS}	2	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient (PCB mount)[1]		$R_{θJA}$	62	°C / W
Maximum Thermal Resistance Junction-Case [1]		$R_{θJC}$	1.12	°C / W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	650	-	-	V	V_{GS}=0, I_D= 250μA
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance	g_{fs}	-	3	-	S	V_{DS}=15V, I_D=2A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±30V
Drain-Source Leakage Current	I_{DSS}	-	-	2	μA	V_{DS}=520V, V_{GS}=0
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	2.1	2.6	Ω	V_{GS}=10V, I_D=2A
Gate Resistance	R_G	-	3.4	6.8	Ω	V_{DS}=V_{GS}=0, f=1MHz
Total Gate Charge(10V)	Q_g	-	18	-	nC	I_D=1A V_{DS}=520V V_{GS}=10V
Gate-Source Charge	Q_{gs}	-	4.9	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	6.1	-		
Turn-on Delay Time	$T_{d(on)}$	-	11.2	-	nS	V_{DD}=300V I_D=1A V_{GS}=10V R_G=10 Ω
Rise Time	T_r	-	18.8	-		
Turn-off Delay Time	$T_{d(off)}$	-	29.2	-		
Fall Time	T_f	-	29.2	-		
Input Capacitance	C_{iss}	-	775	-	pF	V_{GS} =0 V_{DS}=25V f =1.0MHz
Output Capacitance	C_{oss}	-	56	-		
Reverse Transfer Capacitance	C_{rss}	-	3.8	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy [5]	EAS	0.6	-	-	mJ	V_{DD}=100V,L=1mH , I_{AS}=1A
Source-Drain Diode						
Diode Forward Voltage [2]	V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0
Reverse Recovery Time	T_{rr}	-	195	-	ns	I_F=1A,T_J=25°C, dI/dt=100A/μS
Reverse Recovery Charge	Q_{rr}	-	580	-	nC	
Continuous Source Current [1,6]	I_S	-	-	4	A	V_D=V_G=0, Force Current
Pulsed Source Current [2,6]	I_{SM}	-	-	8	A	

Notes:

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2_{OZ} copper.
2. The data tested by pulsed , pulse width ≦ 300μs , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=100V,V_{GS}=10V,L=1mH,I_{AS}=2A
4. The power dissipation is limited by 150°C, junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

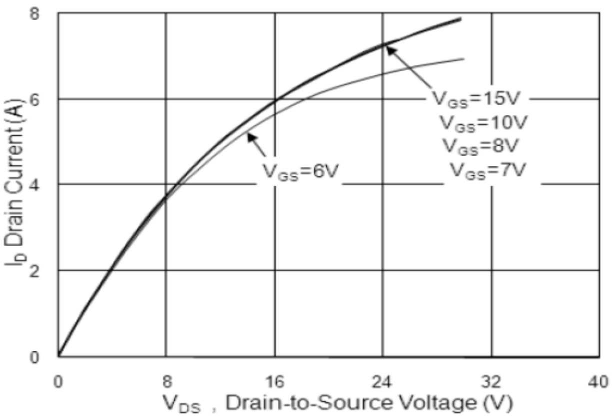


Fig.1 Typical Output Characteristics

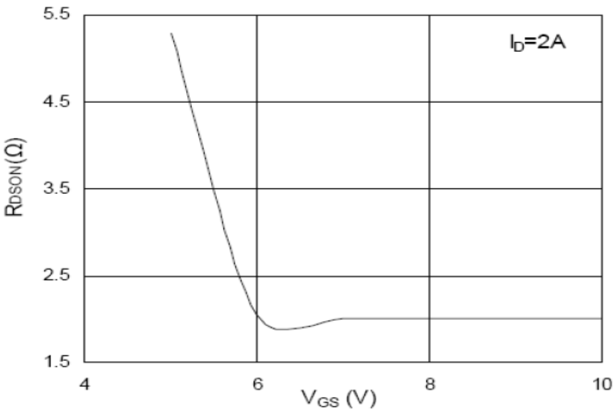


Fig.2 On-Resistance vs. G-S Voltage

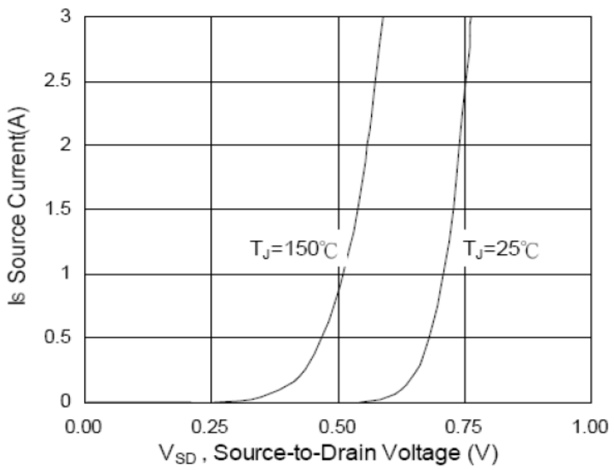


Fig.3 Forward Characteristics of Reverse

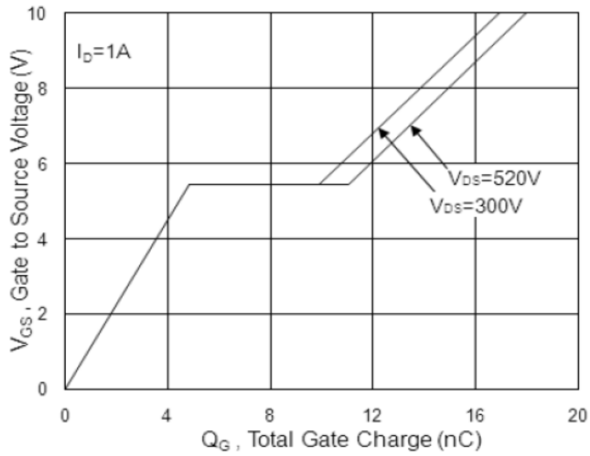


Fig.4 Gate-Charge Characteristics

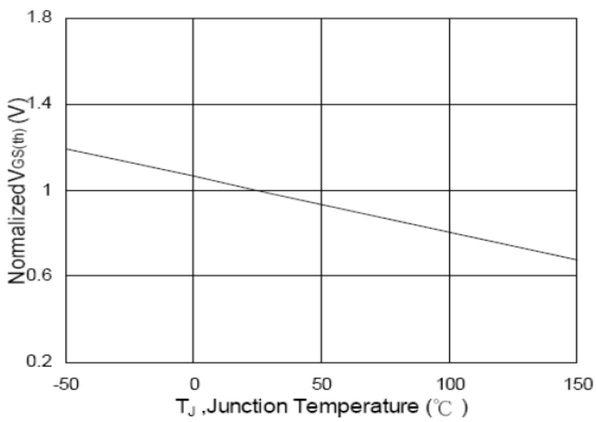


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

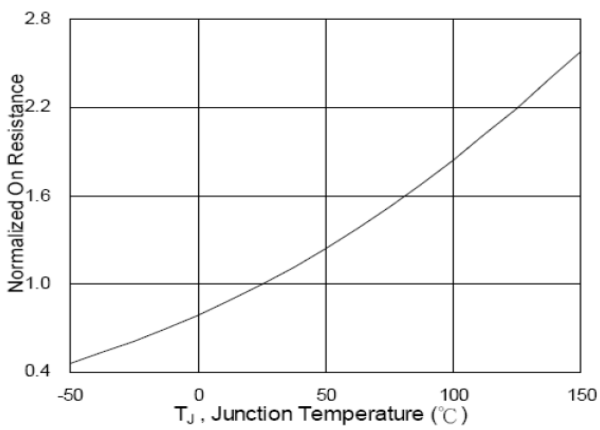


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

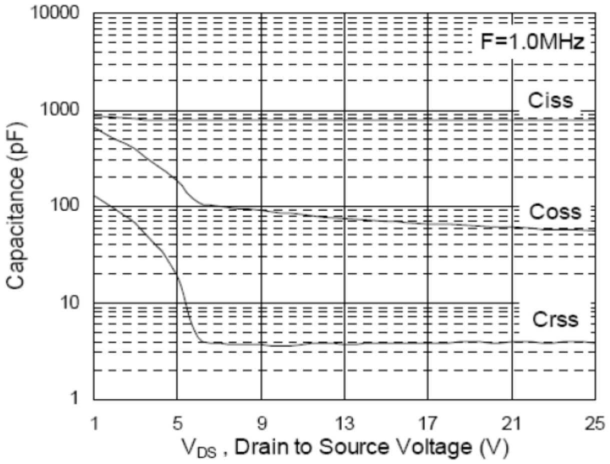


Fig.7 Capacitance

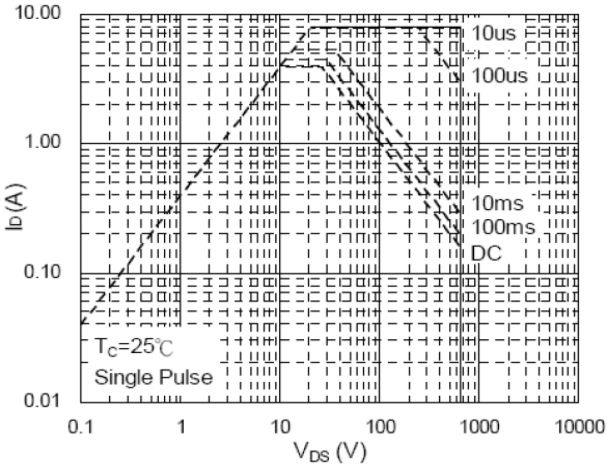


Fig.8 Safe Operating Area

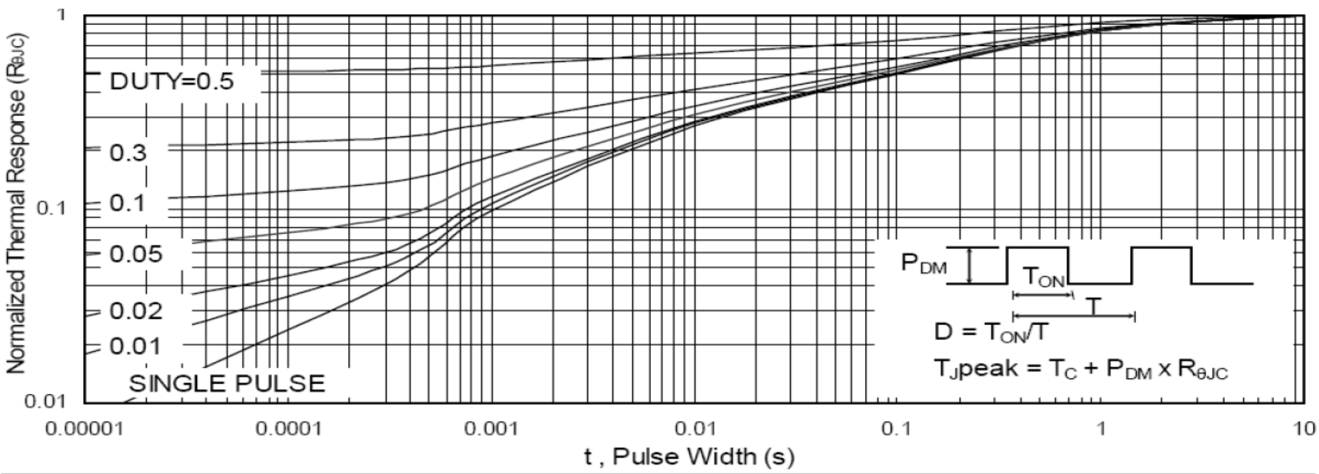


Fig.9 Normalized Maximum Transient Thermal Impedance

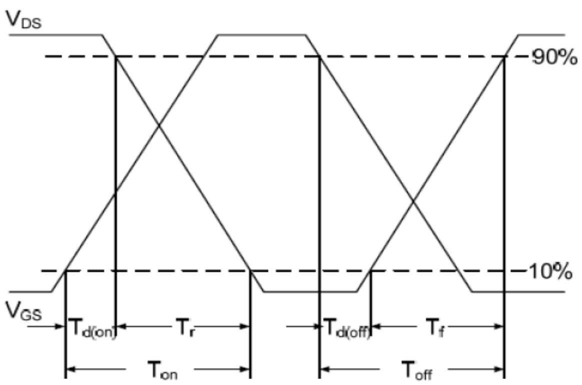


Fig.10 Switching Time Waveform

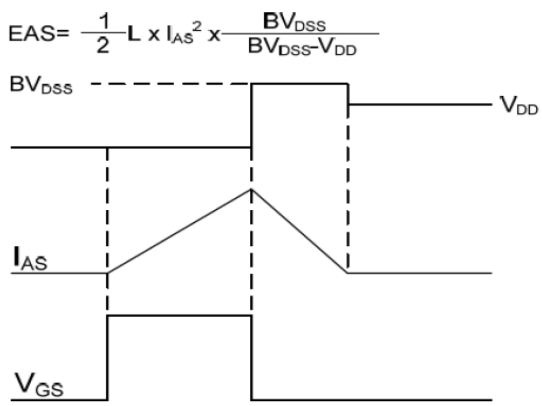


Fig.11 Unclamped Inductive Switching Waveform