

# **FDC8602** Dual N-Channel PowerTrench<sup>®</sup> MOSFET 100 V, 1.2 A, 350 m $\Omega$

## Features

- Max  $r_{DS(on)}$  = 350 m $\Omega$  at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 1.2 A
- Max  $r_{DS(on)}$  = 575 m $\Omega$  at V<sub>GS</sub> = 6 V, I<sub>D</sub> = 0.9 A
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

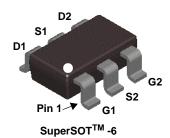


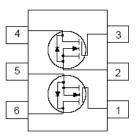
# **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

# Applications

- Load Switch
- Synchronous Rectifier





### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage		100	V	
V <sub>GS</sub>	Gate to Source Voltage		±20	V	
	Drain Current -Continuous	(Note 1a)	1.2	А	
ID	-Pulsed		5	А	
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	1.5	mJ	
P	Power Dissipation	(Note 1a)	0.96	w	
PD	Power Dissipation	(Note 1b)	0.69	vv	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C	

### **Thermal Characteristics**

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	60	°C/W
$R_{\thetaJA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 130	C/vv

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.862	FDC8602	SSOT-6	7 "	8 mm	3000 units

July 2011

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, V_{GS} = 0 \ V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C		73		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 80 V, V_{GS} = 0 V$			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V			±100	nA
On Chara	acteristics					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \ \mu A$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C		-8		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.2 A		285	350	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 6 V, I_D = 0.9 A$		409	575	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.2 A, T <sub>J</sub> = 125 °C		489	600	
		· gg · · · ·,· b · · = · ·, · j · · = · ·				
9fs	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 1.2 \text{ A}$		1.3		S
Dynamic	Characteristics			I	70	
Dynamic <sub>Ciss</sub>	Characteristics Input Capacitance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ 		53	70	pF
Dynamic C <sub>iss</sub> C <sub>oss</sub>	Characteristics Input Capacitance Output Capacitance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.2 A		I	70 25 5	
Dynamic C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Characteristics Input Capacitance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ 		53 17	25	pF pF
Dynamic C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub> R <sub>g</sub>	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance Gate Resistance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ 		53 17 0.8	25	pF pF pF
Dynamic C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub> R <sub>g</sub> Switching	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ 		53 17 0.8	25	pF pF pF
Dynamic $C_{iss}$ $C_{oss}$ $C_{rss}$ $R_g$ Switching $t_{d(on)}$	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance Gate Resistance g Characteristics	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ $V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ f = 1  MHz		53 17 0.8 1.6	25 5	pF pF pF Ω
Dynamic $C_{iss}$ $C_{oss}$ $C_{rss}$ $R_g$ Switching $t_{d(on)}$ $t_r$	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance Gate Resistance Characteristics Turn-On Delay Time	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ 		53 17 0.8 1.6 3.5	25 5 10	pF pF pF Ω ns
Dynamic $C_{iss}$ $C_{oss}$ $C_{rss}$ $R_g$ Switching $t_{d(on)}$	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance Gate Resistance Characteristics Turn-On Delay Time Rise Time	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ $V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ f = 1  MHz $V_{DD} = 50 \text{ V}, \text{ I}_{D} = 1.2 \text{ A},$		53 17 0.8 1.6 3.5 1.7	25 5 10 10	pF pF pF Ω ns
Dynamic $C_{iss}$ $C_{oss}$ $C_{rss}$ $R_g$ Switching $t_{d(on)}$ $t_r$ $t_{d(off)}$	Characteristics         Input Capacitance         Output Capacitance         Reverse Transfer Capacitance         Gate Resistance         g Characteristics         Turn-On Delay Time         Rise Time         Turn-Off Delay Time	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ $V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ f = 1  MHz $V_{DD} = 50 \text{ V}, \text{ I}_{D} = 1.2 \text{ A},$		53 17 0.8 1.6 3.5 1.7 5.4	25 5 10 10 11	pF pF pF Ω ns ns
$\begin{array}{c} \textbf{Dynamic} \\ \hline \textbf{C}_{iss} \\ \hline \textbf{C}_{rss} \\ \hline \textbf{C}_{rss} \\ \hline \textbf{R}_{g} \\ \hline \textbf{Switching} \\ \hline \textbf{switching} \\ \hline \textbf{t}_{d(on)} \\ \hline \textbf{t}_{r} \\ \hline \textbf{t}_{d(off)} \\ \hline \textbf{t}_{f} \\ \hline \textbf{Q}_{g(TOT)} \\ \hline \end{array}$	Characteristics Input Capacitance Output Capacitance Reverse Transfer Capacitance Gate Resistance  Characteristics Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ $V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$ $V_{DD} = 50 \text{ V}, \text{ I}_{D} = 1.2 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$		53 17 0.8 1.6 3.5 1.7 5.4 2.3	25 5 10 10 11 10	pF pF pF Ω ns ns ns ns
$\begin{array}{c} \textbf{Dynamic} \\ \hline C_{iss} \\ \hline C_{oss} \\ \hline C_{rss} \\ \hline R_g \\ \textbf{Switching} \\ \hline \textbf{Switching} \\ \hline t_{d(on)} \\ t_r \\ \hline t_{d(off)} \\ \hline t_f \\ \hline t_f \\ \end{array}$	Characteristics         Input Capacitance         Output Capacitance         Reverse Transfer Capacitance         Gate Resistance         g Characteristics         Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.2 \text{ A}$ $V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$ $V_{DD} = 50 \text{ V}, \text{ I}_{D} = 1.2 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		53 17 0.8 1.6 3.5 1.7 5.4 2.3 1.2	25 5 10 10 11 10 2	pF pF pF Ω ns ns ns ns ns

Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

V <sub>SD</sub>	Source-Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 1.2 A$ (Note 2)	0.86	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	- I <sub>E</sub> = 1.2 A, di/dt = 100 A/μs	27	43	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$I_F = 1.2 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	12	21	nC

NOTES:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 130 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



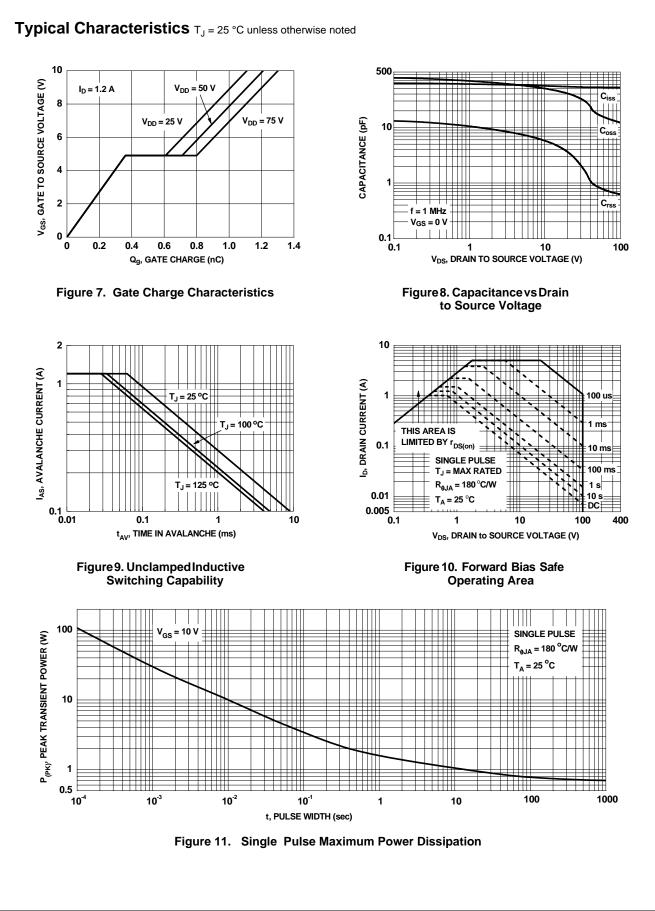
b) 180 °C/W when mounted on a minimum padof 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0%. 3. Starting T<sub>J</sub> = 25 °C; N-ch: L = 3 mH, I<sub>AS</sub> = 1 A, V<sub>DD</sub> = 100 V, V<sub>GS</sub> = 10 V.

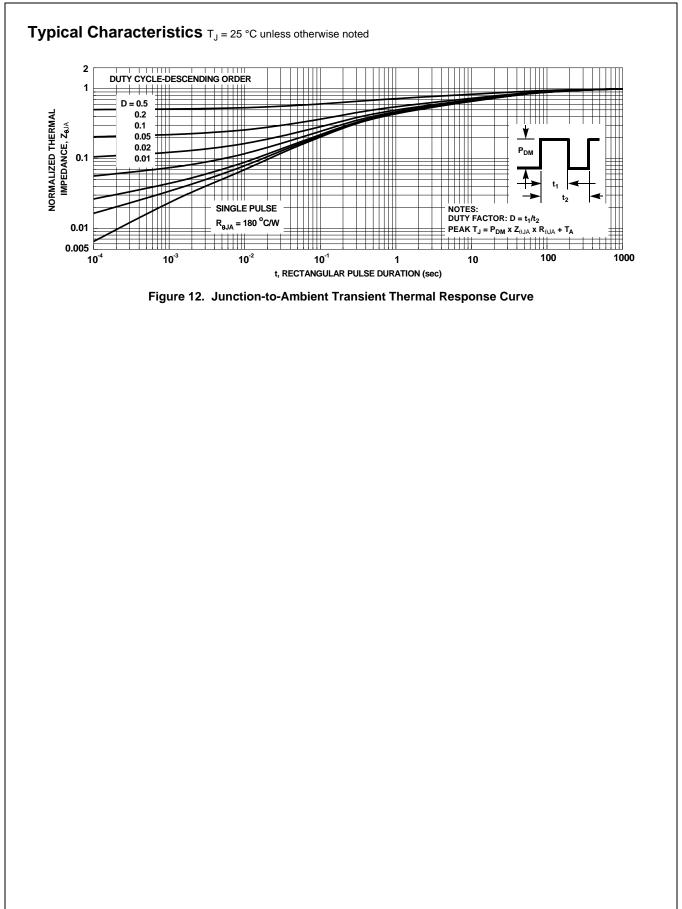
### 5 $V_{GS} = 8 V$ V<sub>GS</sub> = 10 V NORMALIZED DRAIN TO SOURCE ON-RESISTANCE V<sub>GS</sub> = 5 V V<sub>GS</sub> = 7 V V<sub>GS</sub> = 6 V 4 ID, DRAIN CURRENT (A) 3 3 $V_{GS} = 7 V$ 2 V<sub>GS</sub> = 6 V V<sub>GS</sub> = 8 V 2 PULSE DURATION = 80 µs DUTY CYCLE = 0.5% MAX 1 1 V<sub>GS</sub> = 10 V PULSE DURATION = 80 µs V<sub>GS</sub> = 5 V DUTY CYCLE = 0.5% MAX 0 0 0 1 2 3 4 5 0 2 5 1 3 4 V<sub>DS</sub>, DRAIN TO SOURCE VOLTAGE (V) ID, DRAIN CURRENT (A) Figure 1. On Region Characteristics Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage 2.0 1200 DRAIN TO SOURCE ON-RESISTANCE PULSE DURATION = 80 µs I<sub>D</sub> = 1.2 A I<sub>D</sub> = 1.2 A 1.8 r<sub>DS(on)</sub>, DRAIN TO SOURCE ON-RESISTANCE (mg) V<sub>GS</sub> = 10 V DUTY CYCLE = 0.5% MAX 900 1.6 NORMALIZED 1.4 T<sub>.1</sub> = 125 °C 600 1.2 1.0 300 T<sub>J</sub> = 25 °C 0.8 0 ⊾ 5 0.6 -75 -50 75 100 125 150 6 7 8 9 10 -25 0 25 50 TJ, JUNCTION TEMPERATURE (°C) VGS, GATE TO SOURCE VOLTAGE (V) Figure 3. Normalized On Resistance Figure 4. On-Resistance vs Gate to vs Junction Temperature Source Voltage 5 10 PULSE DURATION = 80 µs $V_{GS} = 0 V$ Is, REVERSE DRAIN CURRENT (A) DUTY CYCLE = 0.5% MAX 4 T<sub>J</sub> = 150 °C $V_{DS} = 5 V$ ID, DRAIN CURRENT (A) 1 3 T<sub>J</sub> = 25 °C 0.1 2 T<sub>.1</sub> = 150 °C T<sub>1</sub> = 25 °C 0.01 1 T<sub>J</sub> = -55 °C T<sub>J</sub> = -55 °C 0.001 0 2 3 5 6 7 8 0.2 0.4 0.8 1.0 1.2 4 0.6 V<sub>GS</sub>, GATE TO SOURCE VOLTAGE (V) V<sub>SD</sub>, BODY DIODE FORWARD VOLTAGE (V) **Figure 5. Transfer Characteristics** Figure 6. Source to Drain Diode Forward Voltage vs Source Current

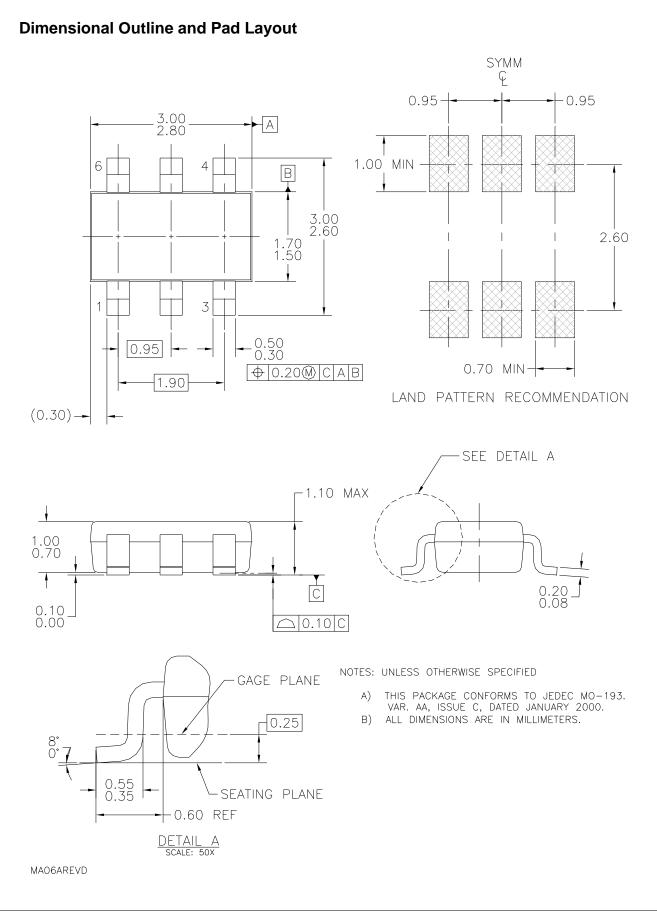
# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

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FDC8602 Dual N-Channel PowerTrench<sup>®</sup> MOSFET







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