DESCRIPTION

The Hynix HYM71V16655AT8 Series are 16Mx64bits Synchronous DRAM Modules. The modules are composed of eight 16Mx8bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, one 2Kbit EEPROM in 8pin TSSOP package on a 168pin glass-epoxy printed circuit board. One 0.22uF and one 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The Hynix HYM71V16655AT8 Series are Dual In-line Memory Modules suitable for easy interchange and addition of 128Mbytes memory. The Hynix HYM71V16655AT8 Series are fully synchronous operation referenced to the positive edge of the clock . All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high band-width.

FEATURES

- PC100MHz support
- 168pin SDRAM Unbuffered DIMM
- Serial Presence Detect with EEPROM
- 1.25” (31.75mm) Height PCB with single sided com-ponents
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4 or 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Internal Bank	Ref.	Power	SDRAM Package	Plating
HYM71V16655AT8-8	125MHz	4 Banks	4K	Normal	TSOP-II	Gold
HYM71V16655AT8-P	100MHz					
HYM71V16655AT8-S	100MHz					
HYM71V16655ALT8-8	125MHz			Low Power		
HYM71V16655ALT8-P	100MHz					
HYM71V16655ALT8-S	100MHz					

PIN DESCRIPTION

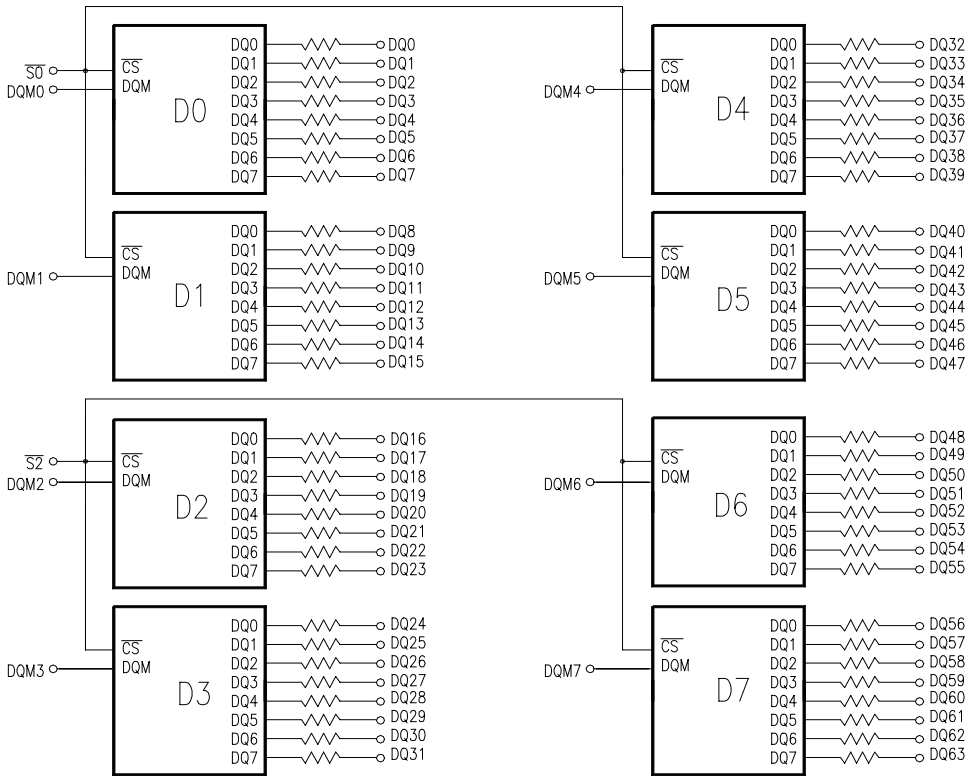
PIN	PIN NAME	DESCRIPTION
CK0~CK3	Clock Inputs	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
/S0, /S2	Chip Select	Enables or disables all inputs except CK, CKE and DQM
BA0, BA1	SDRAM Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA9 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
DQM0~DQM7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ63	Data Input/Output	Multiplexed data input / output pin
VCC	Power Supply (3.3V)	Power supply for internal circuits and input buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
SA0~2	SPD Address Input	Serial Presence Detect Address Input
WP	Write Protect for SPD	Write Protect for Serial Presence Detect on DIMM
NC	No Connection	No connection

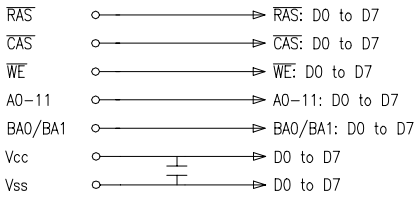
PIN ASSIGNMENTS

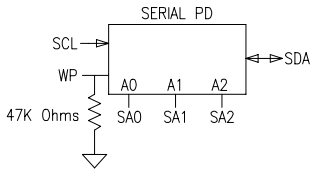
FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	85	VSS	41	VCC	125	*CK1
2	DQ0	86	DQ32	42	CK0	126	NC
3	DQ1	87	DQ33	43	VSS	127	VSS
4	DQ2	88	DQ34	44	NC	128	CKE0
5	DQ3	89	DQ35	45	/S2	129	NC
6	VCC	90	VCC	46	DQM2	130	DQM6
7	DQ4	91	DQ36	47	DQM3	131	DQM7
8	DQ5	92	DQ37	48	NC	132	NC
9	DQ6	93	DQ38	49	VCC	133	VCC
10	DQ7	94	DQ39	50	NC	134	NC
Architecture Key				51	NC	135	NC
				52	NC	136	NC
11	DQ8	95	DQ40	53	NC	137	NC
12	VSS	96	VSS	54	VSS	138	VSS
13	DQ9	97	DQ41	55	DQ16	139	DQ48
14	DQ10	98	DQ42	56	DQ17	140	DQ49
15	DQ11	99	DQ43	57	DQ18	141	DQ50
16	DQ12	100	DQ44	58	DQ19	142	DQ51
17	DQ13	101	DQ45	59	VCC	143	VCC
18	VCC	102	VCC	60	DQ20	144	DQ52
19	DQ14	103	DQ46	61	NC	145	NC
20	DQ15	104	DQ47	62	NC	146	NC
21	NC	105	NC	63	NC	147	NC
22	NC	106	NC	64	VSS	148	VSS
23	VSS	107	VSS	65	DQ21	149	DQ53
24	NC	108	NC	66	DQ22	150	DQ54
25	NC	109	NC	67	DQ23	151	DQ55
26	VCC	110	VCC	68	VSS	152	VSS
27	/WE	111	/CAS	69	DQ24	153	DQ56
28	DQM0	112	DQM4	70	DQ25	154	DQ57
29	DQM1	113	DQM5	71	DQ26	155	DQ58
30	/S0	114	NC	72	DQ27	156	DQ59
31	NC	115	/RAS	73	VCC	157	VCC
32	VSS	116	VSS	74	DQ28	158	DQ60
33	A0	117	A1	75	DQ29	159	DQ61
34	A2	118	A3	76	DQ30	160	DQ62
35	A4	119	A5	77	DQ31	161	DQ63
36	A6	120	A7	78	VSS	162	VSS
37	A8	121	A9	79	CK2	163	*CK3
38	A10/AP	122	BA0	80	NC	164	NC
39	BA1	123	A11	81	WP	165	SA0
40	VCC	124	VCC	82	SDA	166	SA1
Voltage Key				83	SCL	167	SA2
				84	VCC	168	VCC

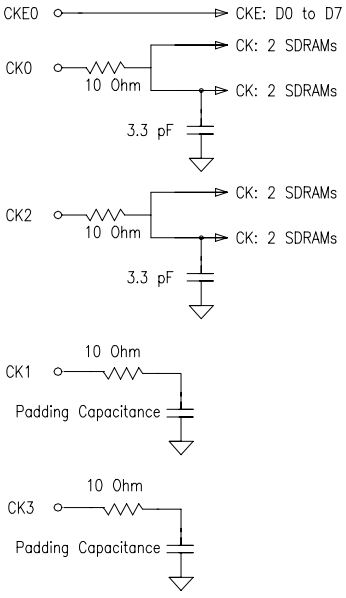
Note : * CK1 and CK3 are connected with termination R/C (Refer to the block diagram)

BLOCK DIAGRAM









Note : 1. The serial resistor values of DQs are 10ohms
2. The padding capacitance of termination R/C for CK1,CK3 is 10pF

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION			VALUE			NOTE
		-8	-P	-S	-8	-P	-S	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	12			0Ch			1
BYTE4	# of Column Addresses on This Assembly	10			0Ah			
BYTE5	# of Module Banks on This Assembly	1 Bank			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @/CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @/CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	15.625us / Self Refresh Supported			80h			
BYTE13	Primary SDRAM Width	x8			08h			
BYTE14	Error Checking SDRAM Width	None			00h			
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK			01h			
BYTE16	Burst Lenth Supported	1,2,4,8,Full Page			8Fh			2
BYTE17	# of Banks on Each SDRAM Device	4 Banks			04h			
BYTE18	SDRAM Device Attributes, /CAS Lataency	/CAS Latency=2,3			06h			
BYTE19	SDRAM Device Attributes, /CS Lataency	/CS Latency=0			01h			
BYTE20	SDRAM Device Attributes, /WE Lataency	/WE Latency=0			01h			
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered			00h			
BYTE22	SDRAM Device Attributes, General	+/- 10% voltage tolerence, Burst Read Single Bit Write, Precharge All, Auto Precharge, Early RAS Precharge			0Eh			
BYTE23	SDRAM Cycle Time @/CAS Latency=2	8ns	10ns	12ns	A0h	A0h	C0h	
BYTE24	Access Time from Clock @/CAS Latency=2	6ns	6ns	6ns	60h	60h	60h	
BYTE25	SDRAM Cycle Time @/CAS Latency=1	-	-	-	00h	00h	00h	
BYTE26	Access Time from Clock @/CAS Latency=1	-	-	-	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (tRP)	20ns	20ns	20ns	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	20ns	20ns	20ns	14h	14h	14h	
BYTE30	Minimum /RAS Pulse Width (tRAS)	48ns	50ns	50ns	30h	32h	32h	
BYTE31	Module Bank Density	128MB			20h			
BYTE32	Command and Address Signal Input Setup Time	2ns	2ns	2ns	20h	20h	20h	
BYTE33	Command and Address Signal Input Hold Time	1ns	1ns	1ns	10h	10h	10h	
BYTE34	Data Signal Input Setup Time	2ns	2ns	2ns	20h	20h	20h	
BYTE35	Data Signal Input Hold Time	1ns	1ns	1ns	10h	10h	10h	
BYTE36 ~61	Superset Information (may be used in future)	-			00h			
BYTE62	SPD Revision	Intel SPD 1.2B			12h			3, 8
BYTE63	Checksum for Byte 0~62	-			F0h	16h	36h	
BYTE64	Manufacturer JEDEC ID Code	Hynix JEDED ID			ADh			
BYTE65 ~71	....Manufacturer JEDEC ID Code	Unused			FFh			
BYTE72	Manufacturing Location	HSI (Korea Area) HSA (United States Area) HSE (Europe Area) HSJ (Japan Area) HSS(Singapore) ASIA Area			0*h 1*h 2*h 3*h 4*h 5*h			10

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION			VALUE			NOTE
		-8	-P	-S	-8	-P	-S	
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)			37h			4, 5
BYTE74	Manufacturer's Part Number (128Mb based)	1			31h			4, 5
BYTE75	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTL)			56h			4, 5
BYTE76	Manufacturer's Part Number (Memory Width)	1			31h			4, 5
BYTE77	....Manufacturer's Part Number (Memory Width)	6			36h			4, 5
BYTE78	Manufacturer's Part Number (Data Width)	6			36h			4, 5
BYTE79	....Manufacturer's Part Number (Data Width)	5			35h			4, 5
BYTE80	Manufacturer's Part Number (Refresh, SDRAM Bank)	5 (4K Refresh, 4Banks)			35h			4, 5
BYTE81	Manufacturer's Part Number (Generation)	A			41h			4, 5
BYTE82	Manufacturer's Part Number (Package Type)	T			54h			4, 5
BYTE83	Manufacturer's Part Number (Component Configuration)	8 (x8 based)			38h			4, 5
BYTE84	Manufacturer's Part Number (Hyphent)	- (Hyphen)			2Dh			4, 5
BYTE85	Manufacturer's Part Number (Min. Cycle Time)	8	P	S	38h	50h	53h	4, 5
BYTE86 ~90	Manufacturer's Part Number	Blanks			20h			4, 5
BYTE91	Revision Code (for Component)	Process Code			-			4, 6
BYTE92	....Revision Code (for PCB)	Process Code			-			4, 6
BYTE93	Manufacturing Date	Year			-			3, 6
BYTE94	....Manufacturing Date	Work Week			-			3, 6
BYTE95 ~98	Assembly Serial Number	Serial Number			-			6
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None			00h			
BYTE126	System Frequency Support	100MHz			64h			7, 8
BYTE127	Intel Specification Details for 100MHz Support	Refer to Note7			AFh	AFh	ADh	7, 8
BYTE128 ~256	Unused Storage Locations	-			00h			

Note :
1. The bank address is excluded
2. 1, 2, 4, 8 for Interleave Burst Type
3. BCD adopted
4. ASCII adopted
5. Basically Hynix writes Part No. except for 'HYM' in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90
6. Not fixed but dependent
7. CK0, CK2 connected to DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to Intel SPD Specification 1.2B
9. In the case of L-Part, character 'L' will be added between byte 81 and byte 82
10. Refer to HSI Web Site.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	8	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low voltage	VIL	-0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to VSS = 0V
2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

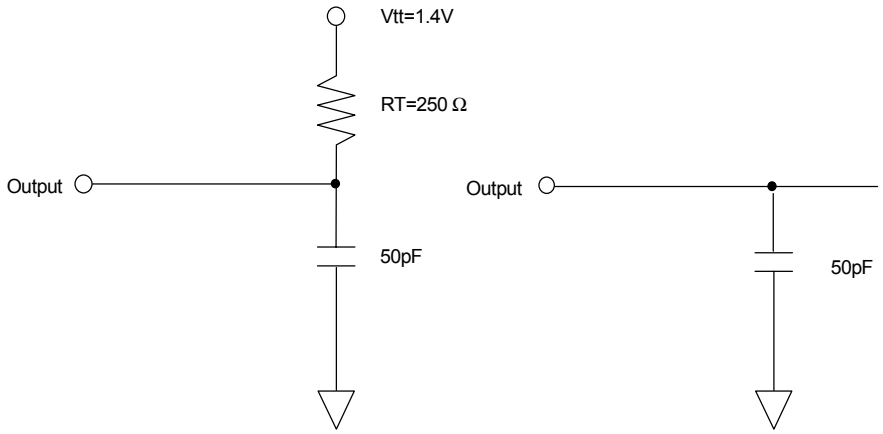
Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-8/P/S		Unit
			Min	Max	
Input Capacitance	CK0, CK2	C_{I1}	25	45	pF
	CKE0	C_{I2}	35	55	pF
	/S0, /S2	C_{I3}	25	40	pF
	A0~11, BA0, BA1	C_{I4}	40	60	pF
	/RAS, /CAS, /WE	C_{I5}	40	60	pF
	DQM0~DQM7	C_{I6}	5	20	pF
Data Input / Output Capacitance	DQ0 ~ DQ63	$C_{I/O}$	5	20	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, VDD=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-8	8	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note :
1.VIN = 0 to 3.6V, All other pins are not tested under VIN =0V
2.DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition		Speed			Unit	Note
				-8	-P	-S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		**800**	**800**	**800**	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		16			mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		16				
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V		160			mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		80				
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		56			mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		56				
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V		320			mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		320				
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	**880**	**800**	**800**	mA	1
			CL=2	**800**	**800**	**720**		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		**1600**			mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		16			mA	3
		Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		6.4			mA	4

Note :
1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3.HYM71V16655AT8-8/P/S
4.HYM71V16655ALT8-8/P/S

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK3	8	1000	10	1000	10	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		10		12		ns	
Clock High Pulse Width		tCHW	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	3	-	3	-	3	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency = 3	tAC3	-	6	-	6	-	6	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency = 3	tOHZ3	3	6	3	6	3	6	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	3	6	3	6	3	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns
If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter

2.Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	68	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	20	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	48	100K	50	100K	50	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	16	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	4	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HYM71V16655A(L)T8-8

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V16655A(L)T8-P

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V16655A(L)T8-S

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	L	X	A9 Pin High (Other Pins OP code)			MRS Mode
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation
3. The burst read sigle write mode is entered by programming the Write burst mode bit (A9) in the mode register to a logic 1.

PACKAGE DEMENSION