EPSON
EXCEED YOUR VISION

S1C17555/565/955/965

16-bit Single Chip Microcontroller

- Built-in FSA (Flexible Signal processing Accelerator) function;
  It realize high processing with low power
- 12-bit A/D converter
- Several kinds of serial interface
- 48-pin wafer-chip-scale package (WCSP)
- Built-in the flash memory that it can write with a single power supply

■ DESCRIPTIONS

S1C17555/565/955/965 can operate at high speed with low power and it has large address area.

These products have good points such as Space-saving package (WCSP), 12-bit A/D converter and Signal processing accelerator(FSA) every model and selectable depending on a use.

In FSA, signal processing ranging from image processing to audio handling is possible.

S1C17955/965 is most suitable for the application such as mobile devices. FSA realize high processing with a low clock, and realize a low consumption design by using this function.

■ FEATURES

機種	S1C17555	S1C17565	S1C17955	S1C17965
CPU				
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17			
Multiplier/Divider (COPRO)	· 16-bit × 16-bit multiplier · 16-bit × 16-bit + 32-bit multiply and accumulation unit · 16-bit ÷ 16-bit divider			
FSA *1				
Multiply and accumulation unit	-		32-bit × 32-bit multiplier + 72-bit adder	
Data access	-		2 inputs and 1 output	
Address space			12K bytes	
Embedded Flash memory				
Capacity	128K bytes (for both instructions and data)			
Erase/program count	40 times (min.) (Applied only when FLS V1.0 or later is used.)			
Other	· Read/program protection function · An embedded power supply booster for erasing/programming · Allows on-board programming using a debugging tool such as ICDmini.			
Embedded RaM				
RAM1 Capacity	4K bytes			
RAM2 (FSA RAM) Capacity	12K bytes			
Clock generator (CIG)				
System clock source	2 sources (IOSC/OSC1)	3 sources (IOSC/OSC1/OSC3)	2 sources (IOSC/OSC1)	3 sources (IOSC/OSC1/OSC3)
IOSC oscillator circuit	2/4/8/12 MHz (typ.) internal oscillator circuit			
OSC3 oscillator circuit	-	24 MHz (max.) crystal or ceramic oscillator circuit Supports an external clock input.	-	24 MHz (max.) crystal or ceramic oscillator circuit Supports an external clock input.
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit. Supports an external clock input.			
Other	· Core clock frequency control · Peripheral module clock supply control			
I/O ports (P)				
Number of general-purpose I/O ports	Max. 20 bits	Max. 24 bits	Max. 20 bits	Max. 24 bits
	Pins are shared with the peripheral I/O.			
Serial interfaces				
8-bit SPI (SPI)	2 channels			
16-bit SPI (SPI16)	1 channel			
I²C master (I2CM)	1 channel			
I²C slave (I2CS)	1 channel			
UART（UART）	1 channel (IrDA1.0 supported)	2 channels (IrDA1.0 supported)	1 channel (IrDA1.0 supported)	2 channels (IrDA1.0 supported)
IR remote controller (REMC)	–	1 channel	–	1 channel
Timers				
16-bit timer (T16)	3 channels			
Fine mode 16-bit timer (T16F)	2 channels			
16-bit PWM timer (T16A2)	4 channels			
Clock timer (CT)	1 channel			
Stopwatch timer (SWT)	1 channel			
Watchdog timer (WDT)	1 channel			

12-bit A/D converter (aDC12Sa)				
Conversion method	-	Successive approximation type	-	Successive approximation type
Analog input channel	-	6 channels (Three channels can only be used for multichannel conversion.)	-	6 channels (Three channels can only be used for multichannel conversion.)
Resolution	-	12 bits	-	12 bits
Interrupts				
Reset interrupt	#RESET pin			
NMI	Watchdog timer			
Programmable interrupts	21 systems (8 levels)	22 systems (8 levels)	21 systems (8 levels)	22 systems (8 levels)
Power supply voltage				
Core voltage (LVDD)	1.65 V to 1.95 V	1.65 V to 1.95 V (Not required when the regulator is used)	1.65 V to 1.95 V	1.65 V to 1.95 V (Not required when the regulator is used)
I/O voltage (HVDD)	1.65 V to 3.6 V	2.0 V to 3.6 V (When the regulator is used) 1.65 V to 3.6 V (When the regulator is not used)	1.65 V to 3.6 V	2.0 V to 3.6 V (When the regulator is used) 1.65 V to 3.6 V (When the regulator is not used)
Analog voltage (AVDD)	-	2.7 V to 3.6 V (Not required when the regulator is used)	-	2.7 V to 3.6 V (Not required when the regulator is used)
Flash programming voltage (VPP)	7.5 V (Not required when the regulator/booster is used.)			
Regulators				
LVDD regulator	-	Input: 2.0 V to 3.6 V Output: 1.8 V	-	Input: 2.0 V to 3.6 V Output: 1.8 V
AVDD regulator	-	Input: 3.1 V to 3.6 V, Output: 2.8 V	-	Input: 3.1 V to 3.6 V, Output: 2.8 V
VPP regulator/booster	Input: 2.4 V to 3.6 V Output: 7.5 V			
Operating temperature				
Operating temperature range	-40°C to 85°C (10 to 40°C when programing/erasing the Flash)			
Current consumption (Typ. value, IVDD = hVDD = 1.8 V, regulator not used)				
SLEEP state	1.0 µA (IOSC = Off, OSC1 = Off, OSC3 = Off)			
HALT state	2.9 µA (IOSC = Off, OSC1 = 32 kHz, OSC3 = Off)			
Run state	3500 µA (IOSC = 12 MHz, OSC1 = Off, OSC3 = Off)			
FSA operating current	-		+270 µA/MHz	
Shipping form				
1	WCSP-48 3.863 × 3.863 × 0.8 mm, ball pitch: 0.5 mm	TQFP13-64pin 10 × 10 × 1.0 mm, lead pitch: 0.5 mm	WCSP-48 3.863 × 3.863 × 0.8 mm, ball pitch: 0.5 mm	TQFP13-64pin 10 × 10 × 1.0 mm, lead pitch: 0.5 mm
2		Die form 3.863 × 3.863 mm, pad pitch: 140 µm		Die form 3.863 × 3.863 mm, pad pitch: 140 µm

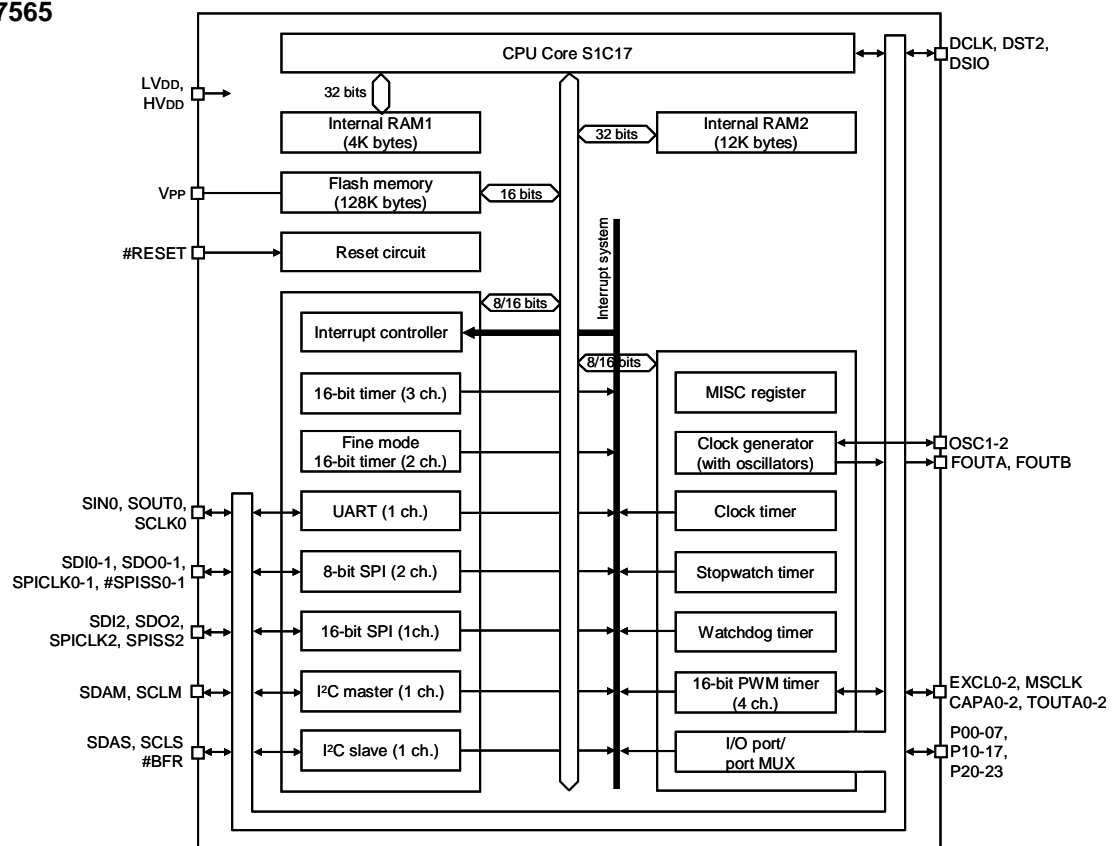*1 For more information on the FSA, please contact Seiko Epson.
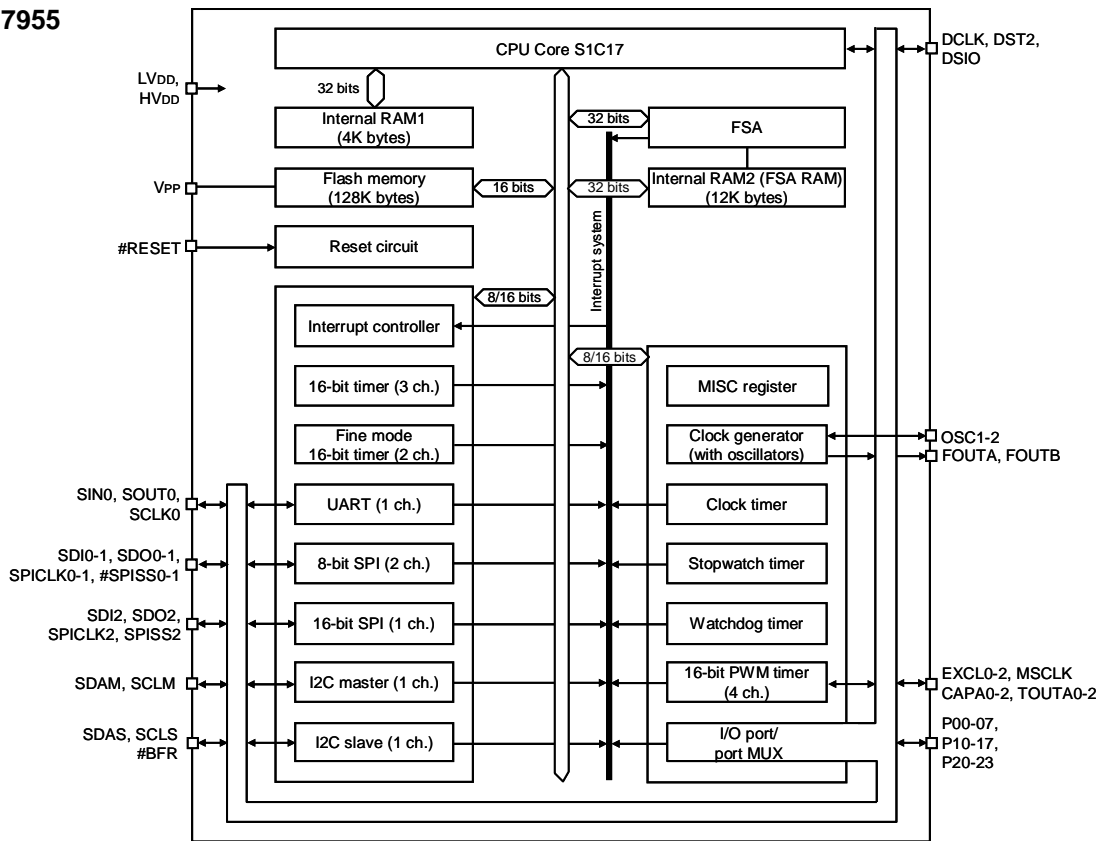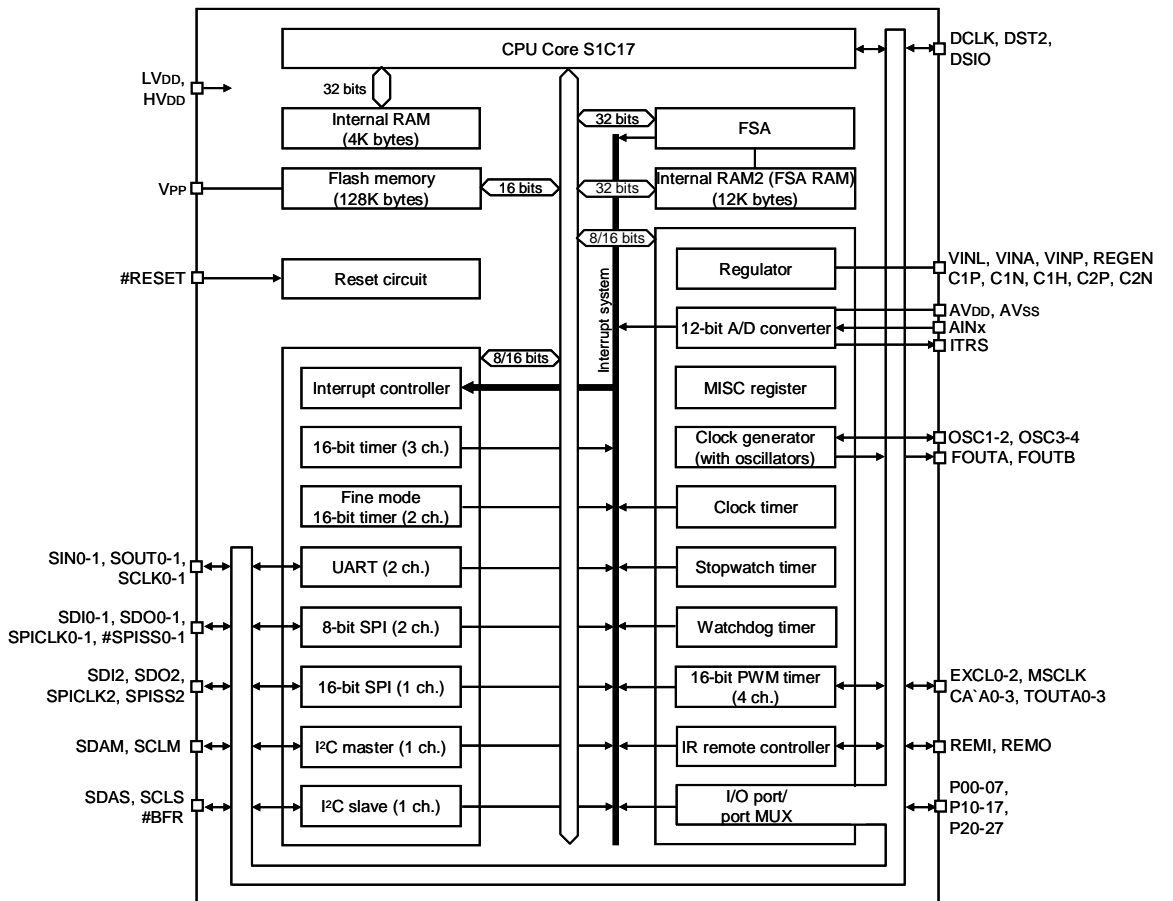
■ BLOCK DIAGRAM

S1C17555
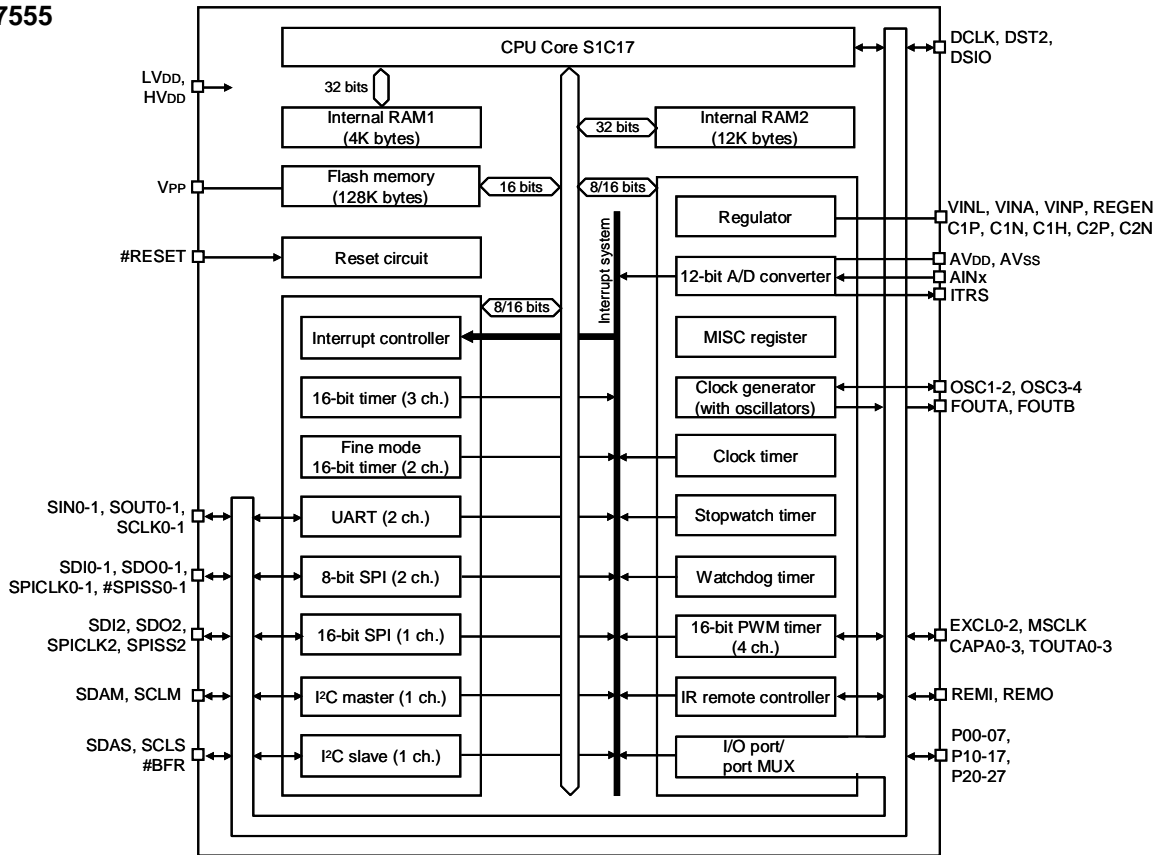
S1C17565

S1C17555/565/955/965

S1C17955

CPU Core S1C17

DCLK, DST2, DSIO

LV_DD, HV_DD

32 bits

Internal RAM1 (4K bytes)

32 bits

FSA

VPP

Flash memory (128K bytes)

16 bits

32 bits

Internal RAM2 (FSA RAM) (12K bytes)

#RESET

Reset circuit

8/16 bits

Interrupt controller

Interrupt system

8/16 bits

16-bit timer (3 ch.)

MISC register

Fine mode 16-bit timer (2 ch.)

Clock generator (with oscillators)

OSC1-2
FOUTA, FOUTB

SIN0, SOUT0, SCLK0

UART (1 ch.)

Clock timer

SDI0-1, SDO0-1, SPICLK0-1, #SPISS0-1

8-bit SPI (2 ch.)

Stopwatch timer

SDI2, SDO2, SPICLK2, SPISS2

16-bit SPI (1 ch.)

Watchdog timer

SDAM, SCLM

I2C master (1 ch.)

16-bit PWM timer (4 ch.)

EXCL0-2, MSCLK
CAPA0-2, TOUTA0-2

SDAS, SCLS #BFR

I2C slave (1 ch.)

I/O port/ port MUX

P00-07, P10-17, P20-23

S1C17965

CPU Core S1C17

DCLK, DST2, DSIO

LV_DD, HV_DD

32 bits

Internal RAM (4K bytes)

32 bits

FSA

VPP

Flash memory (128K bytes)

16 bits

32 bits

Internal RAM2 (FSA RAM) (12K bytes)

#RESET

Reset circuit

8/16 bits

Regulator

VINL, VINA, VINP, REGEN
C1P, C1N, C1H, C2P, C2N

12-bit A/D converter

AV_DD, AV_SS
AINx
ITRS

Interrupt system

Interrupt controller

8/16 bits

MISC register

16-bit timer (3 ch.)

Clock generator (with oscillators)

OSC1-2, OSC3-4
FOUTA, FOUTB

Fine mode 16-bit timer (2 ch.)

Clock timer

SIN0-1, SOUT0-1, SCLK0-1

UART (2 ch.)

Stopwatch timer

SDI0-1, SDO0-1, SPICLK0-1, #SPISS0-1

8-bit SPI (2 ch.)

Watchdog timer

SDI2, SDO2, SPICLK2, SPISS2

16-bit SPI (1 ch.)

16-bit PWM timer (4 ch.)

EXCL0-2, MSCLK
CA`A0-3, TOUTA0-3

SDAM, SCLM

I²C master (1 ch.)

IR remote controller

REMI, REMO

SDAS, SCLS #BFR

I²C slave (1 ch.)

I/O port/ port MUX

P00-07, P10-17, P20-27

NOTICE: