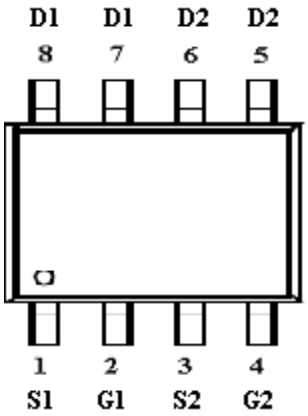
SPC4533
N & P Pair Enhancement Mode MOSFET

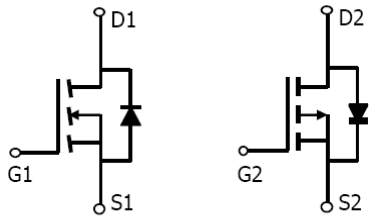
DESCRIPTION
The SPC4533 is the N- and P-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

FEATURES
- N-Channel
  30V/8.0A,$R_{DS(ON)}$= 18Ω@V_{GS}= 10V
  30V/6.0A,$R_{DS(ON)}$= 36mΩ@V_{GS}= 4.5V
- P-Channel
  -30V/-6.0A,$R_{DS(ON)}$= 36mΩ@V_{GS}=- 10V
  -30V/-4.0A,$R_{DS(ON)}$= 65mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOP – 8P package design

APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

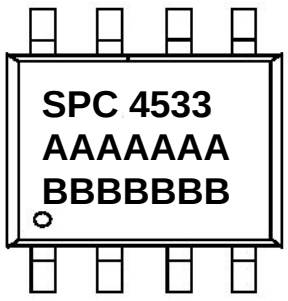
PIN CONFIGURATION(SOP – 8P)





n-channel p-channel

PART MARKING



AAAAAAA : Lot NO.
BBBBBBB : Date Code

SPC4533
N & P Pair Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPC4533S8RGB	SOP- 8P	SPC4533

※ SPC4533S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate –Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	8.4	-6.0	A
	T_A=70℃		6.7	-4.0	
Pulsed Drain Current		I_{DM}	30	-30	A
Power Dissipation	T_A=25℃	P_D	2.0		W
Operating Junction Temperature		T_J	-55/150		℃
Storage Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient	T ≤ 10sec	$R_{\theta JA}$	50	52	℃/W
	Steady State		80	80	

N-CH Electrical Characteristics@ T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=8A	-	-	18	mΩ
		V_{GS}=4.5V, I_D=6A	-	-	36	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=8A	-	13	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=24V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±30	uA
Q_g	Total Gate Charge[2]	I_D=8A	-	6.5	10.5	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	2.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	3.3	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=15V	-	8	-	ns
t_r	Rise Time	I_D=1A	-	6	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	17	-	ns
t_f	Fall Time	R_D=15Ω	-	6	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	540	860	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	150	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.5A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[2]	I_S=8A, V_{GS}=0V	-	20	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	12	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-6A	-	-	36	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	-	65	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-6A	-	9.4	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (T_J=70°C)	V_{DS}=-24V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±30	uA
Q_g	Total Gate Charge[2]	I_D=-6A	-	9	14.5	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	2.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	5.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-15V	-	8	-	ns
t_r	Rise Time	I_D=-1A	-	9.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=-10V	-	20	-	ns
t_f	Fall Time	R_D=15Ω	-	20	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	500	800	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	180	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	135	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.5A, V_{GS}=0V	-	-	-1.3	V
t_{rr}	Reverse Recovery Time[2]	I_S=-6A, V_{GS}=0V	-	25	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	17	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board , t ≤10sec ; 135℃/W when mounted on min. copper pad.

N-Channel

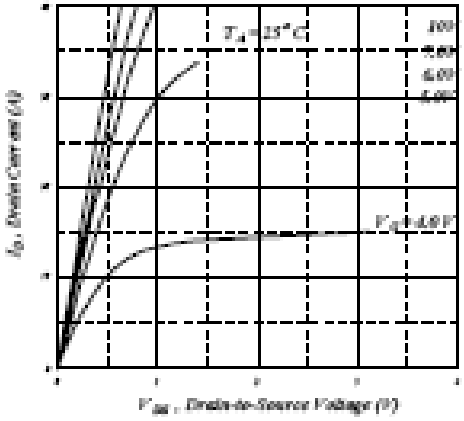


Fig 1. Typical Output Characteristics

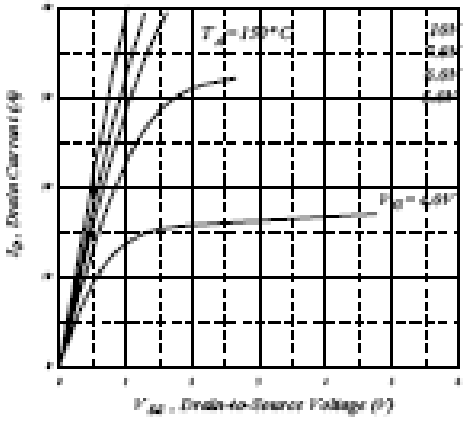


Fig 2. Typical Output Characteristics

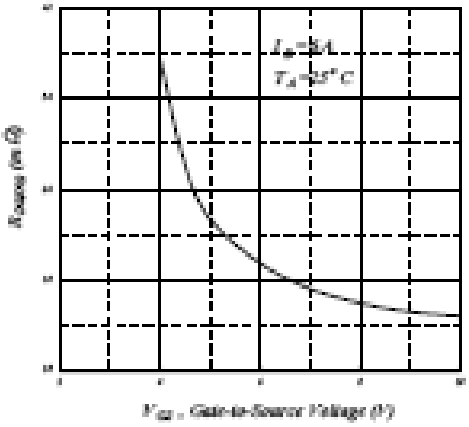


Fig 3. On-Resistance v.s. Gate Voltage

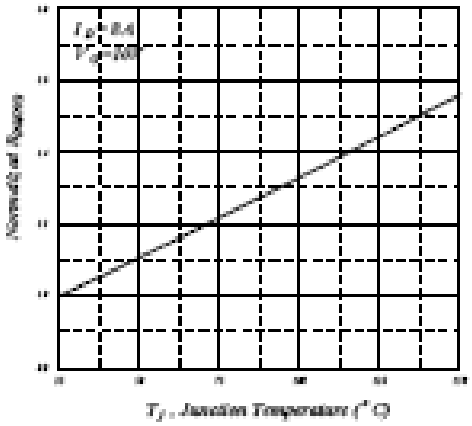


Fig 4. Normalized On-Resistance v.s. Junction Temperature

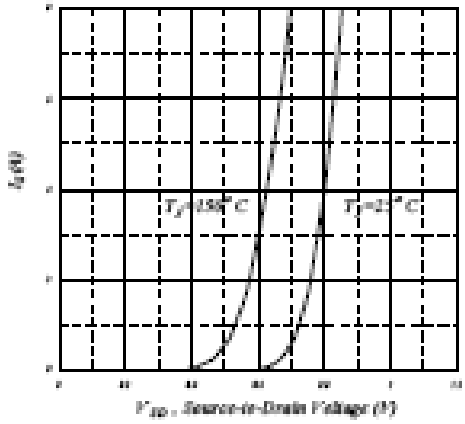


Fig 5. Forward Characteristic of Reverse Diode

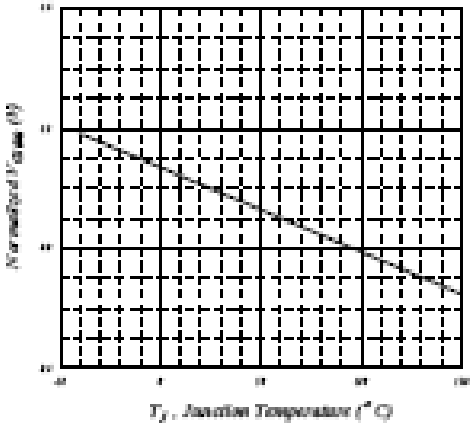


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

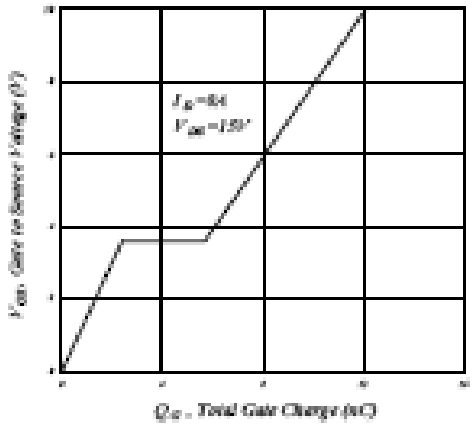


Fig 7. Gate Charge Characteristics

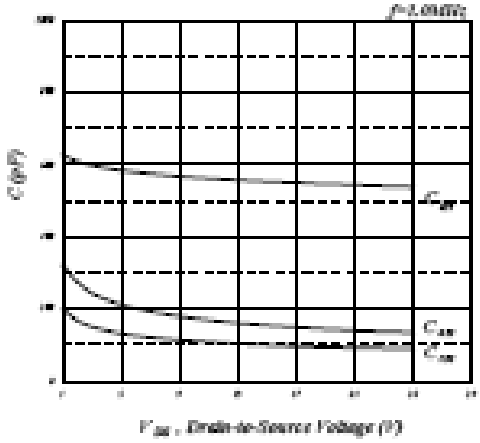


Fig 8. Typical Capacitance Characteristics

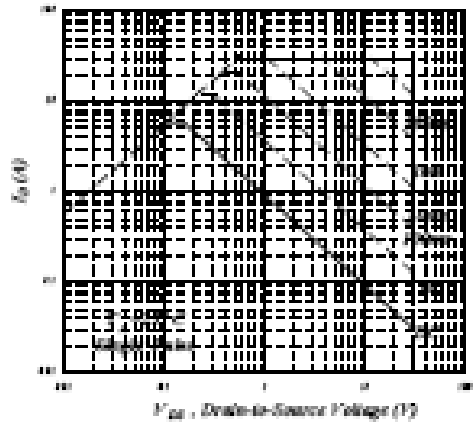


Fig 9. Maximum Safe Operating Area

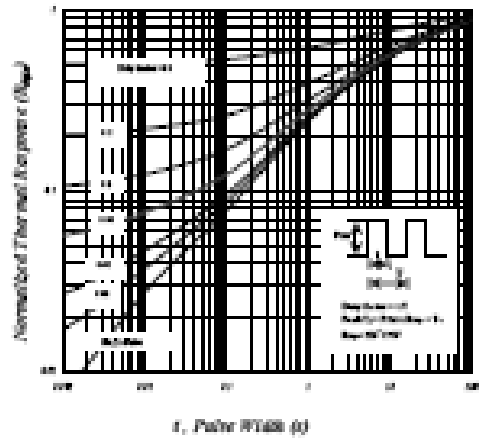


Fig 10. Effective Transient Thermal Impedance

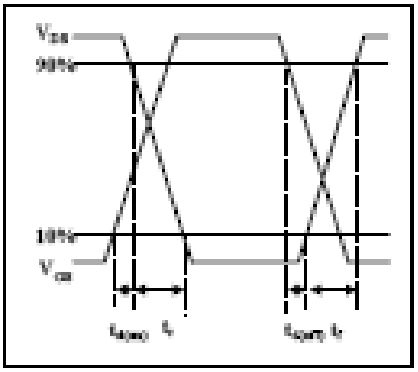


Fig 11. Switching Time Waveform

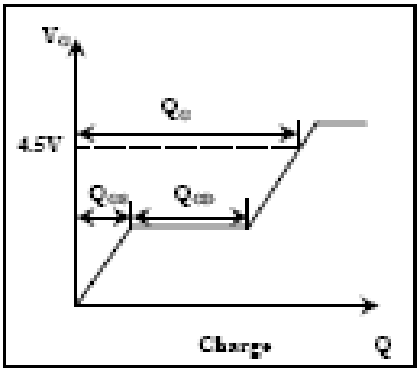


Fig 12. Gate Charge Waveform

P-Channel

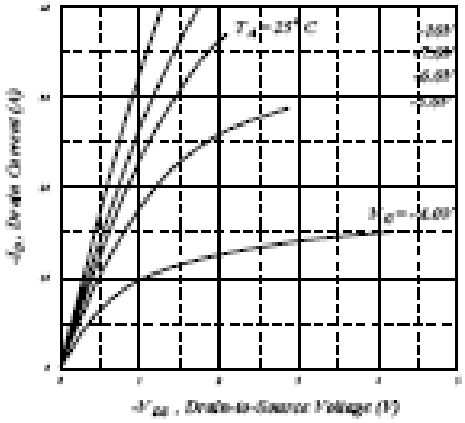


Fig 1. Typical Output Characteristics

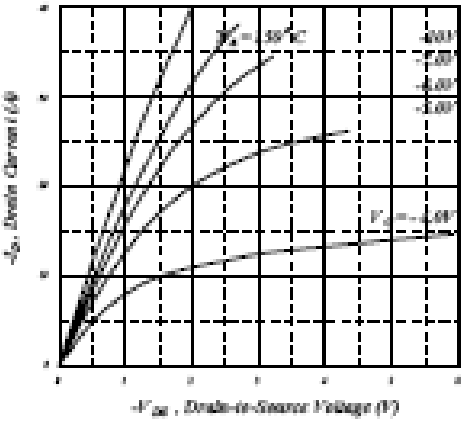


Fig 2. Typical Output Characteristics

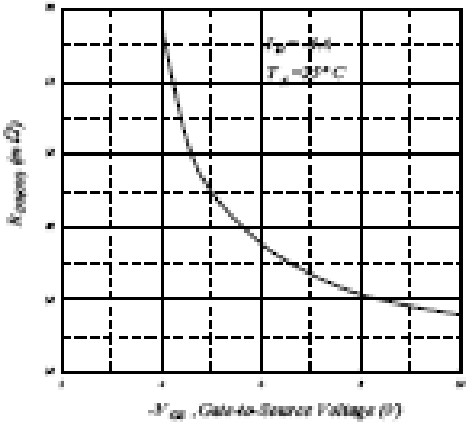


Fig 3. On-Resistance v.s. Gate Voltage

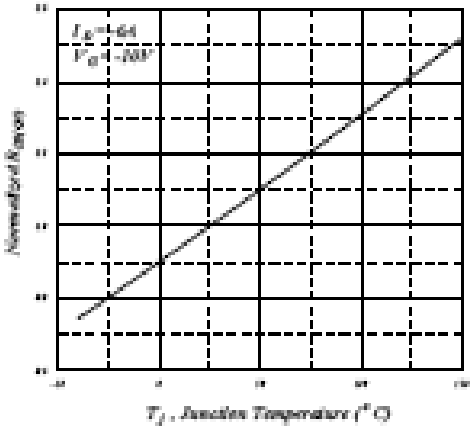


Fig 4. Normalized On-Resistance v.s. Junction Temperature

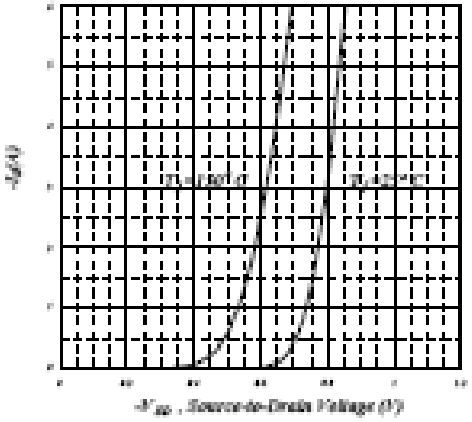


Fig 5. Forward Characteristic of Reverse Diode

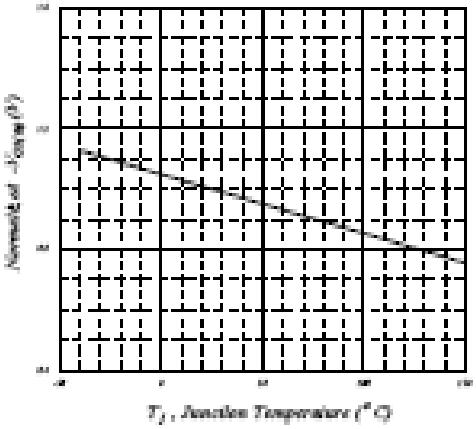


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

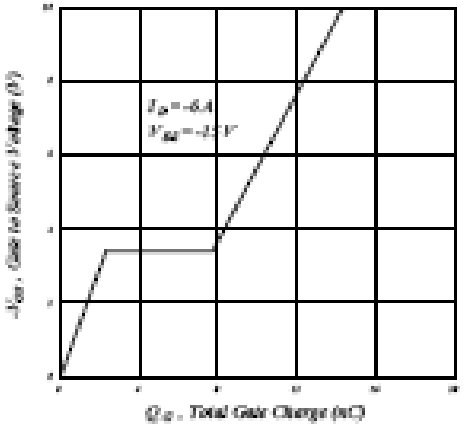


Fig 7. Gate Charge Characteristics

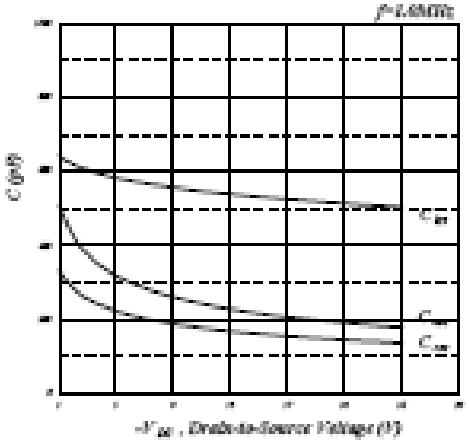


Fig 8. Typical Capacitance Characteristics

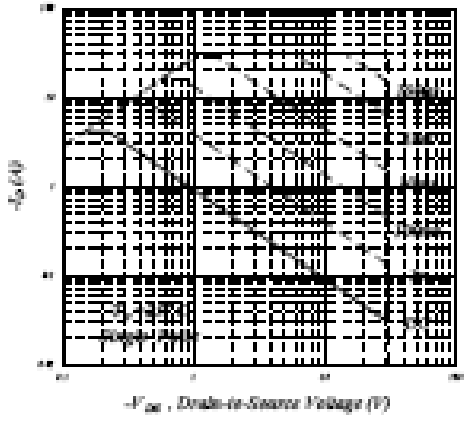


Fig 9. Maximum Safe Operating Area

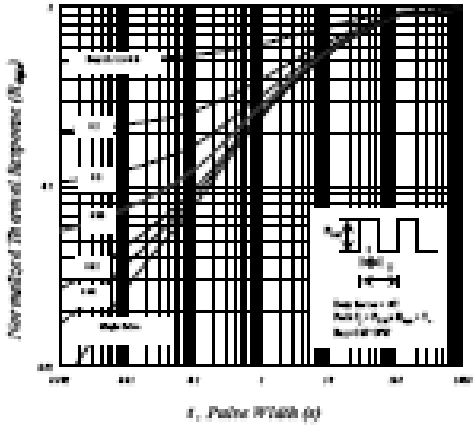


Fig 10. Effective Transient Thermal Impedance

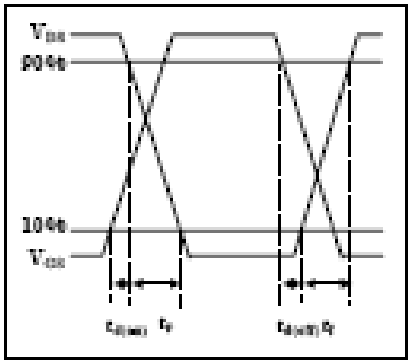


Fig 11. Switching Time Waveform

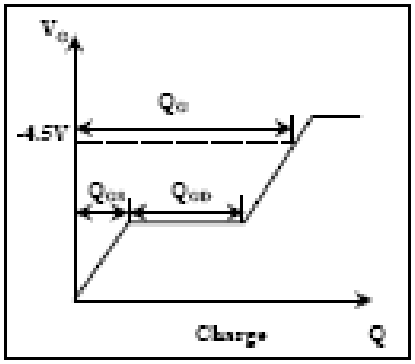
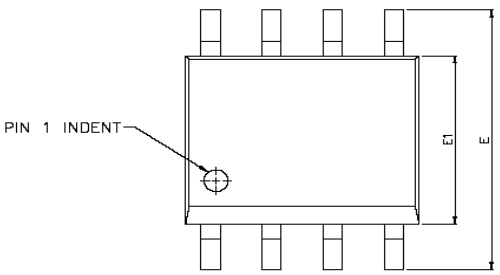
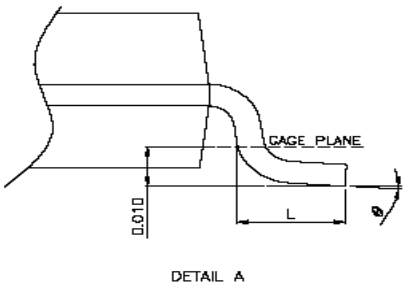
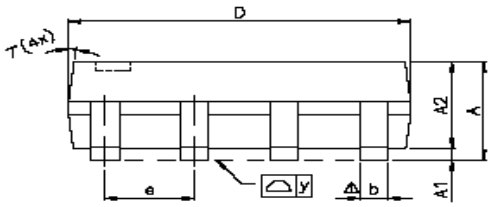


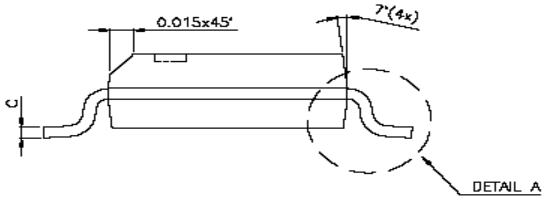
Fig 12. Gate Charge Waveform

SOP- 8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
② y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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