SPT220

FAST SETTLING, WIDEBAND OPERATIONAL AMPLIFIER

General Description

The SPT220 is a wide bandwidth DC-coupled operational amplifier that defines the state-of-the-art in high speed op amps. A -3dB bandwidth of DC to 190MHz is achieved using a current feedback architecture design. Ultra-fast settling time (8nsec to 0.1%) and slew rate (7000V/µsec) make the SPT220 a superior amplifier for pulsed and digital applications.

Since thermal tail has been eliminated, the SPT220 settles fast and remains solidly at the desired level. Flat gain and linear phase (1.2° deviation from linear) from DC to beyond 100MHz help the SPT220 to achieve distortion levels uncommonly low relative to conventional op amps.

Using the SPT220 is as easy as adding power supplies and a gain-setting resistor. The result is reliable, consistent performance because such characteristics as bandwidth and settling time are virtually independent of gain setting. Unlike conventional op amp designs where the optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of -1, maximum slew rate at a gain of +1, et cetera, the SPT220 offers predictable response at gain settings from ±1 to ±50. This, coupled with consistent performance from unit to unit with no external compensation, makes the SPT220 a real time and cost-saver in design and production situations alike.

This combination of features makes the SPT220 appropriate for a broad range of applications. The wide bandwidth, DC coupling, and fast settling lend themselves well to high speed D to A and "flash" A to D applications. Both receivers and transmitters in optical fiber systems have similar requirements. High gain and phase linearity and corresponding low distortion make the SPT220 ideal for many digital communication system applications, such as in the demodulator, where the need for both DC coupling and high frequency amplification creates requirements that are difficult to meet.

The SPT220 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

SPT220AIH -25°C to +85°C 12-pin TO-8 can.

Typical Performance

parameter	gain setting						units
	+4	+20	+50	−4	−20	−50	
−3dB bandwidth	250	190	120	200	190	150	MHz
rise time (2V)	1.6	1.9	2.3	1.6	1.9	2.3	ns
slew rate	7	7	7	7	7	7	V/ns
settling time (0.1%)	10	8	10	8	8	10	ns

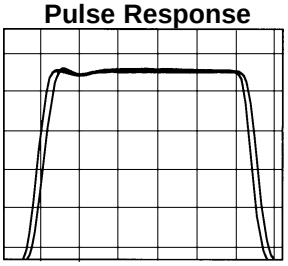
Features

- -3dB bandwidth of 190MHz
- 0.1% settling in 8ns
- 7000V/µs slew rate
- 1.9ns rise and fall times
- Low distortion, linear phase
- Direct replacement for CLC220

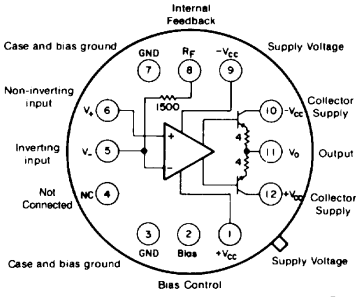
Applications

- Very high-speed A to D, D to A conversion
- High-speed fiber optic systems
- Baseband and video communications
- Radar and IF processors
- Very fast risetime pulse amplifiers

Pulse Response

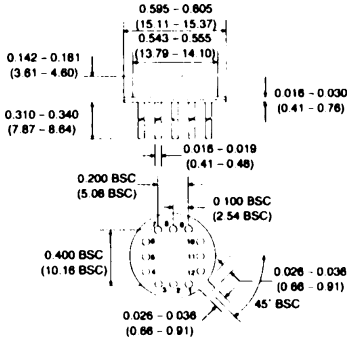


Bottom View



Pin 8 provides access to a 1500 ohm feedback resistor. Pin 2 allows the user to reduce the amplifier supply current or to turn the amplifier off completely.

Package Dimensions



Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA

Phone: (719) 528-2300 FAX: (719) 528-2370 Website: http://www.spt.com E-Mail: sales@spt.com

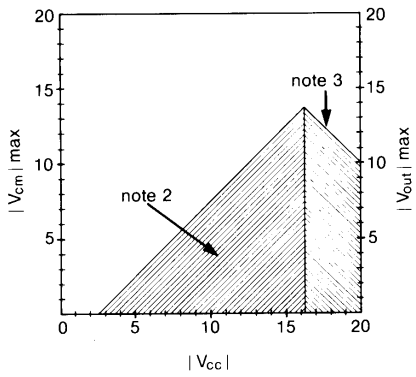
SPT220 Electrical Characteristics (A_V = +20, V_{cc} = ±15V, R_L = 200Ω, R_f = 1500Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	SPT220AIH	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† −3dB bandwidth	V_{out}<2V_{pp}	190	>160	>170	>150	MHz	SSBW
gain flatness at	V_{out}~2V_{pp}						
† peaking	0.1 to 50MHz	0	<0.5	<0.3	<0.4	dB	GFPL
† peaking	>50MHz	0	<1.5	<0.6	<1.0	dB	GFPH
† rolloff	at 100MHz	0	<0.4	<0.6	<0.9	dB	GFR
group delay	to 100MHz	3.0±0.3	—	—	—	ns	GD
linear phase deviation	to 100MHz	1.2	<2	<2	<2	°	LPD
reverse isolation	to 100MHz						
non-inverting		60	>50	>50	>50	dB	RINI
inverting		45	>35	>35	>35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.9	<2.2	<2.1	<2.2	ns	TRS
	5V step	2	<2.6	<2.5	<2.6	ns	TRL
settling time to .02%	5V step[4]	15	—	—	—	ns	TSP
to .1%	5V step[4]	8	<15	<12	<15	ns	TS
overshoot	5V step	7	<15	<12	<12	%	OS
slew rate (overdriven input)		7	>6	>6	>6	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
† 2nd harmonic distortion	2V_{pp}, 20MHz	−58	<−50	<−50	<−50	dBc	HD2
† 3rd harmonic distortion	2V_{pp}, 20MHz	−62	<−50	<−50	<−50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	1kHz to 200MHz	50	<100	<100	<100	μV	INV
noise floor	>5MHz	−156	<−150	<−150	<−150	dBm(1Hz)	SNF
integrated noise	5MHz to 200MHz	50	<100	<100	<100	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		10	<25	<25	<25	mV	VIO
average temperature coefficient		35	<120	<120	<120	μV/°C	DVIO
*input bias current	non-inverting	10	<40	<30	<40	μA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	20	<70	<50	<70	μA	IBI
average temperature coefficient		70	<250	<250	<250	nA/°C	DIBI
*power supply rejection ratio		55	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±10	>±10	>±10	V	VO
internal feedback resistor	absolute tolerance	<0.4	—	—	—	%	RFA

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±50mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

note 1: * AI 100% tested at 25°C.
† AI sample tested at +25°C.

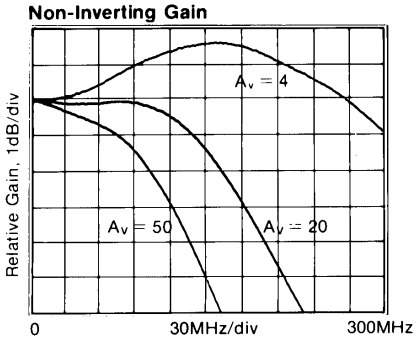
note 2: This rating protects against damage to the input stage caused by saturation of either the input or out stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input volt may be as large as twice the maximum. V_{cm} should never exceed V_{cc} (V_{cm} is the voltage at the non-inver input, pin 6).

note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended is ± 15V.

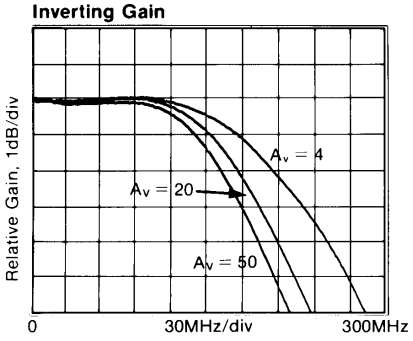
note 4: Settling time specification requires the use of an external feedback resistor (1500Ω).

SPT220 Typical Performance Characteristics (T_A = +25°, A_V = +20, V_{CC} = ±15V, R_L = 200Ω; unless specified)

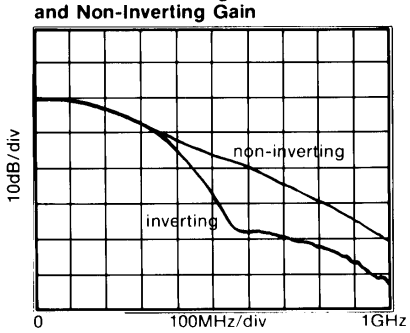
Non-Inverting Gain



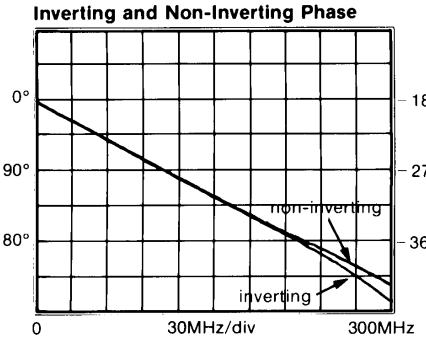
Inverting Gain



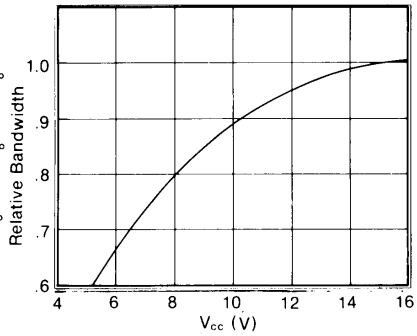
Broadband Inverting and Non-Inverting Gain



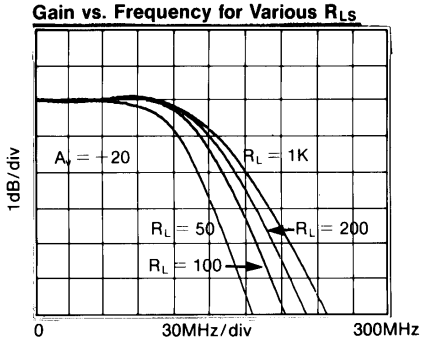
Inverting and Non-Inverting Phase



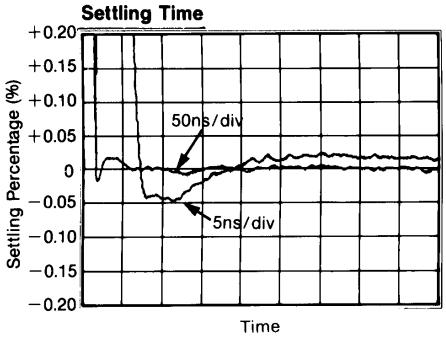
Relative Bandwidth vs. V_{cc}



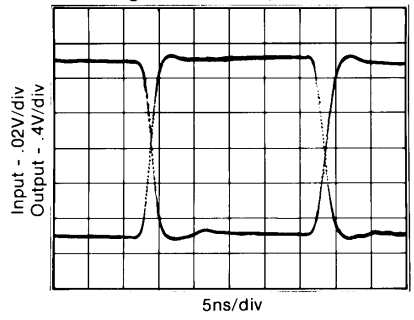
Gain vs. Frequency for Various R_{LS}



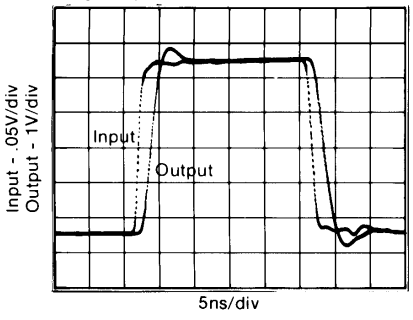
Settling Time



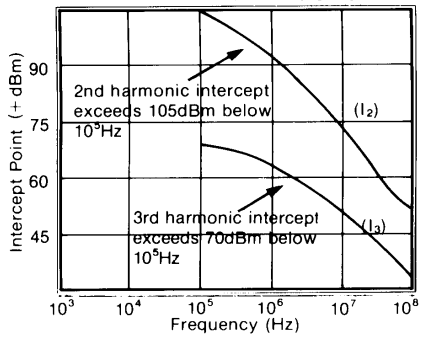
Small Signal Pulse Response (Inv, Non-Inv)



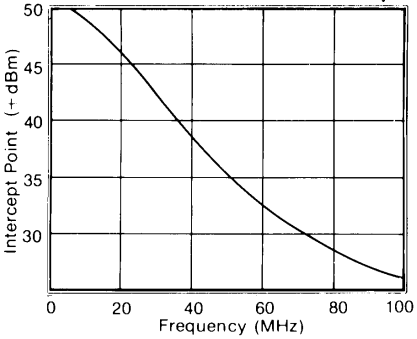
Large Signal Pulse Response



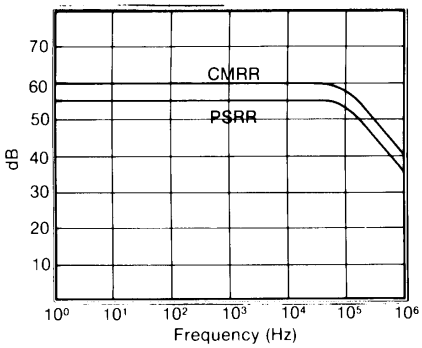
2nd and 3rd Harmonic Distortion Intercept



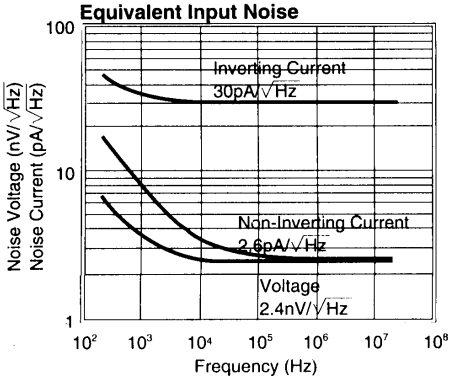
2-Tone 3rd Order Intermod. Intercept

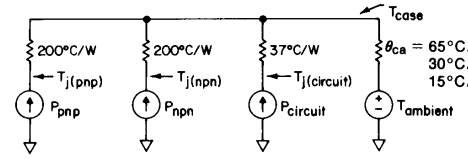


CMRR and PSRR



Equivalent Input Noise





$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where I_{cc} = 26mA at ±15V

$P_{XXX} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 4)](I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and ±V_{cc}.

$T_{j\,(pnp)} = P_{pnp}(200 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(37 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

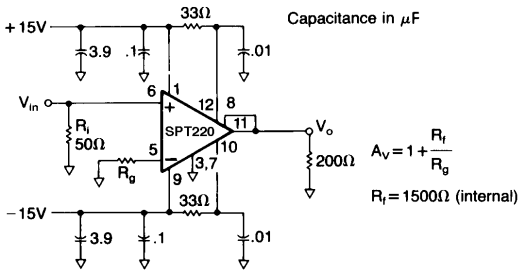


Figure 1: suggested non-inverting gain circuit

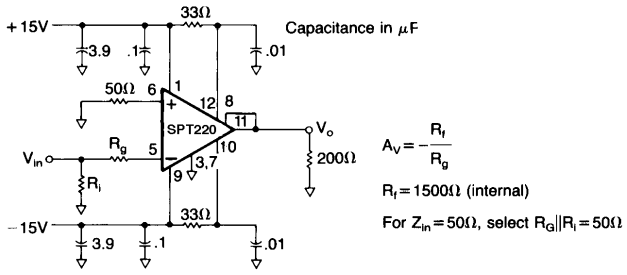


Figure 2: suggested inverting gain circuit

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_f and R_g determines the gain of the SPT220. Unlike conventional op amps, however, the closed loop pole-zero response of the SPT220 is affected very little by the value of R_g. R_g scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_f does influence the feedback and so the SPT220 has been internally compensated for optimum performance with $R_f = 1500Ω$. External R_f values greater than 1500Ω can be used with approximate results as listed in Table 1. Use of R_f values less than 1500Ω will result in extended bandwidth and peaking of the response at high frequencies. For example, $R_f = 1000Ω$ will result in a −3dB bandwidth of about 300MHz, with approximately 3.5dB of peaking above 200MHz. An RC network with a −3dB bandwidth of about 250MHz could be used at the input to flatten the response, although it will reduce the bandwidth of the overall circuit.

Table 1: Bandwidth versus R_f

R_f (kΩ)	$f \pm 0.3$dB (MHz)	$f - 3.0$dB (MHz)
2	25	80
5	10	30

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Distortion and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the SPT220. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the SPT220 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the SPT220 at large output voltage swings (DC component not included) and at high frequencies, observe the (AC output voltage) X (frequency) product specification of 600V • MH_Z. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Operation with Reduced Bias Current

Placing a resistor between pins 1 and 2 will cause the SPT220 bias current to be reduced. A value of 20K will cause only a slight reduction, 3K will almost halve the current, while less than 1K will reduce bias to about 5mA and the amplifier will be off. In this condition, the input signal will be greatly attenuated. In the reduced bias, on condition, bandwidth will be roughly proportional to the reduction in bias current. A mechanical or semiconductor switch can be used to turn the amplifier off. Any connection which would cause current to flow out of pin 2 will result in increased bias current and may lead to device destruction from overheating and excessive current.