

DESCRIPTION

The HY628400A is a high-speed, low power and 4M bits CMOS SRAM organized as 524,288 words by 8 bits. The HY628400A uses Hyundai's high performance twin tub CMOS process technology and was designed for high-speed and low power circuit technology. It is particularly well suited for use in high-density and low power system applications. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0V.

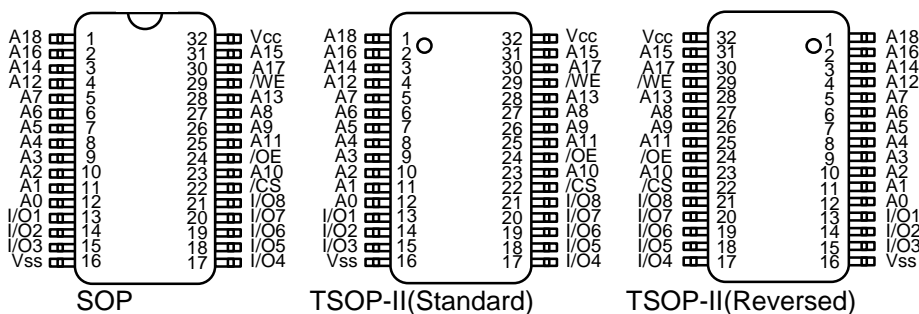
FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
- 2.0V(min) data retention
- Standard pin configuration
- 32pin 525mil SOP
- 32pin 400mil TSOP-II
(Standard and Reversed)

Product No.	Voltage	Speed	Operation	Standby Current(uA)		Temperature
	(V)	(ns)	Current(mA)	L	LL	(°C)
HY628400A	5.0	55/70/85	10	100	30	0~70(Normal)

Note 1. Normal : Normal Temperature
2. Current value are max.

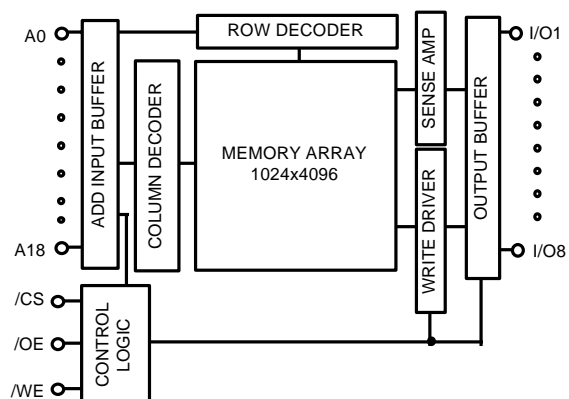
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A18	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY628400ALG	55/70/85	L-part		SOP
HY628400ALLG	55/70/85	LL-part		SOP
HY628400ALT2	55/70/85	L-part		TSOP-II(Standard)
HY628400ALLT2	55/70/85	LL-part		TSOP-II(Standard)
HY628400ALR2	55/70/85	L-part		TSOP-II(Reversed)
HY628400ALLR2	55/70/85	LL-part		TSOP-II(Reversed)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V _{CC} , V _{IN} , V _{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T _A	Operating Temperature	0 to 70	°C	HY628400A
T _{STG}	Storage Temperature	-65 to 125	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

 T_A=0; f_o 70; f_o(Normal)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.5	V
V _{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note :

- V_{IL} = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS1	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note :

- H=V_{IH}, L=V_{IL}, X=don't care

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (Normal) unless otherwise specified

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit	
I _{LI}	Input Leakage Current		V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	-	1	μA	
I _{LO}	Output Leakage Current		V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}	-1	-	1	μA	
I _{CC}	Operating Power Supply Current		/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA	-	5	10	mA	
I _{CC1}	Average Operating Current		/CS = V _{IL} Min Duty Cycle = 100%, I _{I/O} = 0mA	-	50	80	mA	
I _{SB}	TTL Standby Current (TTL Input)		/CS = V _{IH}	-	0.4	2	mA	
I _{SB1}	Standby Current (CMOS Input)	HY628400A	/CS ≥ V _{CC} - 0.2V	L	-	-	100	μA
				LL	-	-	30	μA
V _{OL}	Output Low Voltage		I _{OL} = 2.1Ma	-	-	0.4	V	
V _{OH}	Output High Voltage		I _{OH} = -1Ma	2.4	-	-	V	

Note : Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (Normal) unless otherwise specified

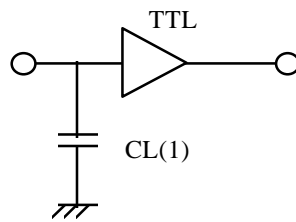
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	t _{RC}	Read Cycle Time	55	-	70	-	85	-	ns
2	t _{AA}	Address Access Time	-	55	-	70	-	85	ns
3	t _{ACS}	Chip Select Access Time	-	55	-	70	-	85	ns
4	t _{OE}	Output Enable to Output Valid	-	25	-	35	-	45	ns
5	t _{CLZ}	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t _{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t _{CHZ}	Chip Deselecting to Output in High Z	0	20	0	25	0	30	ns
8	t _{OHZ}	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	t _{OH}	Output Hold from Address Change	10	-	10	-	10	-	ns
WRITE CYCLE									
10	t _{WC}	Write Cycle Time	55	-	70	-	85	-	ns
11	t _{CW}	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	t _{AW}	Address Valid to End of Write	45	-	60	-	70	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
14	t _{WP}	Write Pulse Width	40	-	50	-	55	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	0	-	ns
16	t _{WHZ}	Write to Output in High Z	0	20	0	25	0	30	ns
17	t _{DW}	Data to Write Time Overlap	25	-	30	-	35	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

TA = 0°C to 70°C (Normal) unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

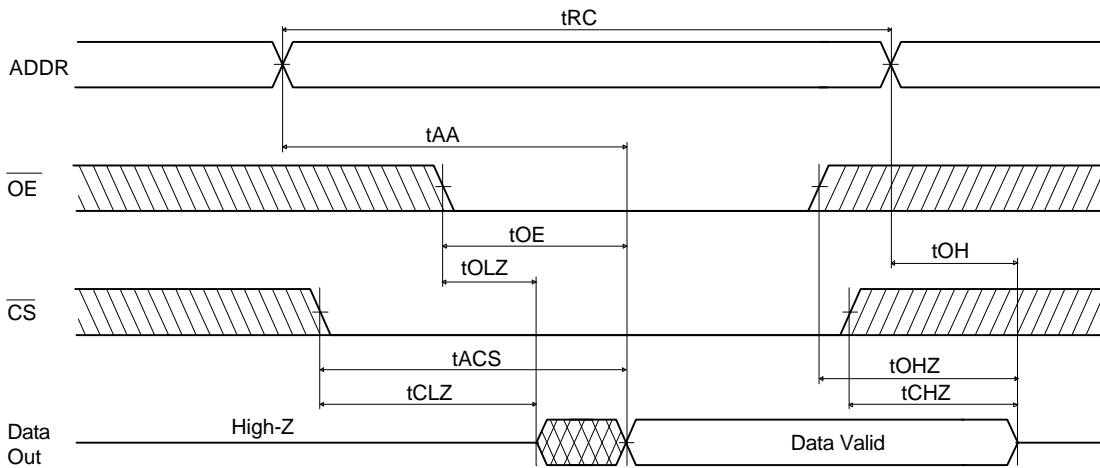
Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VI/O = 0V	8	pF

Note : This parameter is sampled and not 100% tested

TIMING DIAGRAM

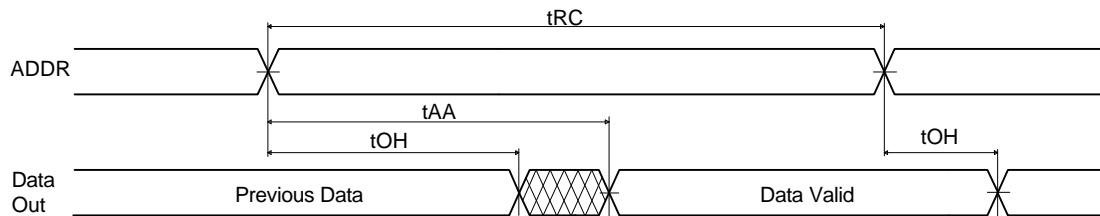
READ CYCLE 1



Note(READ CYCLE):

1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. \overline{WE} is high for the read cycle.

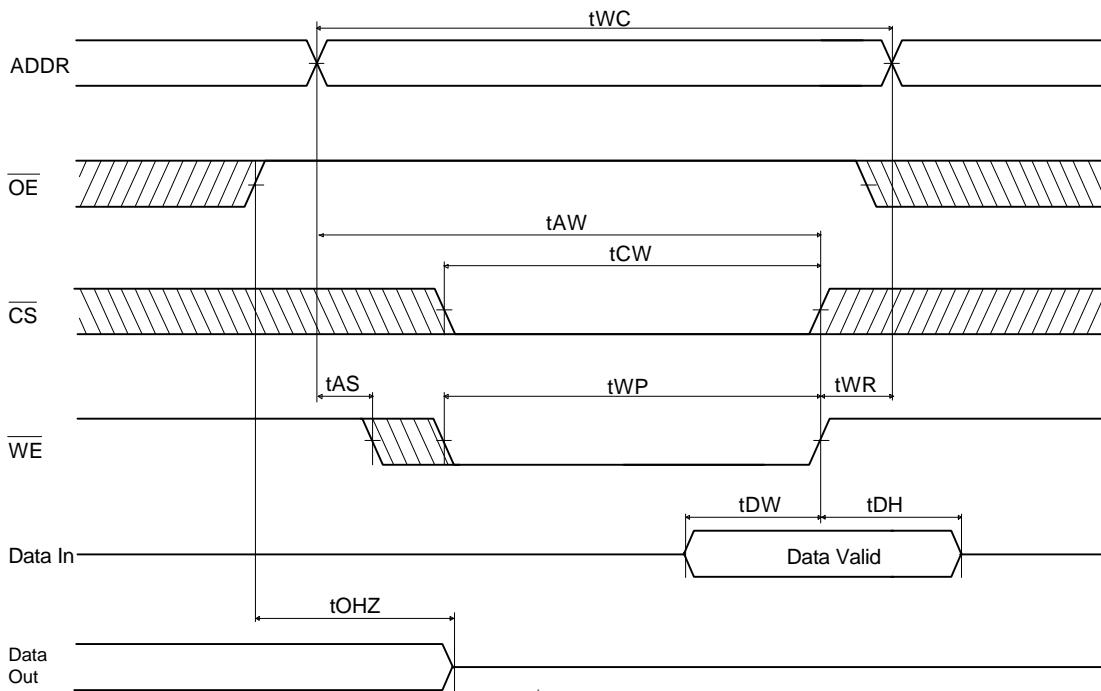
READ CYCLE 2



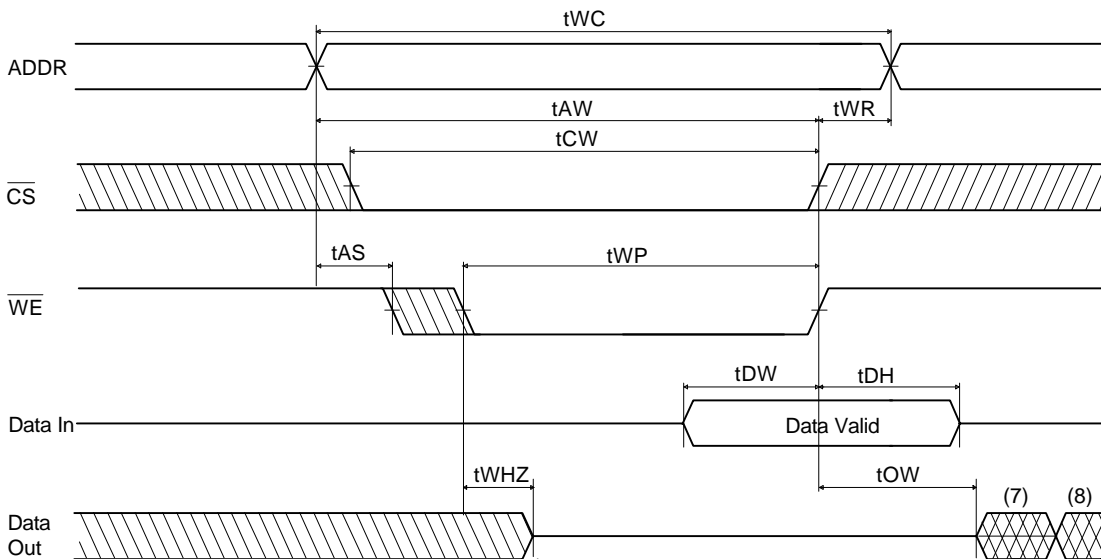
Note(READ CYCLE):

1. \overline{WE} is high for the read cycle.
2. Device is continuously selected $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$.

WRITE CYCLE 1 (/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and low /WE. A write begins at the latest transition among /CS going low /WE going low: A write end at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of /CS going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS is low, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION ELECTRIC CHARACTERISTIC

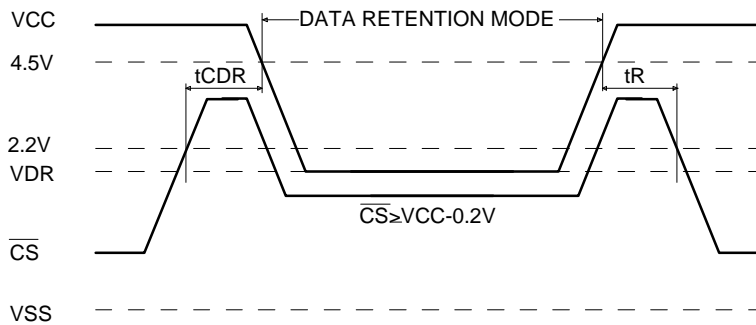
TA=0°C to 70°C (Normal)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
VDR	Vcc for Data Retention		$\overline{CS} \geq V_{CC} - 0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$	2.0	-	-	V
ICCDR	Data Retention Current	HY628400A	Vcc = 3.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	50	uA
				LL	-	15	uA
tCDR	Chip Deselect to Data Retention Time			0	-	-	ns
tR	Operating Recovery Time			tRC(2)	-	-	ns

Notes:

1. Typical values are at the condition of TA = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

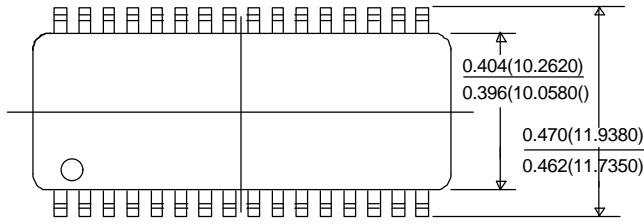


RELIABILITY SPEC.

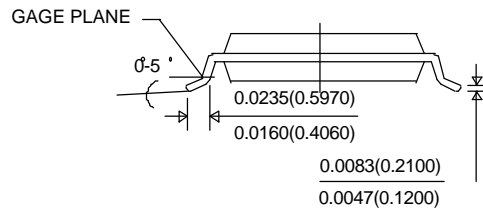
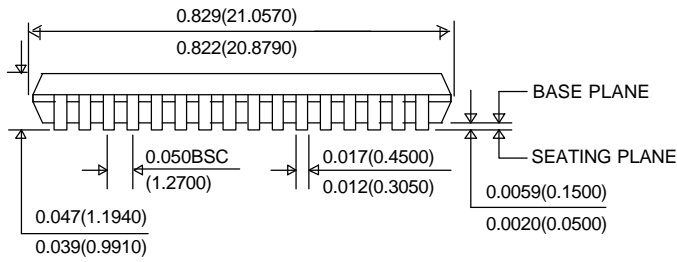
TEST MODE		TEST SPEC.
ESD	HBM	$\geq 2000V$
	MM	$\geq 250V$
LATCH - UP		$\leq -100mA$
		$\geq 100mA$

PACKAGE INFORMATION

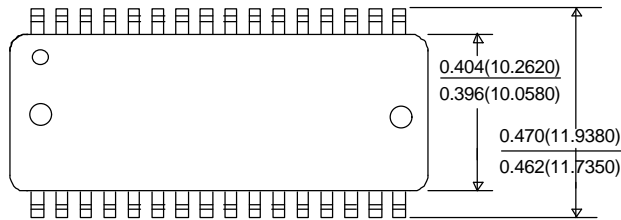
32pin 400mil Thin Small Outline Package Standard(T2)



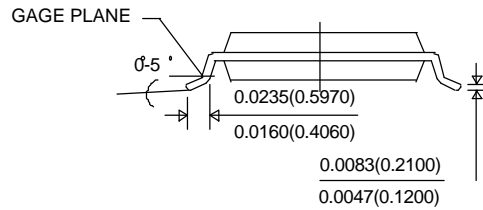
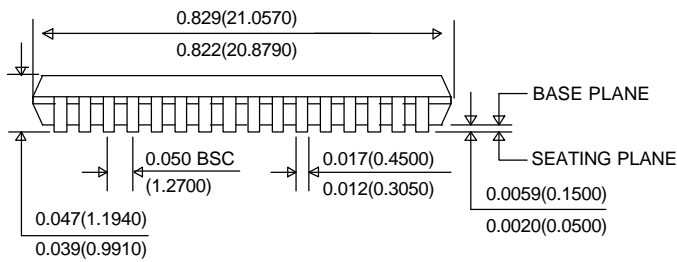
UNIT : INCH(mm) MAX. MIN.



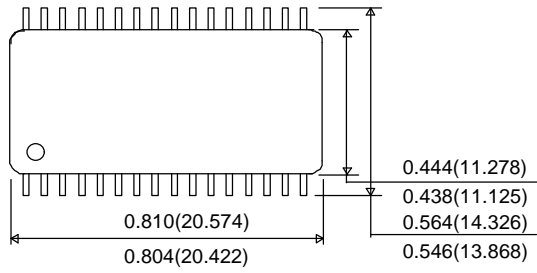
32pin 400mil Thin Small Outline Package Reversed(R2)



UNIT : INCH(mm) MAX. MIN.



32pin 525mil Small Outline Package(G)



UNIT : INCH(mm)

