# Micron Parallel NOR Flash Embedded Memory

## Top/Bottom Boot Block 5V Supply

## M29F200FT/B, M29F400FT/B, M29F800FT/B, M29F160FT/B

## Features

- Supply voltage
  - $V_{CC}$ = 5V
- Access time: 55ns
- Program/erase controller
  - Embedded byte/word program algorithms
- Erase suspend and resume modes
- Low power consumption
  - Standby and automatic standby
- 100,000 PROGRAM/ERASE cycles per block
- Electronic signature
  - Manufacturer code: 0x01h
- Top device codes
  - M29F200FT: 0x2251
  - M29F400FT: 0x2223
  - M29F800FT: 0x22D6
  - M29F160FT: 0x22D2
- Bottom device codes
  - M29F200FB: 0x2257
  - M29F400FB: 0x22AB
  - M29F800FB: 0x2258
  - M29F160FB: 0x22D8
- RoHS-compliant packages
  - TSOP48
  - SO44 (16Mb not available for this package)
- Automotive device grade 3
  - Temperature: –40 to +125°C
- Automotive device grade 6
  - Temperature: –40 to +85°C
- Automotive grade certified (AEC-Q100)


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## Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

**Table 1: Part Number Information**

| Part Number Category | Category Details |
|---|---|
| Device Type | M29F = 5V |
| Density | 200 = 2Mb |
| | 400 = 4Mb |
| | 800 = 8Mb |
| | 160 = 16Mb (not available in SO 44 package) |
| Technology | F = 110nm |
| Configuration | T = Top boot |
| | B = Bottom boot |
| Speed | 55 = 55ns device speed in conjunction with temperature range = 3, which denotes Auto Grade –40 to 125 °C parts |
| | 5A = 55ns access time (Auto Grade) only in conjunction with the Grade 6 option |
| Package | M = SO 44 |
| | N = TSOP 48 12mm x 20mm AL 42 |
| Temperature Range | 6 = –40°C to +85°C |
| | 3 = –40°C to +125°C |
| Shipping Options | blank = standard packing (Tray) |
| | E = RoHS-compliant package, standard packing (tray) |
| | T = Tape and reel packing (24mm) |
| | F = RoHS-compliant package, tape and reel packing (24mm) |
| Fab Location | 2 = Fab 13 (Singapore) |


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# General Description

This description applies specifically to the M29F 16Mb (2 Meg x 8 or 1 Meg x 16) nonvolatile memory device, but also applies to lower densities. The device enables READ, ERASE, and PROGRAM operations using a single, low-voltage (4.5–5.5V) supply. On power-up, the device defaults to read mode and can be read in the same way as a ROM or EPROM.

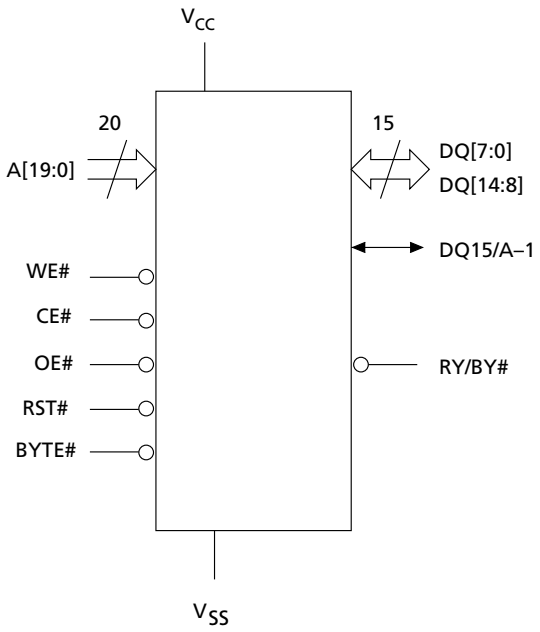
The device is divided into blocks that can be erased independently, preserving valid data while old data is erased. Each block can be protected independently to prevent accidental PROGRAM or ERASE operations from modifying the memory. PROGRAM and ERASE commands are written to the command interface. An on-chip program/erase controller simplifies the process of programming or erasing the device by managing the operations required to update the memory contents.

The end of a PROGRAM or ERASE operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks are asymmetrically arranged. The first or last 64KB have been divided into four additional blocks. The 16KB boot block can be used for small initialization code to start the microprocessor. The two 8KB parameter blocks can be used for parameter storage. The remaining 32KB is a small main block where the application may be stored.

CE#, OE#, and WE# control the bus operation of the memory. They enable simple connection to most microprocessors, often without additional logic. Devices are offered in 48-pin TSOP (12mm x 20mm) and 44-pin small-outline packages. The device is supplied with all the bits erased (set to 1).

**Figure 1: Logic Diagram**





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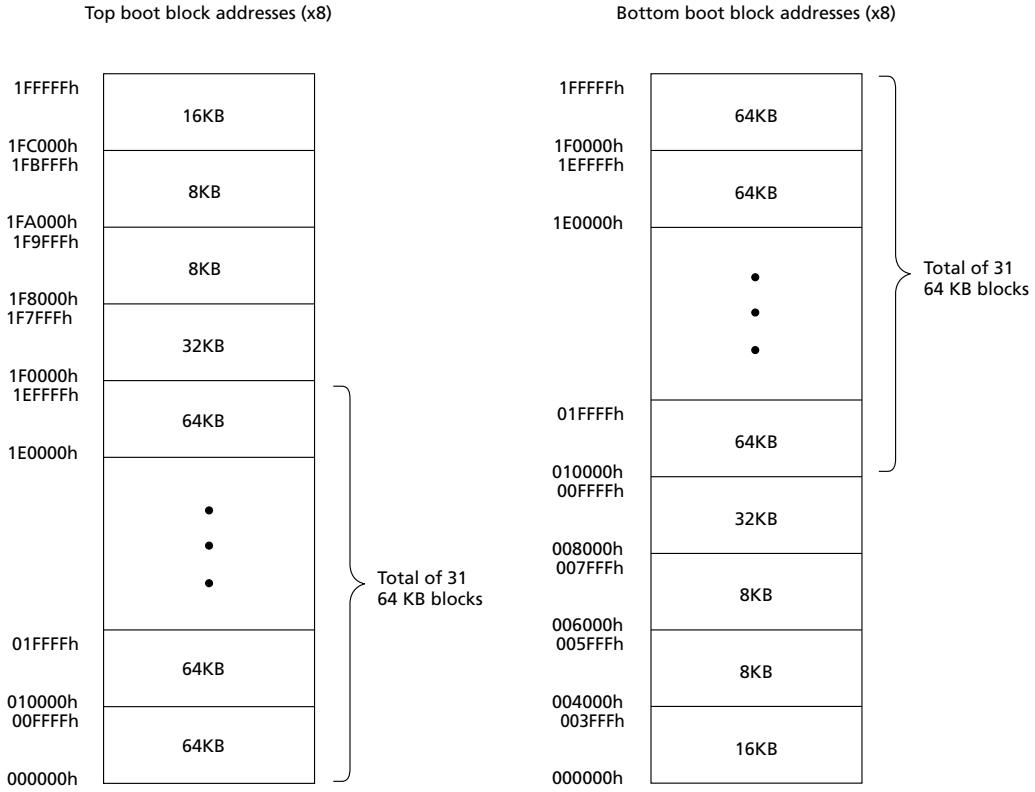
## Figure 2: Block Addresses, M29F160 (x8)





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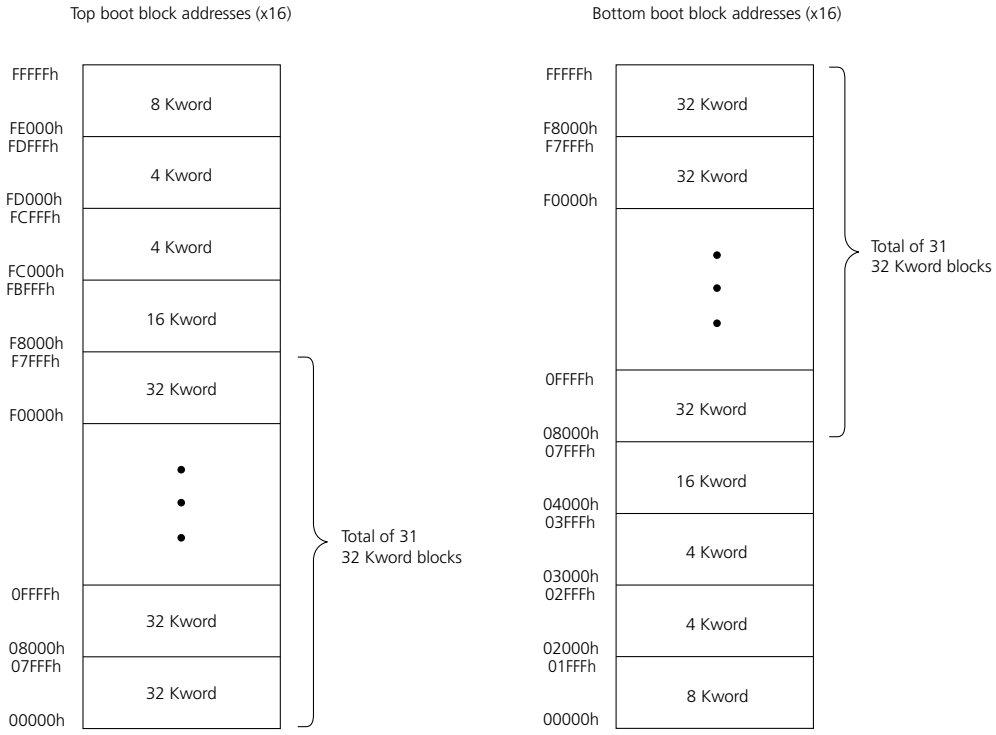
## Figure 3: Block Addresses, M29F160 (x16)





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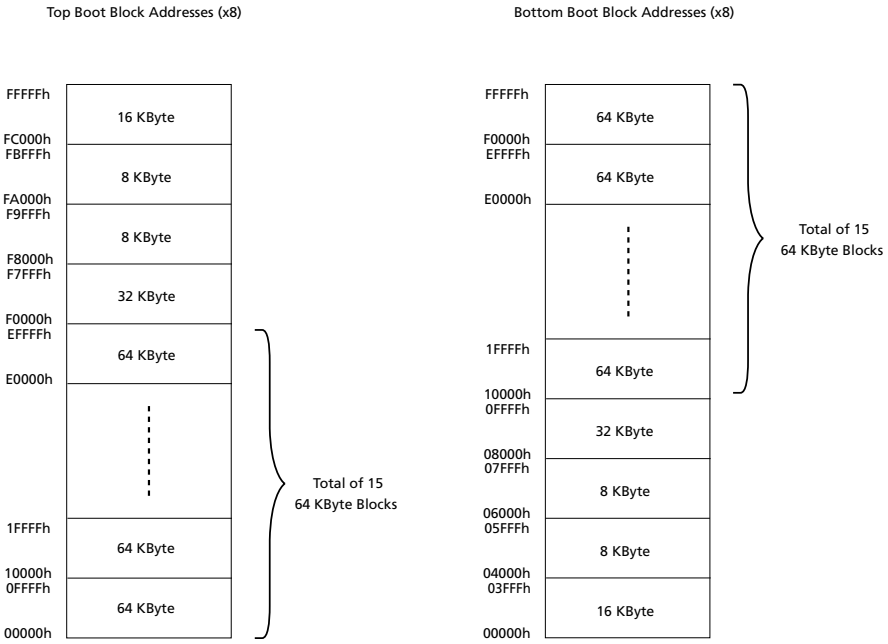
## Figure 4: Block Addresses, M29F800 (x8)





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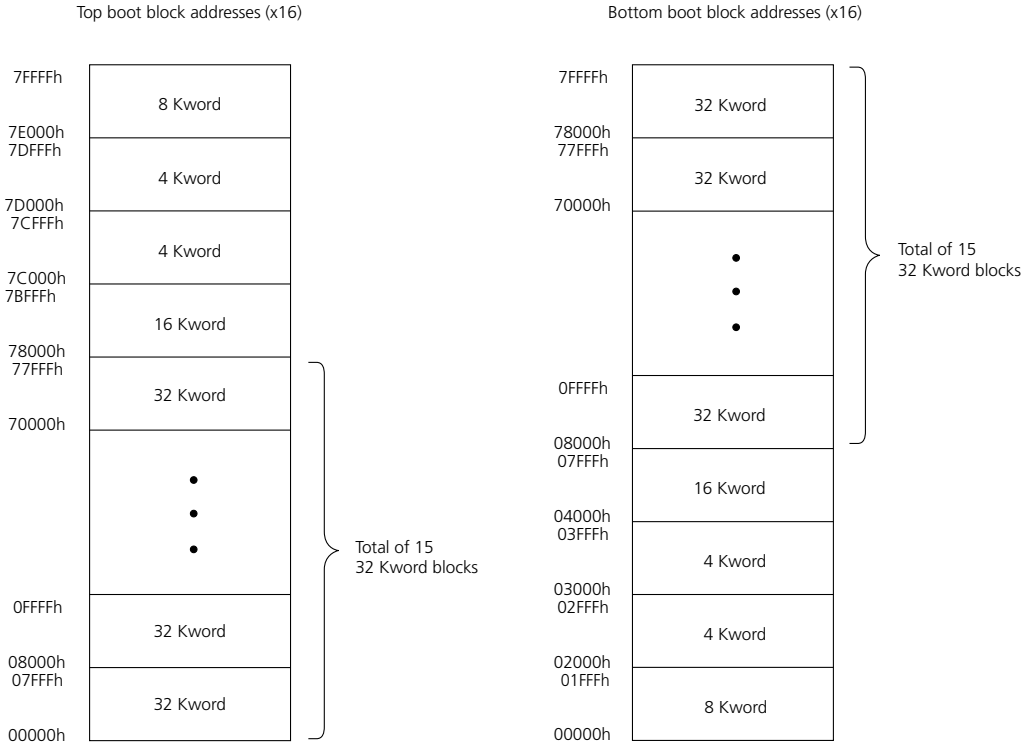
## Figure 5: Block Addresses, M29F800 (x16)





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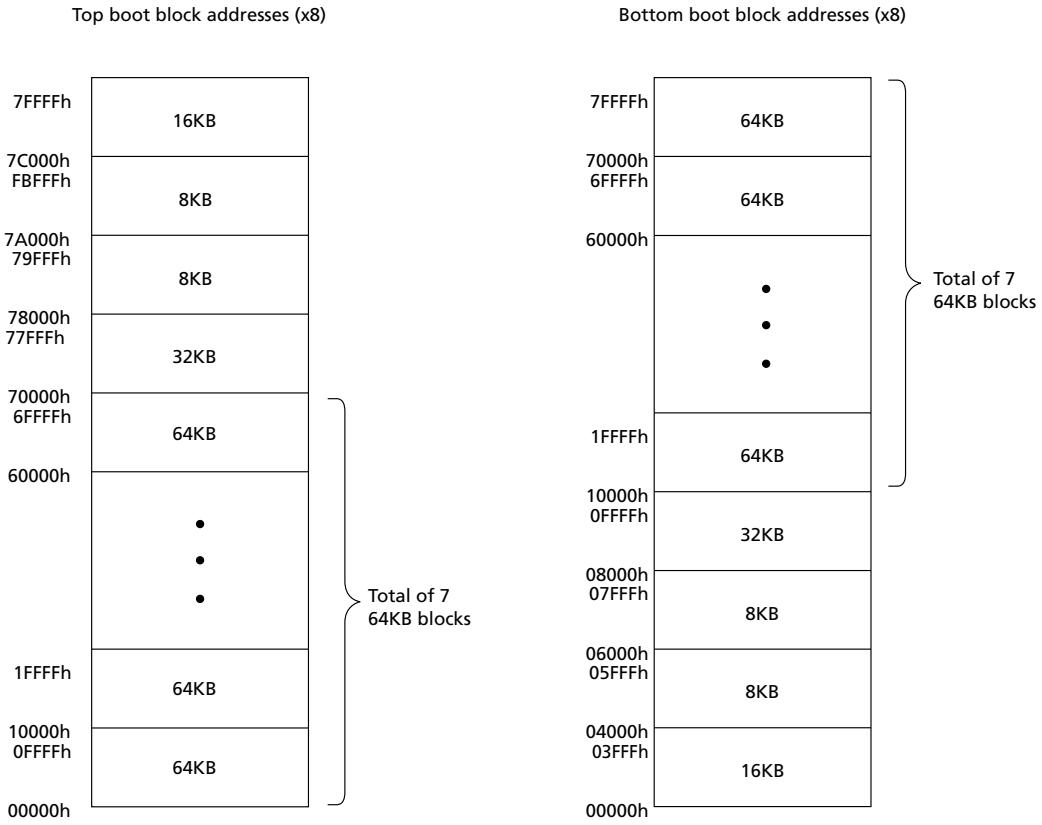
## Figure 6: Block Addresses, M29F400 (x8)





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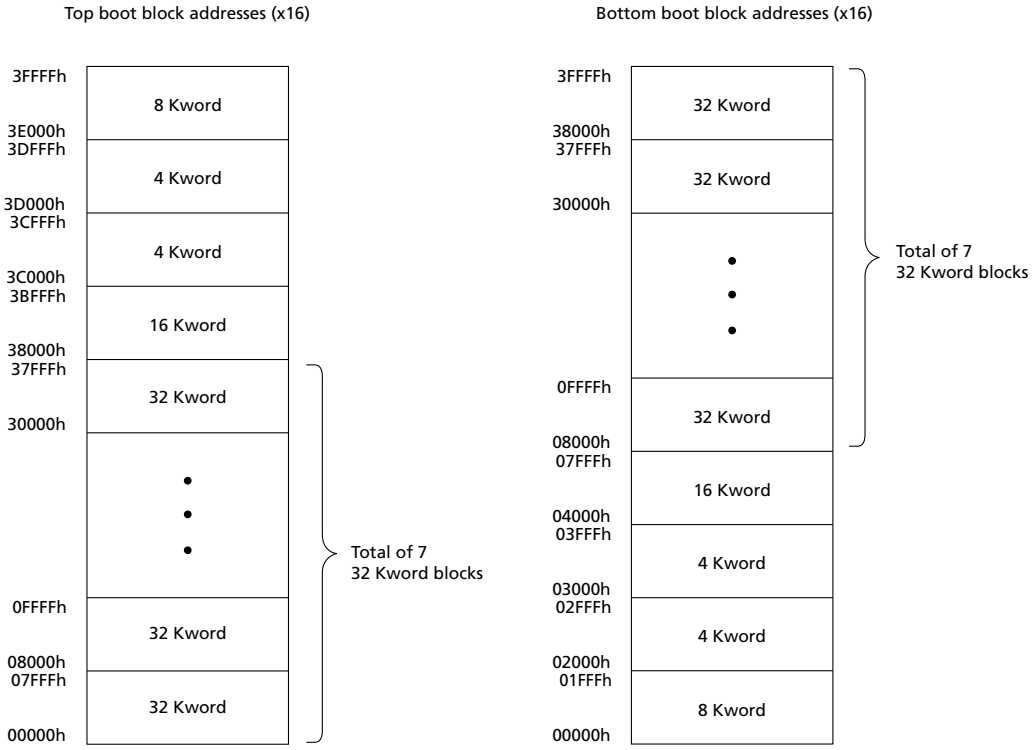
## Figure 7: Block Addresses, M29F400 (x16)





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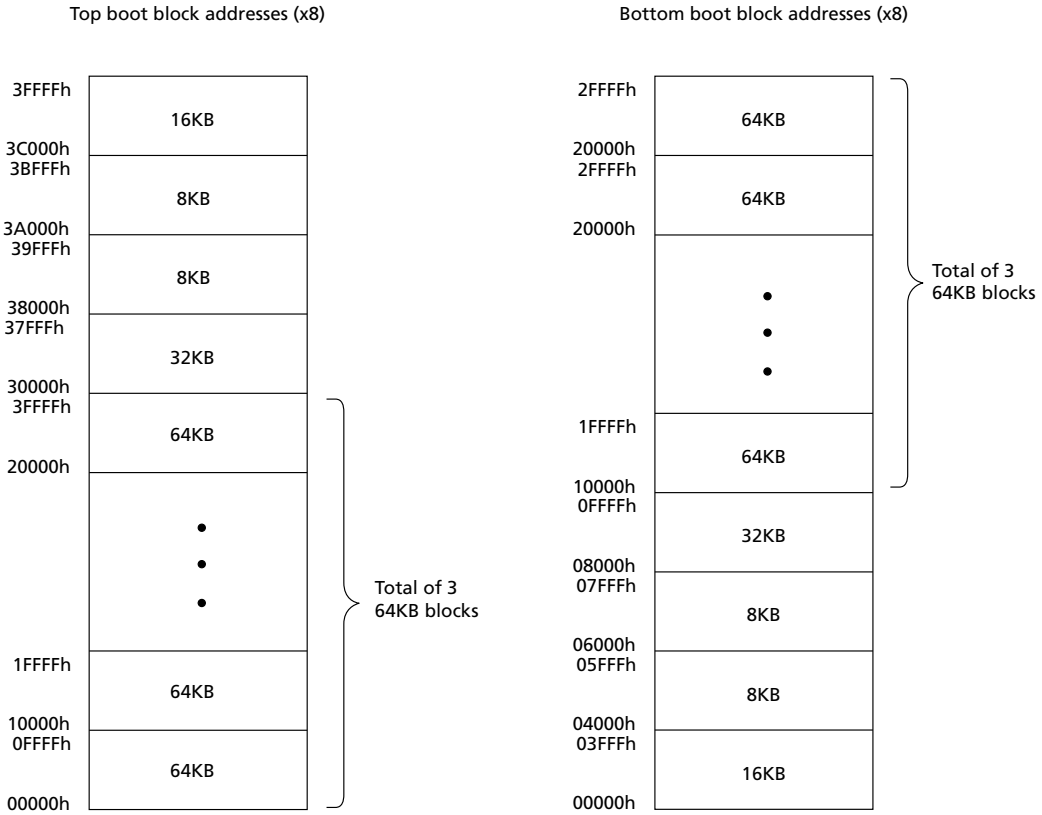
## Figure 8: Block Addresses, M29F200 (x8)





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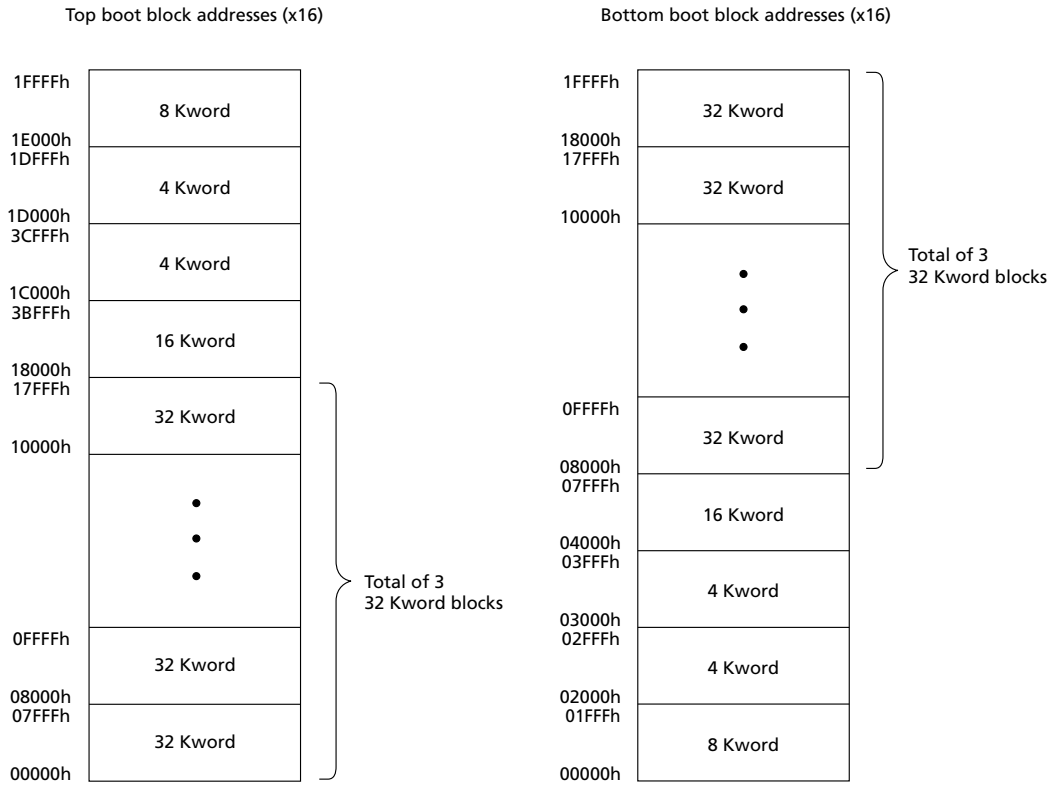
## Figure 9: Block Addresses, M29F200 (x16)





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# Signal Assignments

## TSOP Pin Assignments

**Figure 10: M29F160F**

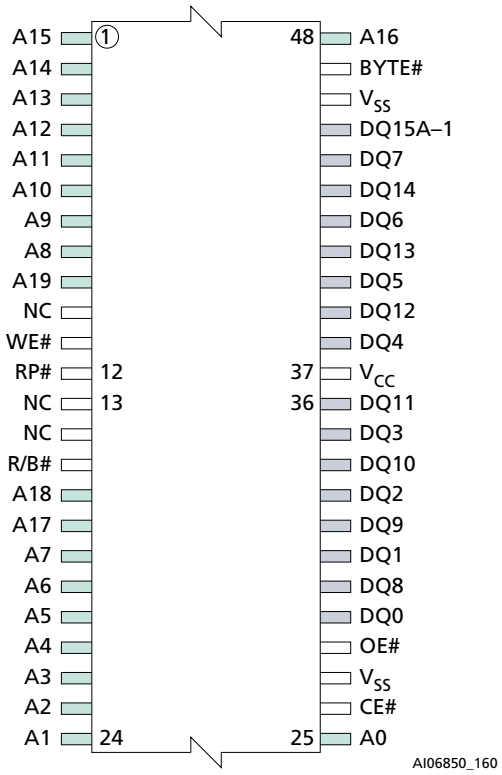



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**Figure 11: M29F800F**

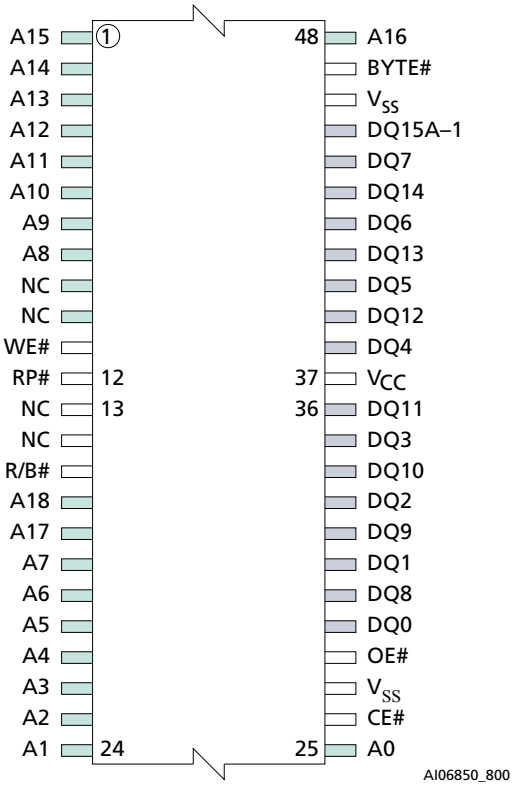



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**Figure 12: M29F400F**

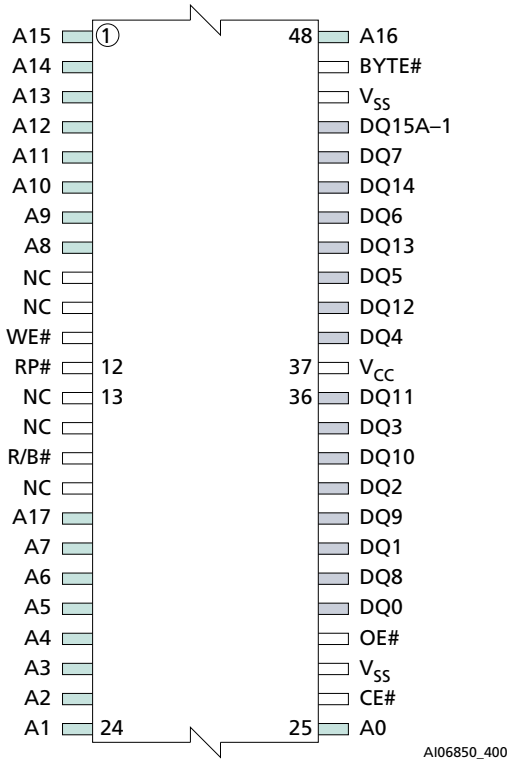




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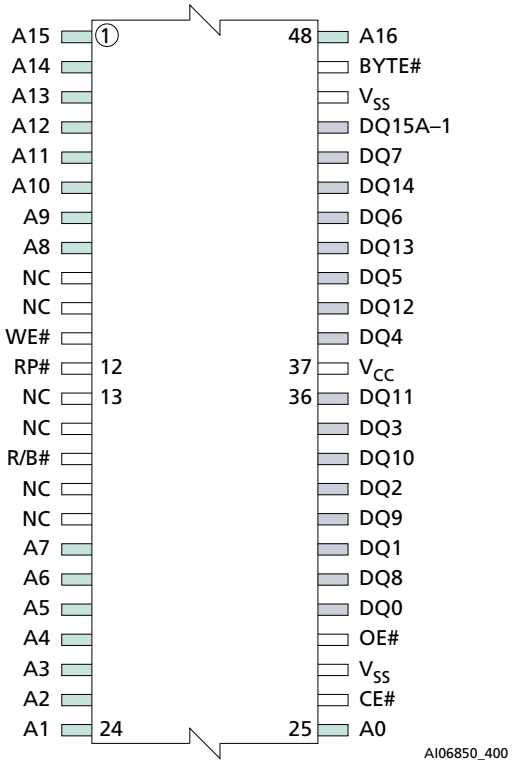
**Figure 13: M29F200F**





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## Small-Outline Pin Assignments

**Figure 14: M29F800**

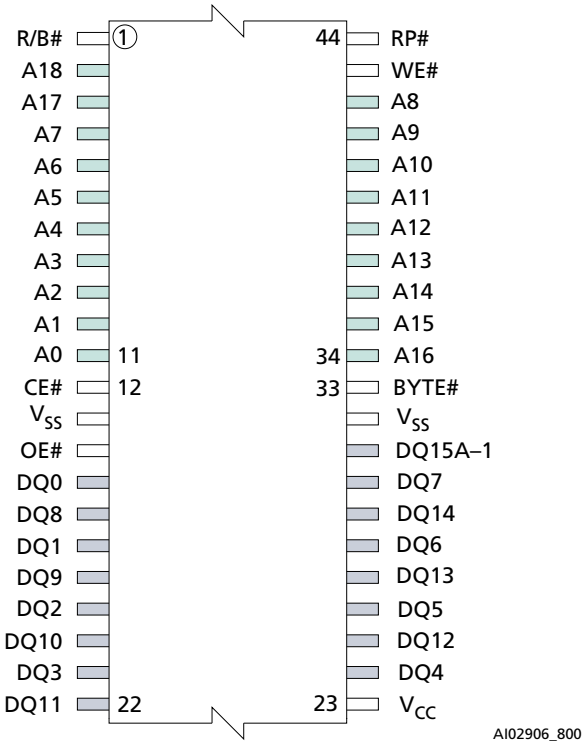



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**Figure 15: M29F400**

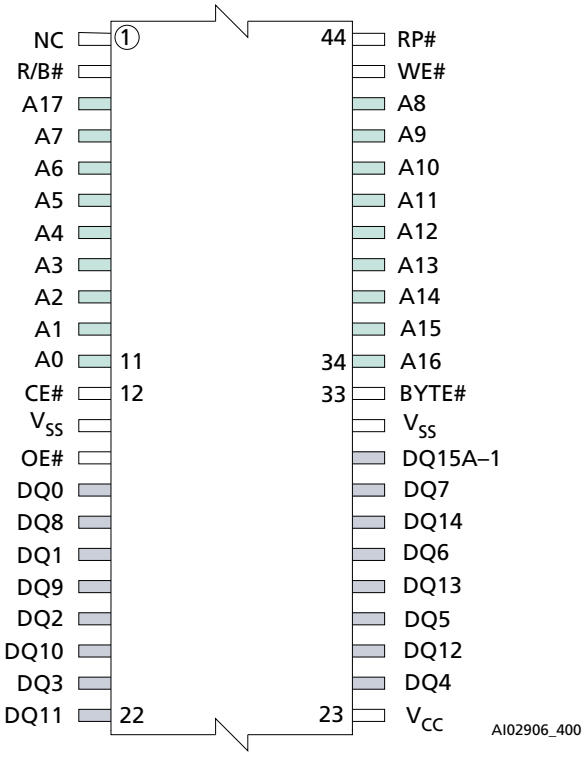



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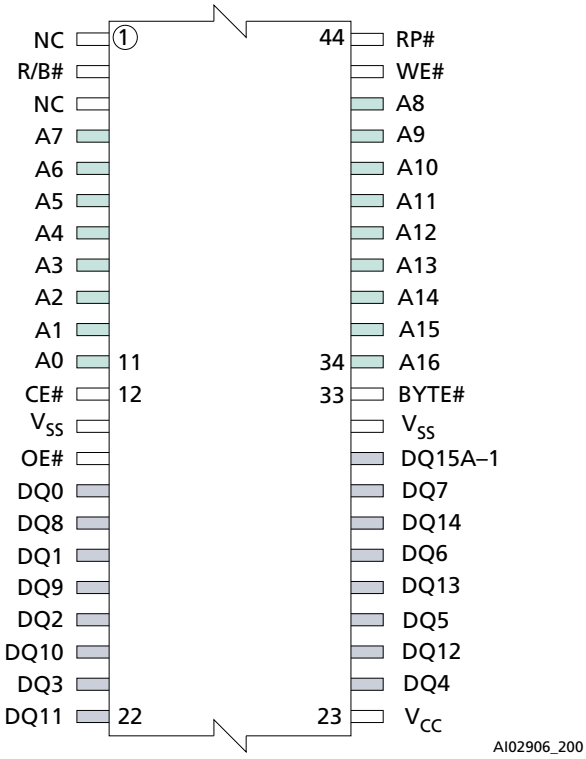
**Figure 16: M29F200**





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# Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

**Table 2: Signal Descriptions**

| Name | Type | Description |
|---|---|---|
| A[MAX:0] | Input | **Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller. |
| CE# | Input | **Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, all other pins are ignored. |
| OE# | Input | **Output enable:** Controls the bus READ operation. |
| WE# | Input | **Write enable:** Controls the bus WRITE operation of the command interface. |
| BYTE# | Input | **Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode. |
| RST# | Input | **Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least $^{t}$PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after $^{t}$PHEL or $^{t}$RHEL, whichever occurs last).<br>Holding RST# at $V_{ID}$ will temporarily unprotect the protected blocks. PROGRAM and ERASE operations on all blocks will then be possible. The transition from $V_{IH}$ to $V_{ID}$ must be slower than $^{t}$PHPHH. |
| DQ[7:0] | I/O | **Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the program/erase controller. |
| DQ[14:8] | I/O | **Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored. |
| DQ15/A-1 | I/O | **Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address.<br>Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode). |
| RY/BY# | Output | **Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details).<br>The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to $V_{CCQ}$. A low value will then indicate that one (or more) of the devices is (are) busy. |


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**Table 2: Signal Descriptions (Continued)**

| Name | Type | Description |
|---|---|---|
| $V_{CC}$ | Supply | **Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when $V_{CC} < V_{LKO}$. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid.<br>A 0.1µF capacitor should be connected between $V_{CC}$ and $V_{SS}$ to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics). |
| $V_{SS}$ | Supply | **Ground:** Reference for all voltage measurements. All $V_{SS}$ pins must be connected to the system ground. |
| NC | – | **Not connected:** Not connected internally. |


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# Bus Operations

### Table 3: Bus Operations

Notes 1 through 2 apply to entire table

| Operation | CE# | OE# | WE# | 8-Bit Mode | | | 16-Bit Mode | |
|---|---|---|---|---|---|---|---|---|
| | | | | A[MAX:0], DQ15/A-1 | DQ[14:8] | DQ[7:0] | A[MAX:0] | DQ15/A-1, DQ[14:0] |
| READ | L | L | H | Cell address | High-Z | Data output | Cell address | Data output |
| WRITE | L | H | L | Command address | High-Z | Data input | Command address | Data input |
| OUTPUT DISABLE | X | H | H | X | High-Z | High-Z | X | High-Z |
| STANDBY | H | X | X | X | High-Z | High-Z | X | High-Z |

Notes: 1. H = Logic level HIGH ($V_{IH}$); L = Logic level LOW ($V_{IL}$); X = HIGH or LOW.
2. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

## Read

Bus READ operations read from the memory cells or specific registers in the command interface. A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

## Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

## Output Disable

Data I/Os are High-Z when OE# is HIGH.

## Standby

When CE# is HIGH, the device enters standby, and data I/Os are High-Z. To reduce the supply current to the standby supply current ($I_{CC2}$), CE# must be held within $V_{CC}$ ±0.2V. (See DC Characteristics.) During PROGRAM or ERASE operations the device will continue to use the program/erase supply current ($I_{CC3}$) until the operation completes.

## Automatic Standby

If CMOS levels ($V_{CC}$ ±0.2V) are used to drive the bus, and the bus is inactive for 150ns or more, the device enters automatic standby, and the internal supply current is reduced to that of the standby supply current, $I_{CC2}$. The data I/Os will output data if a READ operation is in progress.


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# Command Interface

All WRITE operations are interpreted by the command interface. Commands consist of one or more sequential WRITE operations. Failure to observe a valid sequence will result in the memory returning to read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode.

## READ/RESET Command

The READ/RESET command returns the device to read mode, where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the status register. Either one or three WRITE operations can be used to issue the READ/RESET command.

The READ/RESET command can be issued, between WRITE cycles, before the start of a PROGRAM or ERASE operation, to return the device to read mode. Once the PROGRAM or ERASE operation has started, the READ/RESET command is no longer accepted. The READ/RESET command will not abort an ERASE operation when issued while in erase suspend.

## AUTO SELECT Command

The AUTO SELECT command is used to read the electronic signature, including the manufacturer code, the device code and the block protection status. Three consecutive WRITE operations are required to issue the AUTO SELECT command. Once the command is issued, the memory remains in auto select mode until a READ/RESET command is issued. READ CFI QUERY and READ/RESET commands are accepted in auto Select mode, while all other commands are ignored.

**Note:** These operations are intended for use by programming equipment and are not typically used in applications. They require $V_{ID}$ to be applied to some of the pins.

From the auto select mode the manufacturer code can be read using a READ operation with A0 = $V_{IL}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$. The manufacturer code for Micron is 0001h.

The device code can be read using a READ operation with A0 = $V_{IH}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$.

The block protection status of each block can be read using a READ operation with A0 = $V_{IL}$, A1 = $V_{IH}$, and A12-A19 specifying the address of the block. The other address bits may be set to either $V_{IL}$ or $V_{IH}$. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output. See Block Protection Operations for information on the block protection status; the Programmer Technique Block Protection table includes block protection bus READ information.


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**Table 4: Read Electronic Signature**

Notes 1 applies to entire table.

| Operation | CE# | OE# | WE# | 8-Bit Mode | | | 16-Bit Mode | |
|---|---|---|---|---|---|---|---|---|
| | | | | A[MAX:0], DQ15/A-1 | DQ[14:8] | DQ[7:0] | A[MAX:0] | DQ15/A-1, DQ[14:0] |
| READ MANUFACTURER CODE | L | L | H | A0 = $V_{IL}$, A1 = $V_{IL}$, A9 = $V_{ID}$, Others = $V_{IL}$/$V_{ID}$ | High-Z | 0x01 | A0 = VIL, A1 = VIL, A9 = VID, Others = VIL/VID | 0x0001 |
| READ DEVICE CODE | L | L | H | A0 = $V_{IH}$, A1 = $V_{IL}$, A9 = $V_{ID}$, Others = $V_{IL}$/$V_{IH}$ | High-Z | 0x51 (M29F200FT)<br>0x57 (M29F200FB)<br>0x23 (M29F400FT)<br>0xAB(M29F400FB)<br>0xD6 (M29F800FT)<br>0x58 (M29F800FB)<br>0xD2 (M29F160FT)<br>0xD8 (M29F160FB) | A0 = VIH, A1 = VIL, A9 = VID, Others = VIL/VIH | 0x2251 (M29F200FT)<br>0x2257 (M29F200FB)<br>0x2223 (M29F400FT)<br>0x22AB (M29F400FB)<br>0x22D6 (M29F800FT)<br>0x2258 (M29F800FB)<br>0x22D2 (M29F160FT)<br>0x22D8(M29F160FB) |

Note: 1. H = Logic level HIGH ($V_{IH}$); L = Logic level LOW ($V_{IL}$); X = HIGH or LOW.

## PROGRAM Command

The PROGRAM command can be used to program a value to one address at a time. The command requires four bus WRITE operations. The final WRITE operation latches the address and data, and starts the program/erase controller.

If the address falls in a protected block, then the PROGRAM command is ignored, the data remains unchanged. The status register is never read and no error condition is given.

During the PROGRAM operation, the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in READ CFI QUERY Command. READ operations during the PROGRAM operation will output the status register on the data I/Os. (See Registers.)

After the PROGRAM operation has completed, the memory returns to read mode, unless an error has occurred. When an error occurs, the memory continues to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

Note that the PROGRAM command cannot change a bit set at 0 back to 1. One of the ERASE commands must be used to set all the bits in a block, or in the whole device, from 0 to 1.

## UNLOCK BYPASS Command

The UNLOCK BYPASS command is used in conjunction with the UNLOCK BYPASS PROGRAM command to program the memory. When the access time to the device is long (as with some EPROM programmers), considerable time saving can be made by using these commands. Three WRITE operations are required to issue the UNLOCK BYPASS command.


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Once the UNLOCK BYPASS command has been issued, the memory will only accept the UNLOCK BYPASS PROGRAM command and the UNLOCK BYPASS RESET command. The memory can be read as though in read mode.

## UNLOCK BYPASS PROGRAM Command

The UNLOCK BYPASS PROGRAM command can be used to program one address in memory at a time. The command requires two WRITE operations, the final write operation latches the address and data, and starts the program/erase controller.

The PROGRAM operation using the UNLOCK BYPASS PROGRAM command behaves identically to the PROGRAM operation using the PROGRAM command. A protected block cannot be programmed; the operation cannot be aborted and the status register is read. Errors must be reset using the READ/RESET command, which leaves the device in unlock bypass mode. (See the PROGRAM command for details.)

## UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET command can be used to return to read/reset mode from unlock bypass mode. Two WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

## CHIP ERASE Command

The CHIP ERASE command can be used to erase the entire chip. Six WRITE operations are required to issue the CHIP ERASE command and start the program/erase controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected, the CHIP ERASE operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During an ERASE operation, the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in READ CFI QUERY Command. All READ operations during the CHIP ERASE operation will output the status register on the data I/Os. (See Registers for more details.)

After the CHIP ERASE operation has completed, the memory will return to read mode, unless an error has occurred. When an error occurs, the memory will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

The CHIP ERASE command sets all of the bits in unprotected blocks to 1. All previous data is lost.

## BLOCK ERASE Command

The BLOCK ERASE command can be used to erase a list of one or more blocks. Six WRITE operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth WRITE operation, using the address of the additional block. The BLOCK ERASE operation starts the program/erase controller about 50µs after the last WRITE operation. Once the program/erase controller starts, it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The status register can be read after the sixth WRITE operation. See Status Regis-


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ter for details on how to identify whether the program/erase controller has started the BLOCK ERASE operation.

If any selected blocks are protected, then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected, the BLOCK ERASE operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the BLOCK ERASE operation, the device will ignore all commands except the ERASE SUSPEND command. All READ operations during the BLOCK ERASE operation will output the status register on the data I/Os.

After the BLOCK ERASE operation has completed, the device will return to read mode, unless an error has occurred. When an error occurs, the device will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

The BLOCK ERASE command sets all of the bits in the unprotected selected blocks to 1. All previous data in the selected blocks is lost.

## ERASE SUSPEND Command

The ERASE SUSPEND command may be used to temporarily suspend a BLOCK ERASE operation and return the device to read mode. The command requires one WRITE operation.

The program/erase controller will suspend within the erase suspend latency time of the ERASE SUSPEND command being issued. Once the program/erase controller has stopped, the device will be set to read mode and the erase will be suspended. If the ERASE SUSPEND command is issued during the period when the device is waiting for an additional block (before the program/erase controller starts), then the erase is suspended immediately and will start immediately when the ERASE SUSPEND command is issued. It is not possible to select any further blocks to erase after the erase resume.

During erase suspend, it is possible to read and program cells in blocks that are not being erased; both READ and PROGRAM operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the PROGRAM command is ignored and the data remains unchanged. The status register is not read and no error condition is given. Reading from blocks that are being erased will output the status register.

It is also possible to issue the AUTO SELECT, READ CFI QUERY, and UNLOCK BYPASS commands during an erase suspend. The READ/RESET command must be issued to return the device to read array mode before the RESUME command will be accepted.

## ERASE RESUME Command

The ERASE RESUME command must be used to restart the program/erase controller from erase suspend. An erase can be suspended and resumed more than once.

## READ CFI QUERY Command

The READ CFI QUERY command reads data from the CFI. This command is valid when the device is in read array mode, or when the device is in auto select mode. One WRITE cycle is required to issue the READ CFI QUERY command. Once the command is issued, subsequent READ operations then read from the CFI. The READ/RESET command


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must be issued to return the device to the previous mode (read array or auto select mode). A second READ/RESET command would be needed if the device is to be placed in read array from auto select mode.

### 16-Bit Mode Commands

**Table 5: 16-Bit Mode Commands (BYTE# = HIGH)**

| Command | Length | WRITE Operations | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| READ/RESET | 1 | X | F0 | | | | | | | | | | |
| | 3 | 555 | AA | 2AA | 55 | X | F0 | | | | | | |
| AUTO SELECT | 3 | 555 | AA | 2AA | 55 | 555 | 90 | | | | | | |
| PROGRAM | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| UNLOCK BYPASS | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| UNLOCK BYPASS PROGRAM | 2 | X | A0 | PA | PD | | | | | | | | |
| UNLOCK BYPASS RESET | 2 | X | 90 | X | 00 | | | | | | | | |
| CHIP ERASE | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| BLOCK ERASE | 6+ | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | BA | 30 |
| ERASE SUSPEND | 1 | X | B0 | | | | | | | | | | |
| ERASE RESUME | 1 | X | 30 | | | | | | | | | | |
| READ CFI QUERY | 1 | 55 | 98 | | | | | | | | | | |

Notes:
1. X = "Don't Care;" PA = Program address; PD = Program data; BA = Any address in the block. All values in the table are in hexadecimal.
2. Command interface: Only uses A-1, A[10;0], and DQ[7;0] to verify the commands; A[19:11], DQ[14:8], and DQ15 are "Don't Care." DQ15/A-1 is A-1 when BYTE is LOW or DQ15 when BYTE is HIGH.
3. **Read/Reset:** After a READ/RESET command, read the memory as normal until another command is issued.
4. **Auto Select:** After an AUTO SELECT command, read manufacturer ID, device ID, or block protection status.
5. **Program, Unlock Bypass Program, Chip Erase, Block Erase:** After issuing these commands, read the status register until the program/erase controller completes and the device returns to read mode. Add additional blocks during a BLOCK ERASE command with additional bus WRITE operations until the timeout bit is set.
6. **Unlock Bypass:** After the UNLOCK BYPASS command, issue an UNLOCK BYPASS PROGRAM or UNLOCK BYPASS RESET command.
7. **Unlock Bypass Reset:** After the UNLOCK BYPASS RESET command, read the memory as normal until another command is issued.
8. **Erase Suspend:** After the ERASE SUSPEND command, read non-erasing blocks as normal. Issue AUTO SELECT and PROGRAM commands on non-erasing blocks as normal.
9. **Erase Resume:** After the ERASE RESUME command, the suspended ERASE operation resumes. Read the status register until the program/erase controller completes and the device returns to read mode.


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10. **CFI Query:** Command is valid when device is ready to read array data or when device is in auto select mode.

## 8-Bit Mode Commands

### Table 6: 8-Bit Mode Commands (BYTE# = LOW)

| Command | Length | WRITE Operations | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| READ/RESET | 1 | X | F0 | | | | | | | | | | |
| | 3 | AAA | AA | 555 | 55 | X | F0 | | | | | | |
| AUTO SELECT | 3 | AAA | AA | 555 | 55 | AAA | 90 | | | | | | |
| PROGRAM | 4 | AAA | AA | 555 | 55 | AAA | A0 | PA | PD | | | | |
| UNLOCK BYPASS | 3 | AAA | AA | 555 | 55 | AAA | 20 | | | | | | |
| UNLOCK BYPASS PROGRAM | 2 | X | A0 | PA | PD | | | | | | | | |
| UNLOCK BYPASS RESET | 2 | X | 90 | X | 00 | | | | | | | | |
| CHIP ERASE | 6 | AAA | AA | 555 | 55 | AAA | 80 | AAA | AA | 555 | 55 | AAA | 10 |
| BLOCK ERASE | 6+ | AAA | AA | 555 | 55 | AAA | 80 | AAA | AA | 555 | 55 | BA | 30 |
| ERASE SUSPEND | 1 | X | B0 | | | | | | | | | | |
| ERASE RESUME | 1 | X | 30 | | | | | | | | | | |
| READ CFI QUERY | 1 | AA | 98 | | | | | | | | | | |

Notes:
1. X = "Don't Care;" PA = Program address; PD = Program data; BA = Any address in the block. All values in the table are in hexadecimal.
2. Command interface: Only uses A-1, A[10;0], and DQ[7;0] to verify the commands; A[19:11], DQ[14:8], and DQ15 are "Don't Care." DQ15/A-1 is A-1 when BYTE is LOW or DQ15 when BYTE is HIGH.
3. **Read/Reset:** After a READ/RESET command, read the memory as normal until another command is issued.
4. **Auto Select:** After an AUTO SELECT command, read manufacturer ID, device ID, or block protection status.
5. **Program, Unlock Bypass Program, Chip Erase, Block Erase:** After issuing these commands, read the status register until the program/erase controller completes and the device returns to read mode. Add additional blocks during a BLOCK ERASE command with additional bus WRITE operations until the timeout bit is set.
6. **Unlock Bypass:** After the UNLOCK BYPASS command, issue an UNLOCK BYPASS PROGRAM or UNLOCK BYPASS RESET command.
7. **Unlock Bypass Reset:** After the UNLOCK BYPASS RESET command, read the memory as normal until another command is issued.
8. **Erase Suspend:** After the ERASE SUSPEND command, read non-erasing blocks as normal. Issue AUTO SELECT and PROGRAM commands on non-erasing blocks as normal.
9. **Erase Resume:** After the ERASE RESUME command, the suspended ERASE operation resumes. Read the status register until the program/erase controller completes and the device returns to read mode.
10. **CFI Query:** Command is valid when device is ready to read array data or when device is in auto select mode.


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# Block Protection Operations

Block protection can be used to prevent any operation from modifying the data stored in the Flash memory. Each Block can be protected individually. Once protected, Program and Erase operations on the block fail to change the data. Block protection status of the device is read using the AUTO SELECT command.

Two techniques for controlling block protection are explained here: Programmer technique and In-System technique.

**Note:** A third technique for controlling block protection, Temporary Unprotection, is described in the Signal Descriptions table, RP pin (Reset/Block Temporary Unprotection).

Unlike the Command Interface of the Program/Erase Controller, the techniques for protecting and unprotecting blocks could change between different Flash memory suppliers.

**Table 7: Block and Chip Protection Signal Settings**

| Signals | Block Protect | Chip Unprotect | Verify Block Protection | Verify Block Unprotect |
|---|---|---|---|---|
| CE# | L | $V_{ID}$ | L | L |
| OE# | $V_{ID}$ | $V_{ID}$ | L | L |
| WE# | L pulse | L pulse | H | H |
| **Address Input, 8-Bit and 16-Bit** | | | | |
| A[MAX:16] | Block base address | X | Block base address | Block base address |
| A15 | | H | | |
| A14 | | X | | |
| A13 | | X | | |
| A12 | | H | | |
| A11 | X | X | X | X |
| A10 | X | X | X | X |
| A9 | $V_{ID}$ | $V_{ID}$ | $V_{ID}$ | $V_{ID}$ |
| A8 | X | X | X | X |
| A7 | X | X | X | X |
| A6 | X | X | L | H |
| A5 | X | X | X | X |
| A4 | X | X | X | X |
| A3 | X | X | X | X |
| A2 | X | X | X | X |
| A1 | X | X | H | H |
| A0 | X | X | L | L |
| **Data I/O, 8-Bit and 16-Bit** | | | | |


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**Table 7: Block and Chip Protection Signal Settings (Continued)**

| Signals | Block Protect | Chip Unprotect | Verify Block Protection | Verify Block Unprotect |
|---|---|---|---|---|
| DQ[15]/A-1, and DQ[14:0] | X | X | Pass = XX01h | Retry = XX01h |
| | X | X | Retry = XX00h | Pass = XX00h |

Note: 1. H = Logic level HIGH ($V_{IH}$); L = Logic level LOW ($V_{IL}$); X = HIGH or LOW.

## Programmer Technique

The Programmer technique uses high ($V_{ID}$) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a block, follow the Programmer Equipment Block Protect flowchart. During the Block Protect algorithm, the A19-A12 Address Inputs indicate the address of the block to be protected. The block will be correctly protected only if A19-A12 remain valid and stable, and if Chip Enable is kept Low, $V_{IL}$, all along the Protect and Verify phases.

The Chip Unprotect algorithm is used to unprotect all the memory blocks at the same time. This algorithm can only be used if all of the blocks are protected first. To unprotect the chip follow the Programmer Equipment Chip Unprotect flowchart and the Programmer Technique Block Protection table, which give a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

**Figure 17: Block Protect Flowchart – Programmer Equipment**

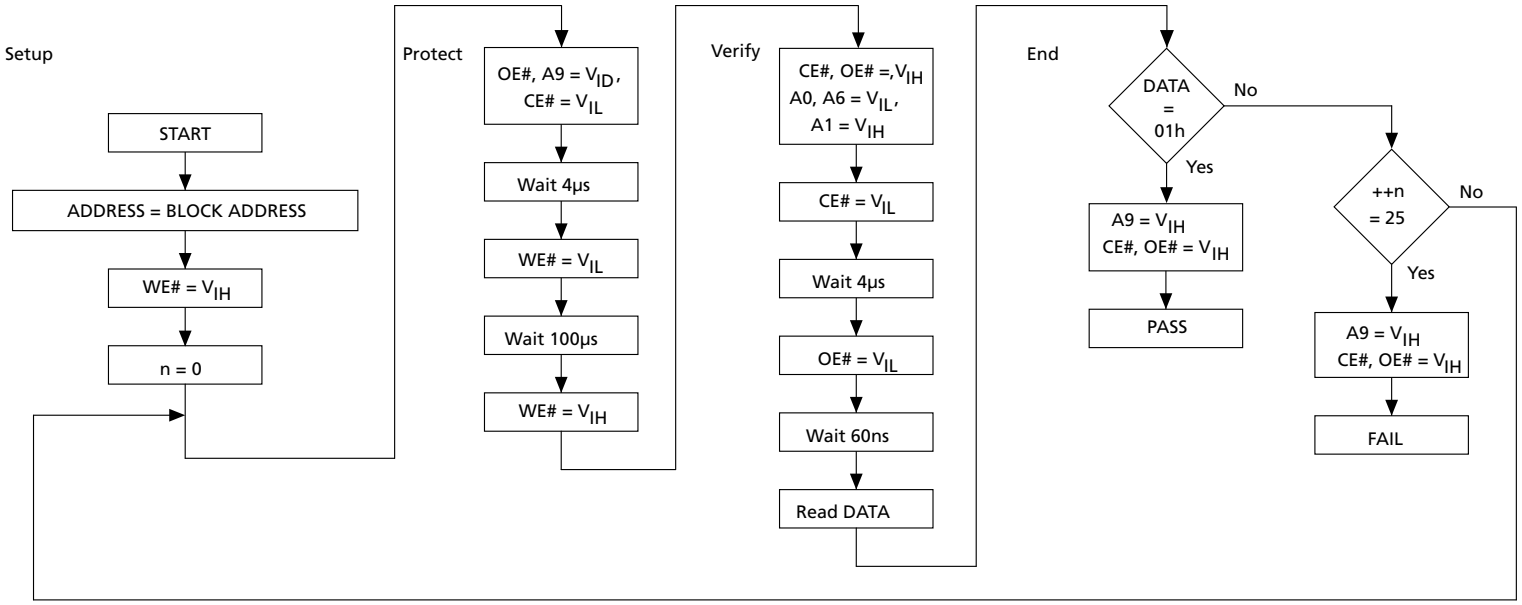



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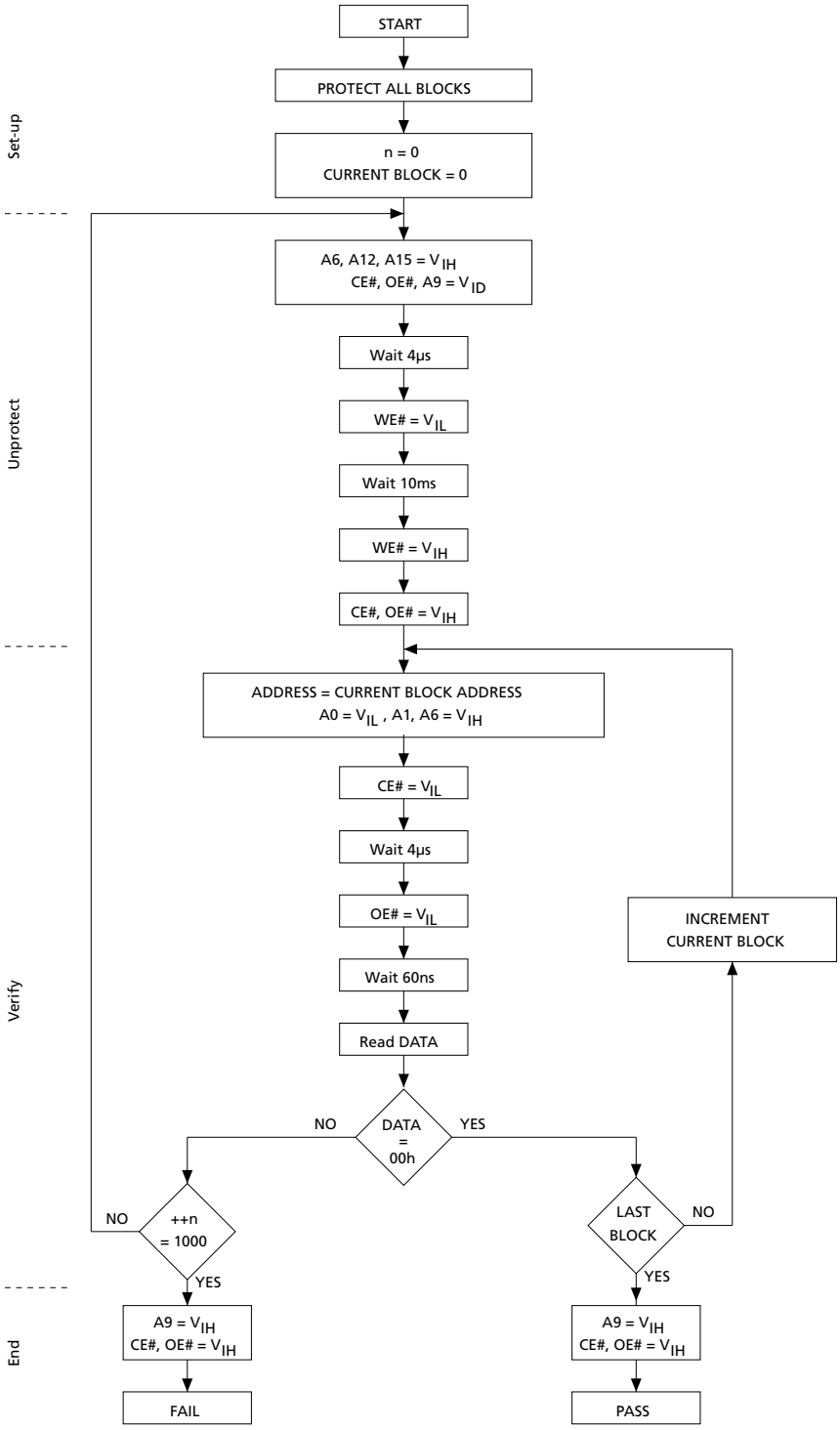
**Figure 18: Chip Unprotect Flowchart – Programmer Equipment**





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Notes:
1. Address Inputs A[9:12] give the address of the block that is to be protected. It is imperative that they remain stable during the operation.
2. During the protect and verify phases of the algorithm, CE# must be kept LOW.

## In-System Technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, RP. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the Flash memory has been fitted to the system.

To protect a block follow the In-System Equipment Block Protect flowchart . To unprotect the whole chip it is necessary to protect all of the blocks first, then all the blocks can be unprotected at the same time. To unprotect the chip follow the In-System Equipment Chip Unprotect flowchart.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

**Figure 19: Block Protect Flowchart – In-System Equipment**

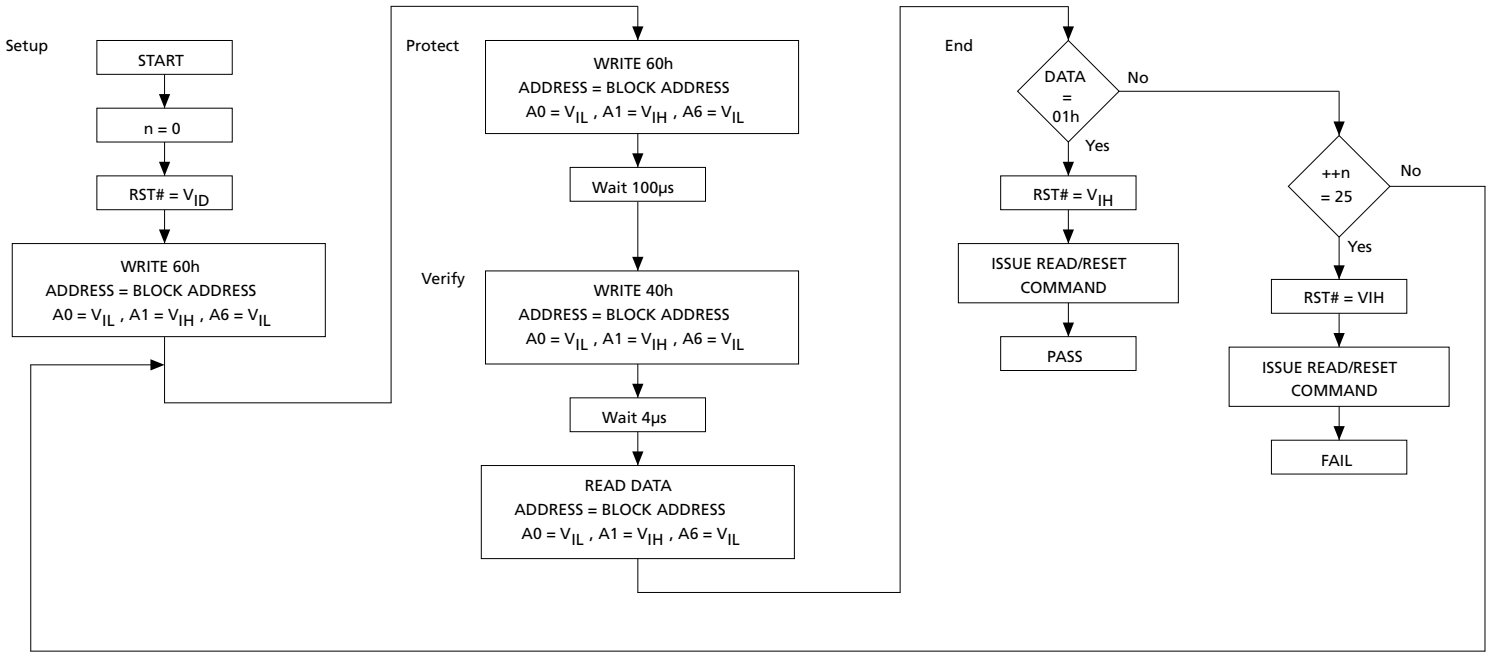



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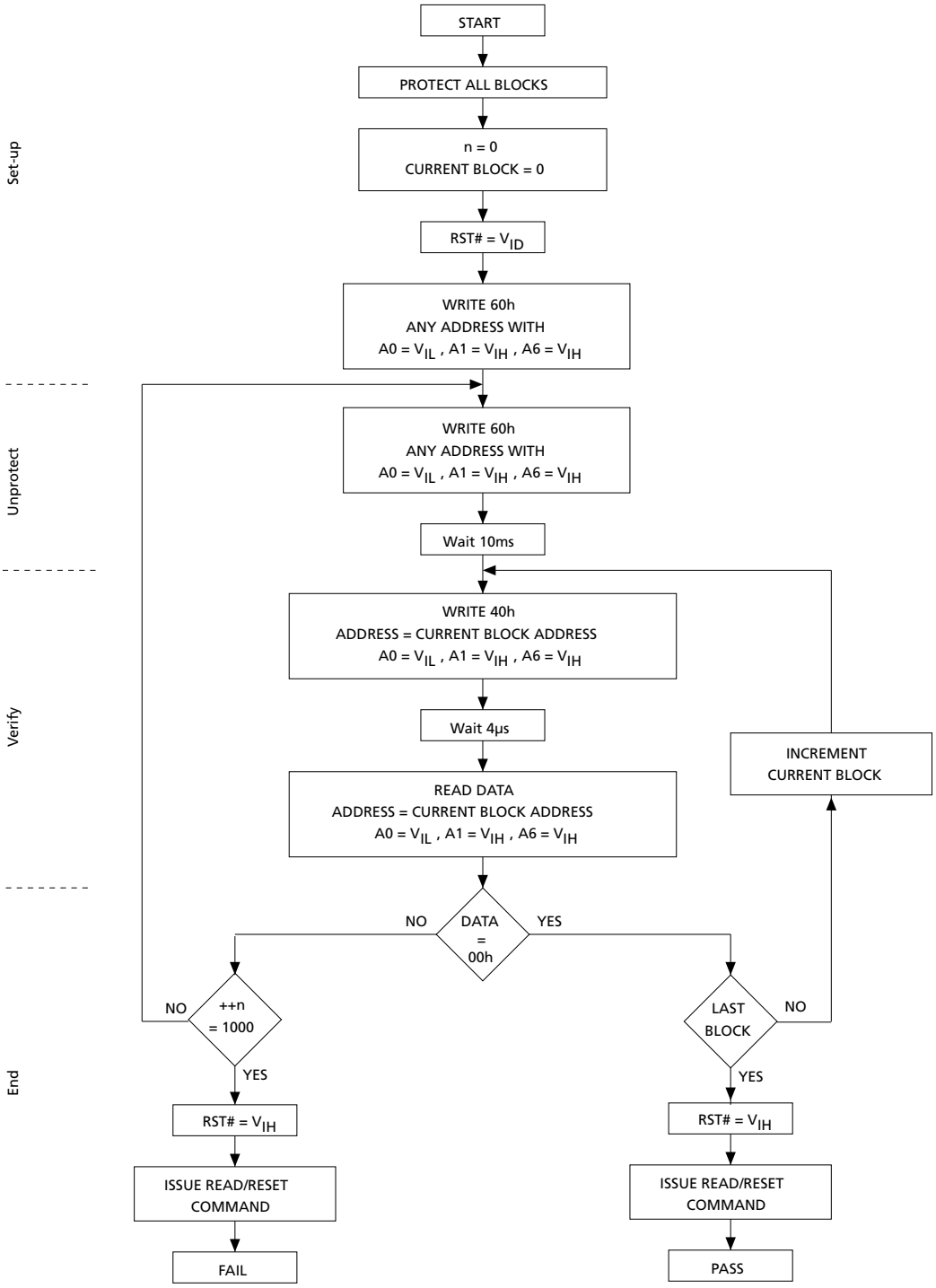
**Figure 20: Chip Protection Flowchart – In-System Equipment**





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## Status Register

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

**Table 8: Status Register Bits**

| Operation | Address | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 | RB# |
|---|---|---|---|---|---|---|---|
| Program | Any Address | DQ7# | Toggle | 0 | – | – | 0 |
| Program During Erase Suspend | Any Address | DQ7# | Toggle | 0 | – | – | 0 |
| Program Error | Any Address | DQ7# | Toggle | 1 | – | – | 0 |
| Chip Erase | Any Address | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Block Erase before time-out | Erasing Block | 0 | Toggle | 0 | 0 | Toggle | 0 |
| | Non-Erasing Block | 0 | Toggle | 0 | 0 | No Toggle | 0 |
| Block Erase | Erasing Block | 0 | Toggle | 0 | 1 | Toggle | 0 |
| | Non-Erasing Block | 0 | Toggle | 0 | 1 | No Toggle | 0 |
| Erase Suspend | Erasing Block | 1 | No Toggle | 0 | – | Toggle | 1 |
| | Non-Erasing Block | Data read as normal | | | | | 1 |
| Erase Error | Good Block Address | 0 | Toggle | 1 | 1 | No Toggle | 0 |
| | Faulty Block Address | 0 | Toggle | 1 | 1 | Toggle | 0 |

Note: 1. Unspecified data bits should be ignored.

## Data Polling Bit

The Data Polling Bit (DQ7) can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

The Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.


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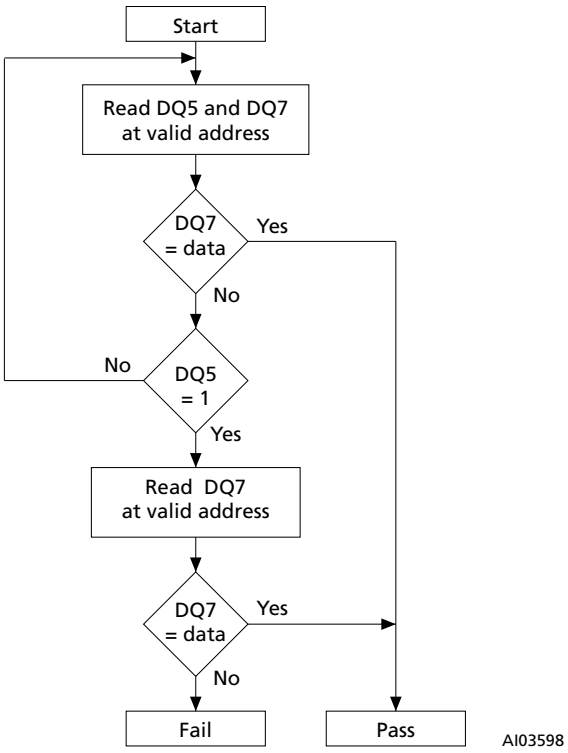
**Figure 21: Data Polling Flowchart**




## Toggle Bit

The Toggle Bit (DQ6) can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 1µs.

The Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.


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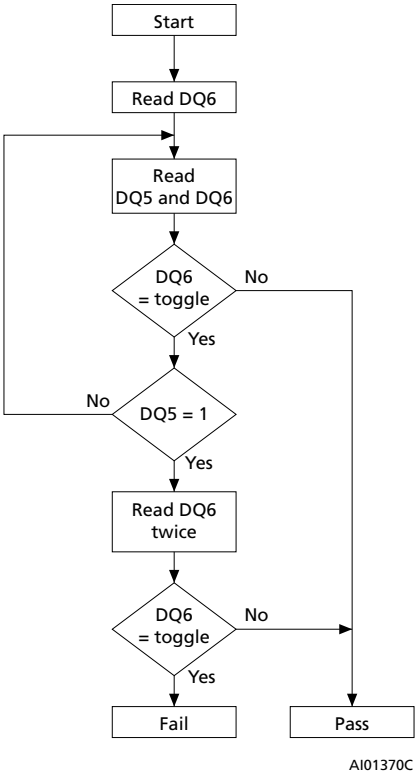
**Figure 22: Data Toggle Flowchart**




## Error Bit

The Error Bit (DQ5) can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to ’1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’

## Erase Timer Bit

The Erase Timer Bit (DQ3) can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to ’1’. Before the Program/Erase Controller starts the Erase Timer Bit is set to ’0’ and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.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## Alternative Toggle Bit

The Alternative Toggle Bit (DQ2) can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.



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# Common Flash Interface (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Addresses used to retrieve the data are shown in the following tables:

The CFI data structure also contains a security area where a 64-bit unique security number is written. This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by Micron. Issue a Read command to return to Read mode.

**Table 9: Query Structure Overview**

| Address | | Sub-section Name | Description |
|---|---|---|---|
| x16 | x8 | | |
| 10h | 20h | CFI Query Identification String | Command set ID and algorithm data offset |
| 1Bh | 36h | System Interface Information | Device timing & voltage information |
| 27h | 4Eh | Device Geometry Definition | Flash device layout |
| 40h | 80h | Primary Algorithm-specific Extended Query table | Additional information specific to the Primary Algorithm (optional) |
| 61h | C2h | Security Code Area | 64 bit unique device number |

Note: 1. Query data are always presented on the lowest order data outputs.

**Table 10: CFI Query Identification String**

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 10h | 20h | 0051h | | "Q" |
| 11h | 22h | 0052h | Query Unique ASCII String "QRY" | "R" |
| 12h | 24h | 0059h | | "Y" |
| 13h | 26h | 0002h | Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm | AMD Compatible |
| 14h | 28h | 0000h | | |
| 15h | 2Ah | 0040h | Address for Primary Algorithm extended Query table (see the Device Geometry table.) | P = 40h |
| 16h | 2Ch | 0000h | | |
| 17h | 2Eh | 0000h | Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported | NA |
| 18h | 30h | 0000h | | |
| 19h | 32h | 0000h | Address for Alternate Algorithm extended Query table | NA |
| 1Ah | 34h | 0000h | | |

Note: 1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are '0'.


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### Table 11: CFI Query System Interface Information

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 1Bh | 36h | 0045h | $V_{CC}$ Logic Supply Minimum Program/Erase voltage<br>bit 7 to 4 BCD value in volts<br>bit 3 to 0 BCD value in 100 mV | 4.5V |
| 1Ch | 38h | 0055h | $V_{CC}$ Logic Supply Maximum Program/Erase voltage<br>bit 7 to 4 BCD value in volts<br>bit 3 to 0 BCD value in 100 mV | 5.5V |
| 1Dh | 3Ah | 0000h | $V_{PP}$ [Programming] Supply Minimum Program/Erase voltage | NA |
| 1Eh | 3Ch | 0000h | $V_{PP}$ [Programming] Supply Maximum Program/Erase voltage | NA |
| 1Fh | 3Eh | 0003h | Typical timeout per single Byte/Word program = $2^n$ µs | 8µs |
| 20h | 40h | 0000h | Typical timeout for minimum size write buffer program = $2^n$ µs | NA |
| 21h | 42h | 000Ah | Typical timeout per individual block erase = $2^n$ ms | 1 s |
| 22h | 44h | 0000h | Typical timeout for full chip erase = $2^n$ ms | NA |
| 23h | 46h | 0004h | Maximum timeout for Byte/Word program = $2^n$ times typical | 256µs |
| 24h | 48h | 0000h | Maximum timeout for write buffer program = $2^n$ times typical | NA |
| 25h | 4Ah | 0003h | Maximum timeout per individual block erase = $2^n$ times typical | 8 s |
| 26h | 4Ch | 0000h | Maximum timeout for chip erase = $2^n$ times typical | NA |

### Table 12: Device Geometry Definition

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 27h | 4Eh | 0015h | Device Size = $2^n$ in number of Bytes | 2MB |
| | | 0014h | | 1MB |
| | | 0013h | | 512KB |
| | | 0012h | | 256KB |
| 28h<br>29h | 50h<br>52h | 0002h<br>0000h | Flash Device Interface Code description | x8, x16 Async. |
| 2Ah<br>2Bh | 54h<br>56h | 0000h<br>0000h | Maximum number of Bytes in multi-Byte program or page = $2^n$ | NA |
| 2Ch | 58h | 0004h | Number of Erase Block Regions within the device.<br>It specifies the number of regions within the device containing contiguous Erase Blocks of the same size. | 4 |
| 2Dh<br>2Eh | 5Ah<br>5Ch | 0000h<br>0000h | Region 1 Information<br>Number of identical size erase block = 0000h+1 | 1 |
| 2Fh<br>30h | 5Eh<br>60h | 0040h<br>0000h | Region 1 Information<br>Block size in Region 1 = 0040h * 256 Byte | 16KB |
| 31h<br>32h | 62h<br>64h | 0001h<br>0000h | Region 2 Information<br>Number of identical size erase block = 0001h+1 | 2 |
| 33h<br>34h | 66h<br>68h | 0020h<br>0000h | Region 2 Information<br>Block size in Region 2 = 0020h * 256 Byte | 8KB |


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**Table 12: Device Geometry Definition (Continued)**

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 35h<br>36h | 6Ah<br>6Ch | 0000h<br>0000h | Region 3 Information<br>Number of identical size erase block = 0000h+1 | 1 |
| 37h<br>38h | 6Eh<br>70h | 0080h<br>0000h | Region 3 Information<br>Block size in Region 3 = 0080h * 256 Byte | 32KB |
| 39h<br>3Ah | 72h<br>74h | 001Eh<br>0000h | Region 4 Information (2 MByte)<br>Number of identical-size erase block = 001Eh+1 | 31 |
| 39h<br>3Ah | 72h<br>74h | 000Eh<br>0000h | Region 4 Information (1 MByte)<br>Number of identical-size erase block = 000Eh+1 | 15 |
| 39h<br>3Ah | 72h<br>74h | 0006h<br>0000h | Region 4 Information (512 KByte)<br>Number of identical-size erase block = 0006h+1 | 7 |
| 39h<br>3Ah | 72h<br>74h | 0002h<br>0000h | Region 4 Information (256 KByte)<br>Number of identical-size erase block = 0002h+1 | 3 |
| 3Bh<br>3Ch | 76h<br>78h | 0000h<br>0001h | Region 4 Information<br>Block size in Region 4 = 0100h * 256 Byte | 64KB |

**Table 13: Primary Algorithm-Specific Extended Query Table**

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 40h | 80h | 0050h | Primary Algorithm extended Query table unique ASCII string “PRI” | "P" |
| 41h | 82h | 0052h | | "R" |
| 42h | 84h | 0049h | | "I" |
| 43h | 86h | 0031h | Major version number, ASCII | "1" |
| 44h | 88h | 0030h | Minor version number, ASCII | "0" |
| 45h | 8Ah | 0000h | Address Sensitive Unlock (bits 1 to 0)<br>00 = required, 01= not required<br>Silicon Revision Number (bits 7 to 2) | Yes |
| 46h | 8Ch | 0002h | Erase Suspend<br>00 = not supported, 01 = Read only, 02 = Read and Write | 2 |
| 47h | 8Eh | 0001h | Block Protection<br>00 = not supported, x = number of blocks in per group | 1 |
| 48h | 90h | 0001h | Temporary Block Unprotect<br>00 = not supported, 01 = supported | Yes |
| 49h | 92h | 0002h<br>0004h<br><br>0008h<br><br>0160h | Block Protect /Unprotect<br>02 = M29F200<br>04 = M29F400<br>08 = M29F800<br>10 = M29F160 | 2<br>4<br>8<br>16 |
| 4Ah | 94h | 0000h | Simultaneous Operations, 00 = not supported | No |
| 4Bh | 96h | 0000h | Burst Mode, 00 = not supported, 01 = supported | No |


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**Table 13: Primary Algorithm-Specific Extended Query Table (Continued)**

| Address | | Data | Description | Value |
|---|---|---|---|---|
| x16 | x8 | | | |
| 4Ch | 98h | 0000h | Page Mode, 00 = not supported, 01 = 4 page Word, 02 = 8 page Word | No |

**Table 14: Security Code Area**

| Address | | Data | Description |
|---|---|---|---|
| x16 | x8 | | |
| 61h | C3h, C2h | XXXX | 64 bit: unique device number |
| 62h | C5h, C4h | XXXX | |
| 63h | C7h, C6h | XXXX | |
| 64h | C9h, C8h | XXXX | |



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# Maximum Ratings and Operating Conditions

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied.

**Table 15: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –50 | 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 | 150 | °C |
| $V_{IO}$ | Input or Output Voltage | –0.6 | $V_{CC}$ +0.6 | V |
| $V_{CC}$ | Supply Voltage | –0.6 | 6 | V |
| $V_{ID}$ | Identification Voltage | –0.6 | 13.5 | V |

Notes:
1. Input or Output Voltage parameter: Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
2. Input or Output Voltage parameter: Maximum voltage may overshoot to $V_{CC}$ +2V during transition and for less than 20ns during transitions.

The parameters in the tables that follow, are derived from tests performed under the Measurement Conditions shown here. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 16: Operating and AC Measurement Conditions**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| $V_{CC}$ Supply Voltage | 4.5 | 5.5 | V |
| Ambient Operating Temperature | –40 | 125 | °C |
| Load Capacitance ($C_L$) | 30 | 30 | pF |
| Input Rise and Fall Times | — | 5 | ns |
| Input Pulse Voltages | 0 to $V_{CC}$ | 0 to $V_{CC}$ | V |
| Input and Output Timing Reference Voltages | $V_{CC}/2$ | $V_{CC}/2$ | V |

**Figure 23: AC Measurement I/O Waveform**

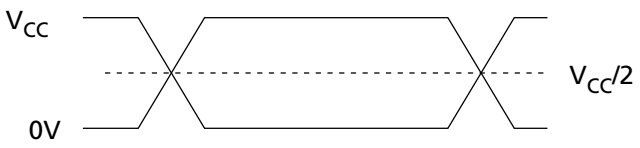


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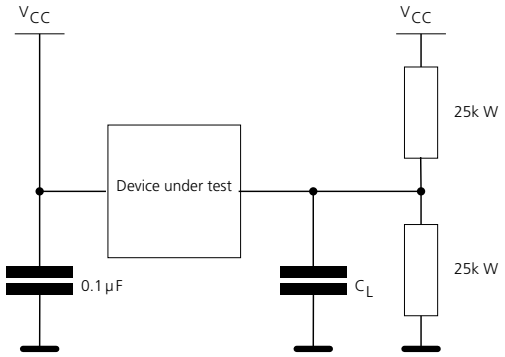
**Figure 24: AC Measurement Load Circuit**




$C_L$ includes JIG capacitance

**Table 17: Device Capacitance**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

Note: 1. Sampled only, not 100% tested.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# DC Electrical Specifications

### Table 18: DC Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | — | — | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | — | — | ±1 | µA |
| $I_{CC1}$ | Supply Current (Read) | CE# = $V_{IL}$, OE# = $V_{IH}$, f = 6MHz | — | 7 | 20 | mA |
| $I_{CC2}$ | Supply Current (Standby) | CE# = $V_{CC}$ ±0.2V, RP# = $V_{CC}$ ±0.2V | — | 60 | 120 | µA |
| $I_{CC3}$ | Supply Current (Program/Erase) | Program/Erase Controller active | — | — | 30 | mA |
| $V_{IL}$ | Input Low Voltage | – | –0.5 | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | – | $0.7V_{CC}$ | — | $V_{CC}$ +0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1.8mA | — | — | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –100µA | $V_{CC}$ –0.4 | — | — | V |
| $V_{ID}$ | Identification Voltage | | 11.5 | — | 12.5 | V |
| $I_{ID}$ | Identification Current | A9 = $V_{ID}$ | — | — | 100 | µA |
| $V_{LKO}$ | Program/Erase Lockout Supply Voltage | – | 1.8 | — | 2.3 | V |

Note: 1. Supply Current (Program/Erase) parameter: Sampled only, not 100% tested.


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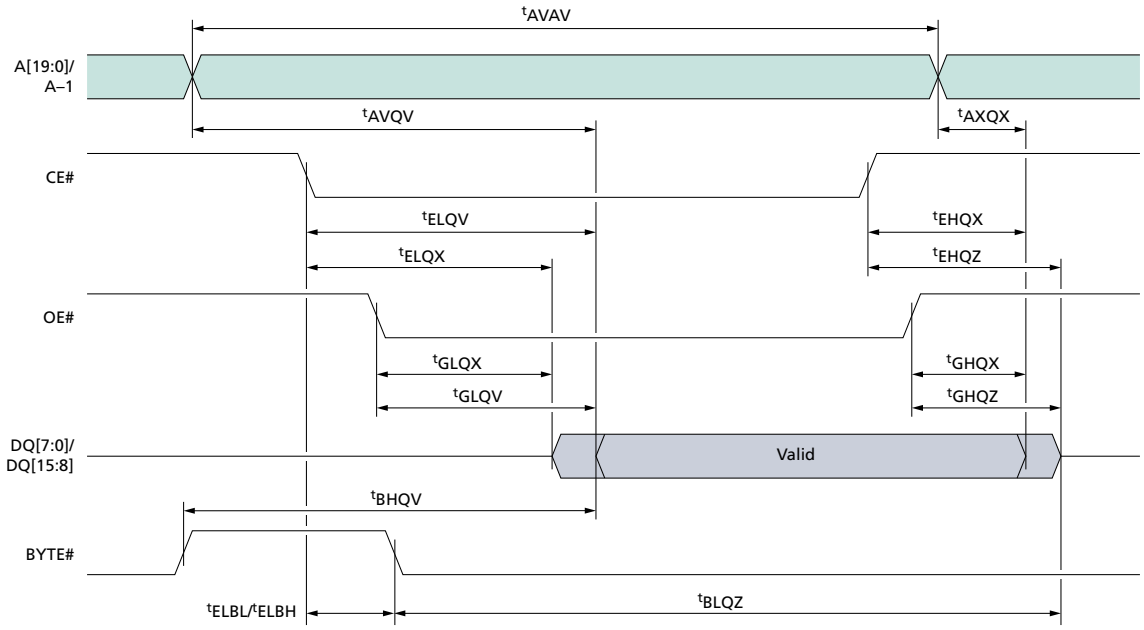
# AC Read Characteristics

### Figure 25: Read Mode AC Waveforms




### Table 19: Read AC Characteristics

| Symbol | Alt | Parameter | Test Condition | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{RC}$ | Address Valid to Next Address Valid | CE# = $V_{IL}$, OE# = $V_{IL}$ | Min | 55 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | CE# = $V_{IL}$, OE# = $V_{IL}$ | Max | 55 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | Chip Enable Low to Output Transition | OE# = $V_{IL}$ | Min | 0 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | OE# = $V_{IL}$ | Max | 55 | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable Low to Output Transition | CE# = $V_{IL}$ | Min | 0 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | CE# = $V_{IL}$ | Max | 20 | ns |
| $t_{EHQZ}$ | $t_{HZ}$ | Chip Enable High to Output Hi-Z | OE# = $V_{IL}$ | Max | 15 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable High to Output Hi-Z | CE# = $V_{IL}$ | Max | 15 | ns |
| $t_{EHQX}$ $t_{GHQX}$ $t_{AXQX}$ | $t_{OH}$ | Chip Enable, Output Enable or Address Transition to Output Transition | – | Min | 0 | ns |


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**Table 19: Read AC Characteristics (Continued)**

| Symbol | Alt | Parameter | Test Condition | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|---|
| $t_{ELBL}$ $t_{ELBH}$ | $t_{ELFL}$ $t_{ELFH}$ | Chip Enable to BYTE# Low or High | – | Max | 3 | ns |
| $t_{BLQZ}$ | $t_{FLQZ}$ | BYTE# Low to Output Hi-Z | – | Max | 15 | ns |
| $t_{BHQV}$ | $t_{FHQV}$ | BYTE# High to Output Valid | – | Max | 20 | ns |

Note: 1. $t_{ELQX}$ $t_{GLQX}$ $t_{EHQZ}$ and $t_{GHQZ}$ parameters: Sampled only, not 100% tested.


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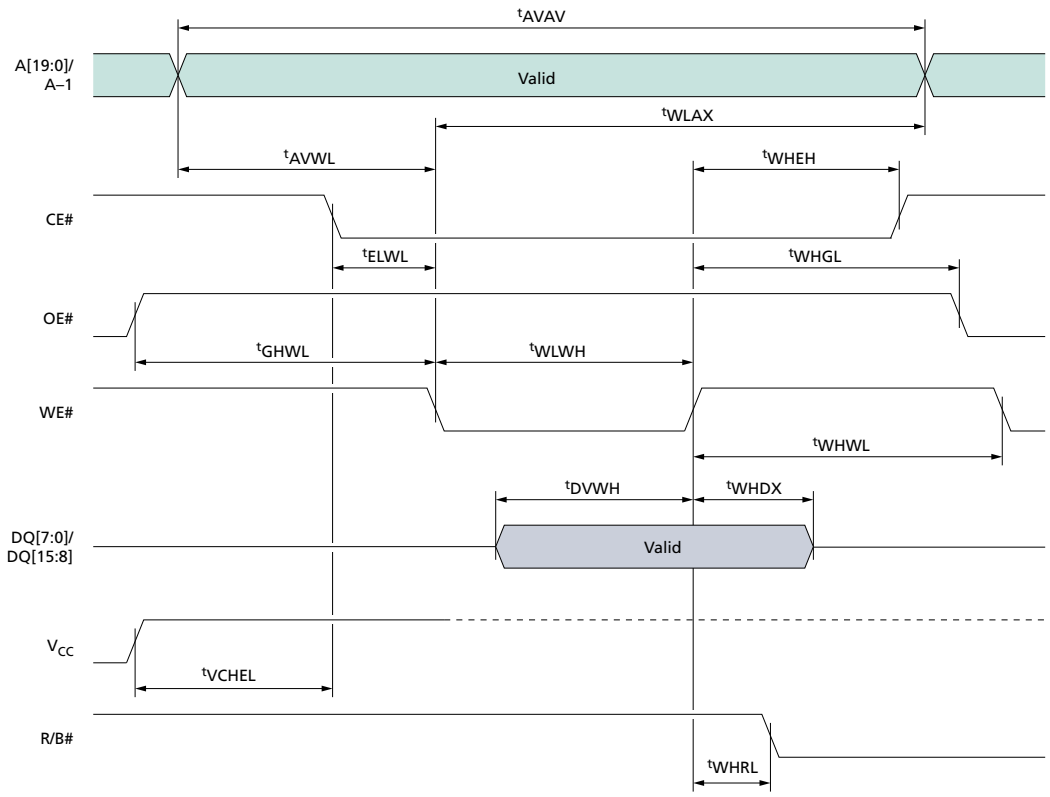
# AC Write Characteristics

### Figure 26: Write AC Waveforms, Write Enable Controlled




### Table 20: Write AC Characteristics, Write Enable Controlled

| Symbol | Alternate | Parameter | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | Min | 55 | ns |
| $t_{ELWL}$ | $t_{CS}$ | Chip Enable Low to Write Enable Low | Min | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Enable Low to Write Enable High | Min | 30 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Input Valid to Write Enable High | Min | 20 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Write Enable High to Input Transition | Min | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | Write Enable High to Chip Enable High | Min | 0 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Enable High to Write Enable Low | Min | 15 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Valid to Write Enable Low | Min | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Write Enable Low to Address Transition | Min | 30 | ns |
| $t_{GHWL}$ | | Output Enable High to Write Enable Low | Min | 0 | ns |
| $t_{WHGL}$ | $t_{OEH}$ | Write Enable High to Output Enable Low | Min | 0 | ns |
| $t_{WHRL}$ | $t_{BUSY}$ | Program/Erase Valid to RB# Low | Max | 20 | ns |


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**Table 20: Write AC Characteristics, Write Enable Controlled (Continued)**

| Symbol | Alternate | Parameter | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|
| $t_{VCHEL}$ | $t_{VCS}$ | $V_{CC}$ High to Chip Enable Low | Min | 50 | µs |

Note: 1. $t_{WHRL}$ parameter: Sampled only, not 100% tested.

**Figure 27: Write AC Waveforms, Chip Enable Controlled**

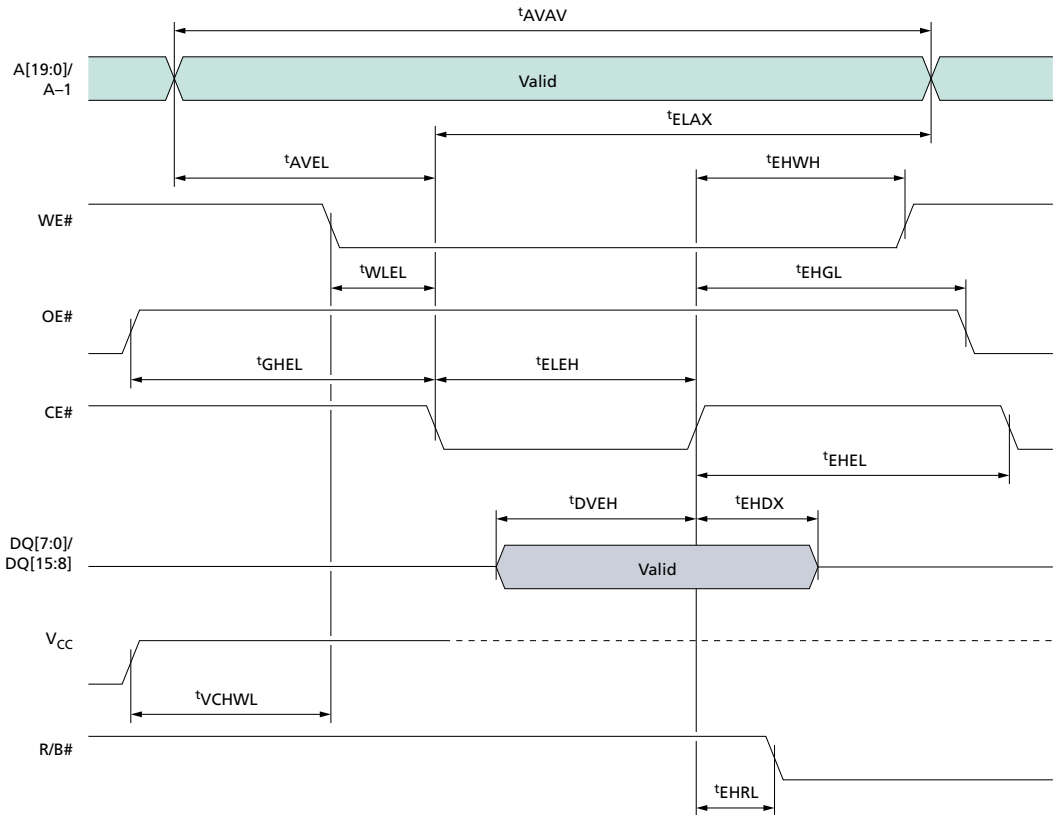


**Table 21: Write AC Characteristics, Chip Enable Controlled**

| Symbol | Alt | Parameter | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | Min | 55 | ns |
| $t_{WLEL}$ | $t_{WS}$ | Write Enable Low to Chip Enable Low | Min | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | Chip Enable Low to Chip Enable High | Min | 30 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Input Valid to Chip Enable High | Min | 20 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Chip Enable High to Input Transition | Min | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | Chip Enable High to Write Enable High | Min | 0 | ns |


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**Table 21: Write AC Characteristics, Chip Enable Controlled (Continued)**

| Symbol | Alt | Parameter | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|
| $t_{EHEL}$ | $t_{CPH}$ | Chip Enable High to Chip Enable Low | Min | 15 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | Min | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Chip Enable Low to Address Transition | Min | 30 | ns |
| $t_{GHEL}$ | | Output Enable High Chip Enable Low | Min | 0 | ns |
| $t_{EHGL}$ | $t_{OEH}$ | Chip Enable High to Output Enable Low | Min | 0 | ns |
| $t_{EHRL}$ | $t_{BUSY}$ | Program/Erase Valid to RB# Low | Max | 20 | ns |
| $t_{VCHWL}$ | $t_{VCS}$ | $V_{CC}$ High to Write Enable Low | Min | 50 | µs |

Note: 1. $t_{EHRL}$ parameter: Sampled only, not 100% tested.

# Reset Specifications

**Figure 28: Reset/Block Temporary Unprotect AC Waveforms**

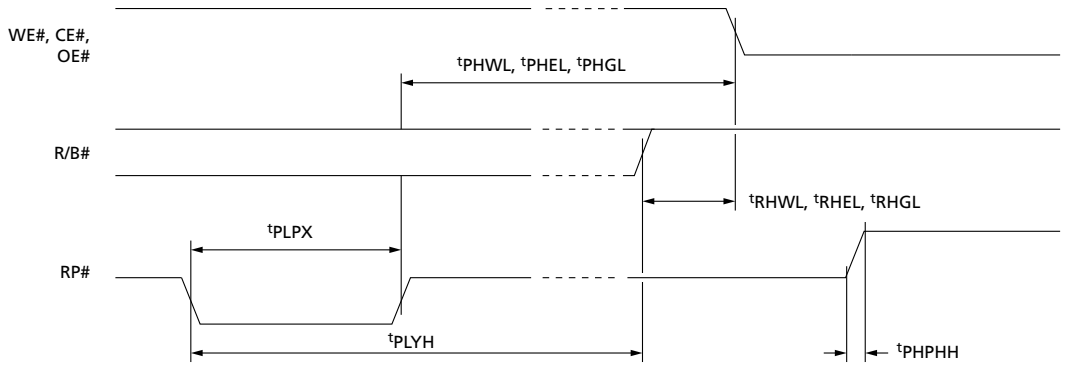


**Table 22: Reset/Block Temporary Unprotect AC Characteristics**

| Symbol | Alt | Parameter | M29F160F 55/5A | | Unit |
|---|---|---|---|---|---|
| $t_{PHWL}$ $t_{PHEL}$ $t_{PHGL}$ | $t_{RH}$ | RP# High to Write Enable Low, Chip Enable Low, Output Enable Low | Min | 50 | ns |
| $t_{RHWL}$ $t_{RHEL}$ $t_{RHGL}$ | $t_{RB}$ | RB# High to Write Enable Low, Chip Enable Low, Output Enable Low | Min | 0 | ns |
| $t_{PLPX}$ | $t_{RP}$ | RP# Pulse Width | Min | 500 | ns |
| $t_{PLYH}$ | $t_{READY}$ | RP# Low to Read Mode | Max | 10 | µs |
| $t_{PHPHH}$ | $t_{VIDR}$ | RP# Rise Time to $V_{ID}$ | Min | 500 | ns |

Note: 1. $t_{PHWL}$ $t_{PHGL}$ $t_{RHWL}$ $t_{RHEL}$ $t_{RHGL}$ $t_{PLYH}$ and $t_{PHPHH}$ parameters: Sampled only, not 100% tested.


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# PROGRAM/ERASE Characteristics

**Table 23: Program/Erase Characteristics**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Chip erase | M29F160F | — | 25 | 120 | s |
| | M29F800F | | 12 | 60 | |
| | M29F400F | | 6 | 30 | |
| | M29F200F | | 3 | 15 | |
| Block erase (64KB) | | — | 0.8 | 6 | s |
| Erase suspend latency time | | — | 20 | 25 | µs |
| Program (byte or word) | | — | 11 | 200 | µs |
| Chip program (byte-by-byte) | M29F160F | — | 24 | 120 | s |
| | M29F800F | | 12 | 60 | |
| | M29F400F | | 6 | 30 | |
| | M29F200F | | 4 | 16 | |
| Chip program (word-by-word) | M29F160F | — | 12 | 60 | s |
| | M29F800F | | 6 | 30 | |
| | M29F400F | | 3 | 15 | |
| | M29F200F | | 2 | 8 | |
| PROGRAM/ERASE cycles (per block) | | 100,000 | — | — | cycles |
| Data retention | | 20 | — | — | years |

Notes:
1. Typical values are measured at room temperature and nominal voltages; typical and maximum values are samples, not 100% tested.
2. Chip erase, program, and chip program parameters: Maximum value measured at worst case conditions for both temperature and $V_{CC}$ after 100,000 PROGRAM/ERASE cycles.
3. Block erase and erase suspend latency parameter: Maximum value measured at worst-case conditions for both temperature and $V_{CC}$.


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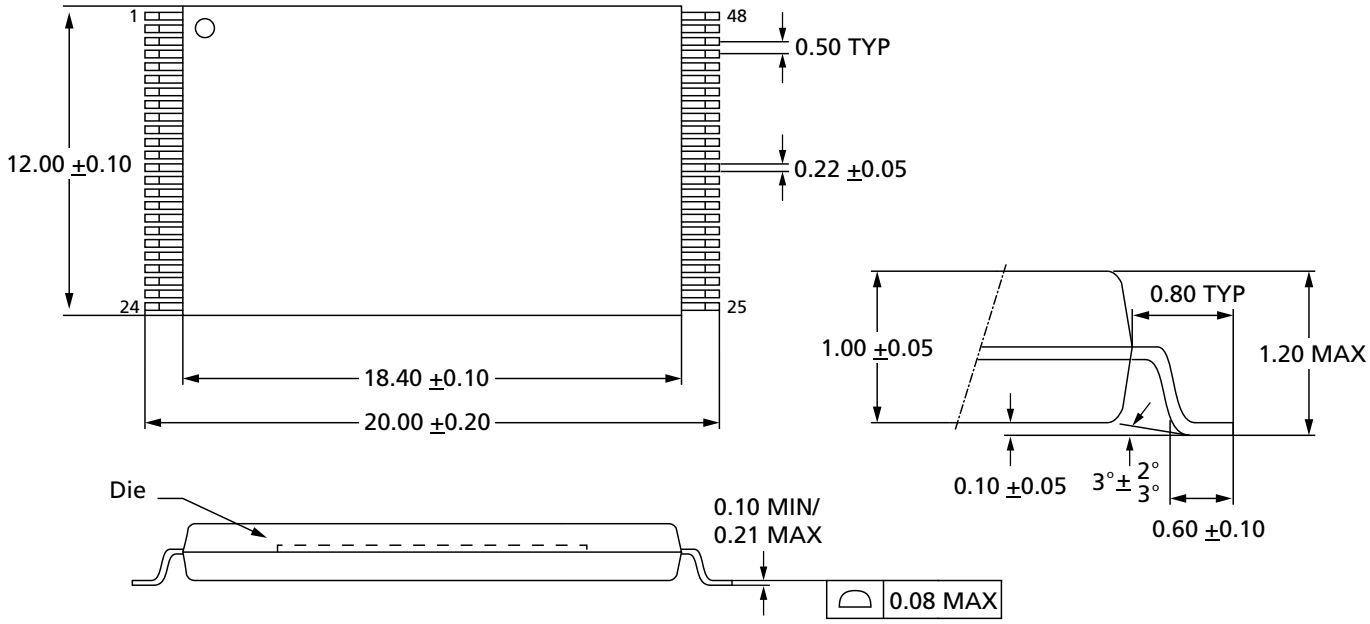
# Package Dimensions

**Figure 29: 48-Lead TSOP – 12mm x 20mm**




Note: 1. Drawing is not to scale.


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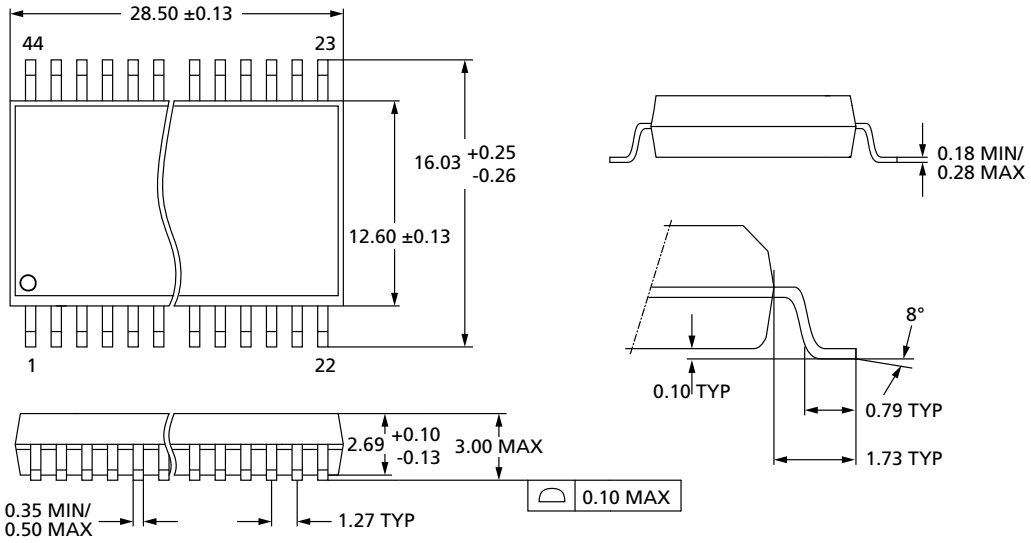
**Figure 30: 44-Lead Small-Outline – 500 Mil**




Note: 1. Drawing is not to scale.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# Revision History

## Rev. B – 2/14

- In Block and Chip Protection section, added block protect and chip unprotect flowcharts

## Rev. A – 2/13

- Initial Micron brand release

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