DDR3 SDRAM UDIMM

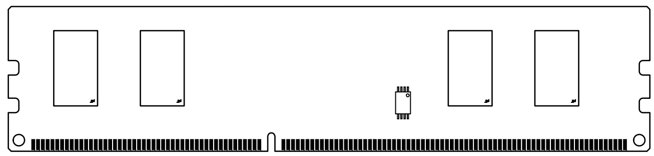
MT4JTF6464AZ – 512MB
MT4JTF12864AZ – 1GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 512 (128 Meg x 64), 1GB (128 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.5V \pm 0.075V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin UDIMM (MO-269 R/C C)

Module height: 30.0mm (1.181in)



Options	**Marking**
• Operating temperature [1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	8K A[12:0]	16K A[13:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb 64 Meg x 16	2Gb 128 Meg x 16
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT41J64M16,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT4JTF6464AZ-1G6__	512MB	64 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4JTF6464AZ1G4__	512MB	64 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4JTF6464AZ-1G1__	512MB	64 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41J128M16,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Da-ta Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT4JTF12864AZ-1G6__	1GB	128 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4JTF12864AZ-1G4__	1GB	128 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4JTF12864AZ-1G1__	1GB	128 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT4JTF12864AZ-1G4D1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin DDR3 UDIMM Front								240-Pin DDR3 UDIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DM3	182	V_{DD}	212	DM5
3	DQ0	33	DQS3#	63	CK1	93	DQS5#	123	DQ5	153	NC	183	V_{DD}	213	NC
4	DQ1	34	DQS3	64	CK1#	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42	126	NC	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	NC	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	NC	98	V_{SS}	128	DQ6	158	NC	188	A0	218	DQ52
9	DQ2	39	NC	69	V_{DD}	99	DQ48	129	DQ7	159	NC	189	V_{DD}	219	DQ53
10	DQ3	40	NC	70	A10	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	NC	191	V_{DD}	221	DM6
12	DQ8	42	NC	72	V_{DD}	102	DQS6#	132	DQ13	162	NC	192	RAS#	222	NC
13	DQ9	43	NC	73	WE#	103	DQS6	133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}	134	DM1	164	NC	194	V_{DD}	224	DQ54
15	DQS1#	45	NC	75	V_{DD}	105	DQ50	135	NC	165	NC	195	ODT0	225	DQ55
16	DQS1	46	NC	76	NC	106	DQ51	136	V_{SS}	166	V_{SS}	196	NC/A13[1]	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	NC	107	V_{SS}	137	DQ14	167	NC	197	V_{DD}	227	DQ60
18	DQ10	48	NC	78	V_{DD}	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	V_{SS}	169	NC	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DM7
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#	141	DQ21	171	NC	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	NC	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	NC	83	V_{SS}	113	V_{SS}	143	DM2	173	V_{DD}	203	DM4	233	DQ62
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

Note: 1. Pin 196 is NC for 512MB and A13 for 1GB.

Table 6: Pin Descriptions

Symbol	Type	Description
A[13:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[12:0] address the 1Gb DDR3 devices. A[13:0] address the 2Gb DDR3 devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK[1:0], CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** An active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DD}.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the communication to and from the temperature sensor/SPD EEPROM.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V. The component V_{DD} and V_{DDQ} are connected to the module Vdd.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address (V_{DD}/2).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM (V_{DD}/2).
V_{SS}	Supply	Ground.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD}/2).
NC	–	**No connect:** These pins are not connected on the module.

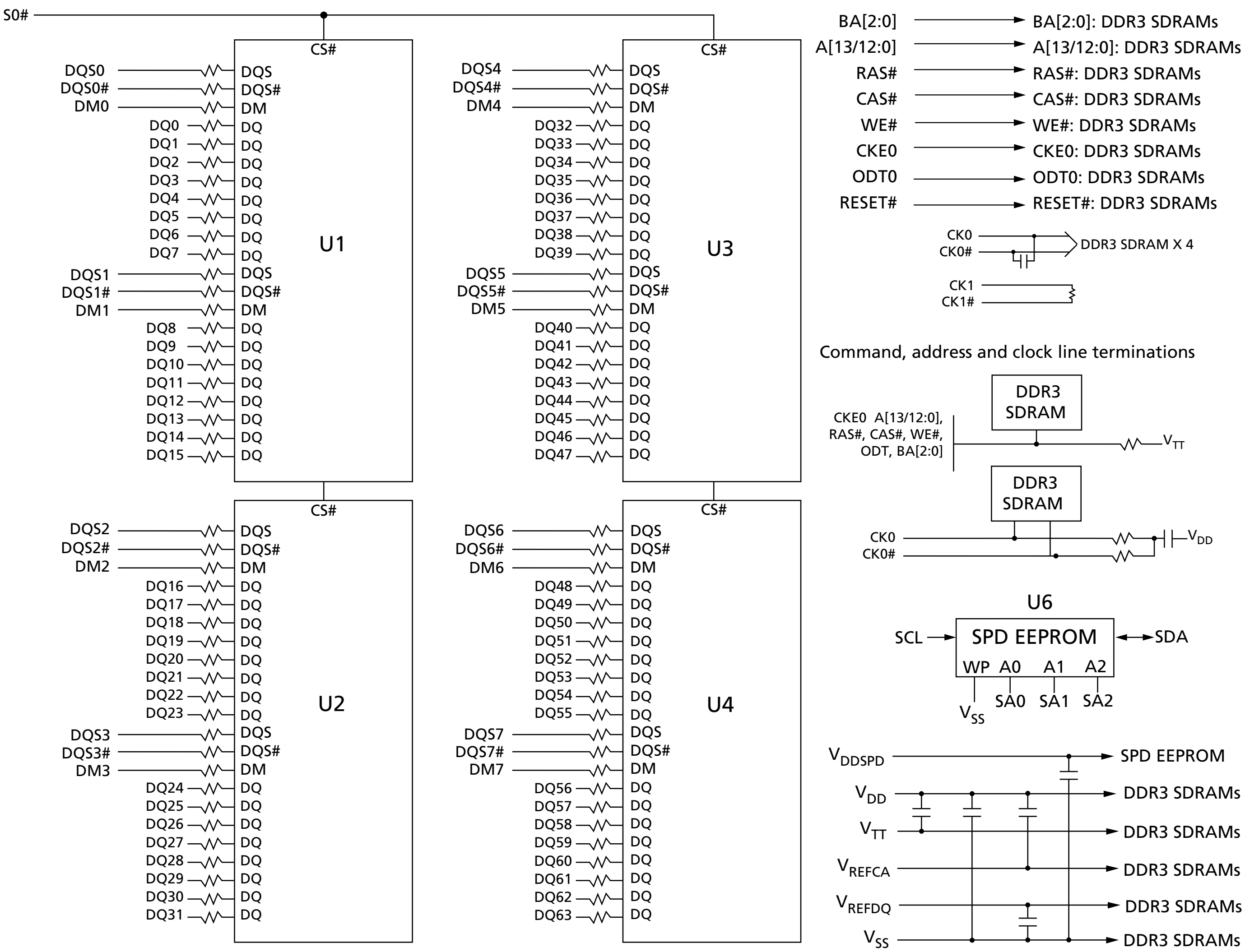
DQ Map

Table 7: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	9	U2	0	18	27
	1	1	4		1	17	22
	2	3	10		2	19	28
	3	5	123		3	21	141
	4	6	128		4	22	146
	5	4	122		5	20	140
	6	7	129		6	23	147
	7	0	3		7	16	21
	8	8	12		8	24	30
	9	15	138		9	31	156
	10	9	13		10	25	31
	11	11	19		11	27	37
	12	12	131		12	28	149
	13	14	137		13	30	155
	14	13	132		14	29	150
	15	10	18		15	26	36
U3	0	34	87	U4	0	50	105
	1	33	82		1	49	100
	2	35	88		2	51	106
	3	37	201		3	53	219
	4	38	206		4	54	224
	5	36	200		5	52	218
	6	39	207		6	55	225
	7	32	81		7	48	99
	8	40	90		8	56	108
	9	47	216		9	63	234
	10	41	91		10	57	109
	11	43	97		11	59	115
	12	44	209		12	60	227
	13	46	215		13	62	233
	14	45	210		14	61	228
	15	42	96		15	58	114

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, “Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules.” These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via an I^2C bus. Write protect (WP) is connected to Vss, permanently disabling hardware write protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
$V_{REFCA(DC)}$	Input reference voltage command/address bus		$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus		$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	+600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		$0.49 \times V_{DD}$ - 20mV	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$ + 20mV	V	1
I_I	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; V_{REF} input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE, ODT, CK, CK#	–8	0	+8	µA	
		DM	–2	0	+2		
I_{OZ}	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–5	0	+5	µA	
I_{VREF}	V_{REF} supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		–4	0	+4	µA	
T_A	Module ambient operating temperature		0	–	+70	°C	2, 3
T_C	DDR3 SDRAM component case operating temperature		0	–	+85	°C	2, 3, 4

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when $85°C < T_C \leq 95°C$.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 11: DDR3 I_{DD} Specifications and Conditions – 512MB

Values are for the MT41J64M16 DDR3 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	480	440	400	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	680	600	520	mA
Precharge power-down current: Slow exit	I_{DD2P}	48	48	48	mA
Precharge power-down current: Fast exit	I_{DD2P}	180	160	140	mA
Precharge quiet standby current	I_{DD2Q}	268	240	212	mA
Precharge standby current	I_{DD2N}	280	260	220	mA
Precharge standby ODT current	I_{DD2NT}	460	420	380	mA
Active power-down current	I_{DD3P}	180	160	140	mA
Active standby current	I_{DD3N}	260	240	220	mA
Burst read operating current	I_{DD4R}	1280	1160	1040	mA
Burst write operating current	I_{DD4W}	1720	1420	1180	mA
Refresh current	I_{DD5B}	1040	960	880	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	24	24	24	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	36	36	36	mA
All banks interleaved read current	I_{DD7}	1840	1680	1520	mA
Reset current	I_{DD8}	56	56	56	mA

Table 12: DDR3 I_{DD} Specifications and Conditions – 1GB

Values are for the MT41J128M16DDR3 SDRAM only and are computed from values specified in the 2Gb (128 Meg x 16) component data sheet (Die Rev D)

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	TBD	480	420	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	TBD	600	520	mA
Precharge power-down current: Slow exit	I_{DD2P}	TBD	48	48	mA
Precharge power-down current: Fast exit	I_{DD2P}	TBD	140	120	mA
Precharge quiet standby current	I_{DD2Q}	TBD	260	220	mA
Precharge standby current	I_{DD2N}	TBD	260	220	mA
Precharge standby ODT current	I_{DD2NT}	TBD	400	360	mA
Active power-down current	I_{DD3P}	TBD	180	160	mA
Active standby current	I_{DD3N}	TBD	300	240	mA
Burst read operating current	I_{DD4R}	TBD	1160	980	mA
Burst write operating current	I_{DD4W}	TBD	1340	1120	mA
Refresh current	I_{DD5B}	TBD	1020	980	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	TBD	36	36	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	TBD	48	48	mA

Table 12: DDR3 I_{DD} Specifications and Conditions – 1GB (Continued)

Values are for the MT41J128M16DDR3 SDRAM only and are computed from values specified in the 2Gb (128 Meg x 16) component data sheet (Die Rev D)

Parameter	Symbol	1600	1333	1066	Units
All banks interleaved read current	I_{DD7}	TBD	1780	1560	mA
Reset current	I_{DD8}	TBD	56	56	mA

Serial Presence-Detect EEPROM

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} + 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} + 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	2.0	µA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	^tSCL	10	400	kHz	
Clock pulse width high time	^tHIGH	0.6	–	µs	
Clock pulse width low time	^tLOW	1.3	–	µs	
SDA rise time	^tR	–	300	µs	1
SDA fall time	^tF	20	300	ns	1
Data-in setup time	$^tSU:DAT$	100	–	ns	
Data-in hold time	$^tHD:DI$	0	–	µs	
Data-out hold time	$^tHD:DAT$	200	900	ns	
Data out access time from SCL low	$^tAA:DAT$	0.2	0.9	µs	2
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
WRITE time	^tW	–	10	ms	

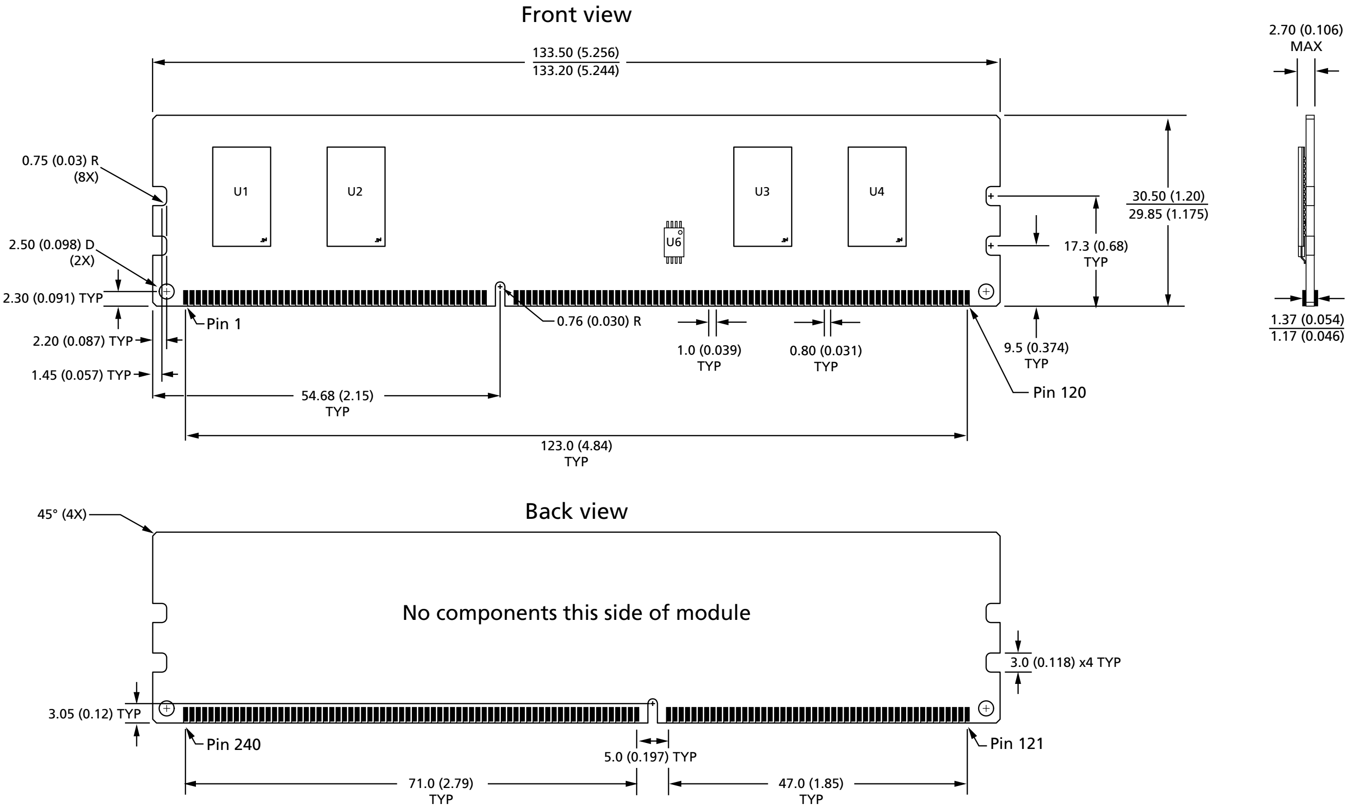
Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.