



SPN30T10

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN30T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. SPN30T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

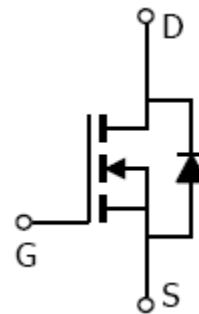
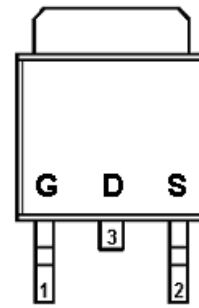
- ◆ 100V/20A, $R_{DS(ON)}=50m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252 package design

APPLICATIONS

- High Frequency Small Power System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

TO-252



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN30T10T252RGB	TO-252	SPN30T10

※ SPN30T10T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	100	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	T _C =25°C	22	A
		T _C =70°C	16	
Pulsed Drain Current	I _{DM}	45	A	
Avalanche Current	I _{AS}	27	A	
Power Dissipation @ TA=25°C	P _D	52	W	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W	



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			10	μA
		V _{DS} =80V, V _{GS} =0V T _J =125°C			100	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V	22			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =10V, I _D =20A			45	mΩ
		V _{GS} =4.5V, I _D =15A			50	mΩ
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =3A		68		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =4.5V I _D =15A		55		nC
Gate-Source Charge	Q _{gs}			7.5		
Gate-Drain Charge	Q _{gd}			7		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		3850		pF
Output Capacitance	C _{oss}			137		
Reverse Transfer Capacitance	C _{rss}			82		
Turn-On Time	t _{d(on)}	V _{DD} =50V, I _D =1A, V _{GEN} =10V R _G =3.3Ω		19		nS
	t _r			4		
Turn-Off Time	t _{d(off)}			84		
	t _f			5		



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TYPICAL CHARACTERISTICS

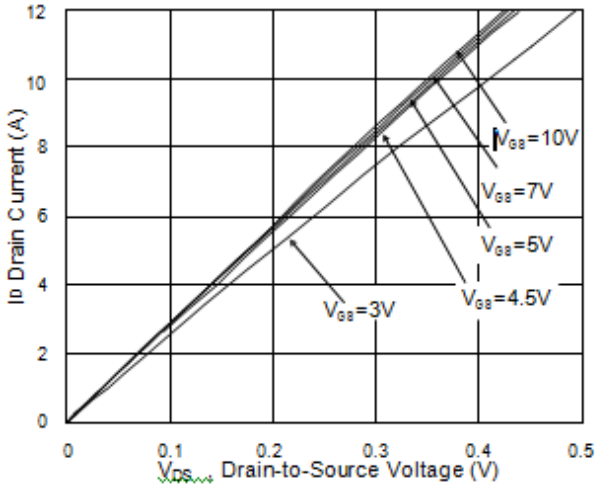


Fig. 1 Typical Output Characteristics

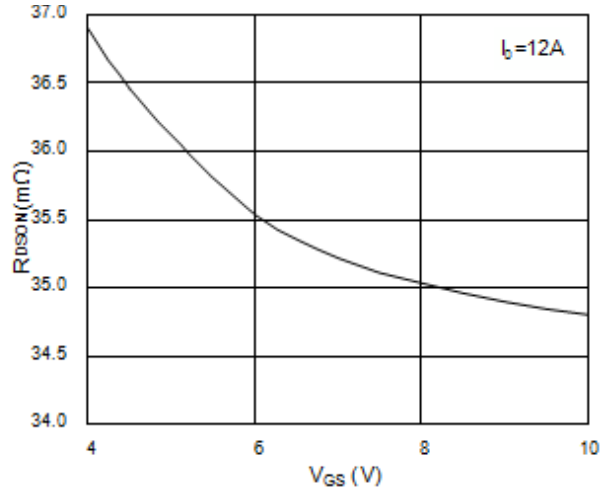


Fig. 2 On-Resistance vs. Gate Voltage

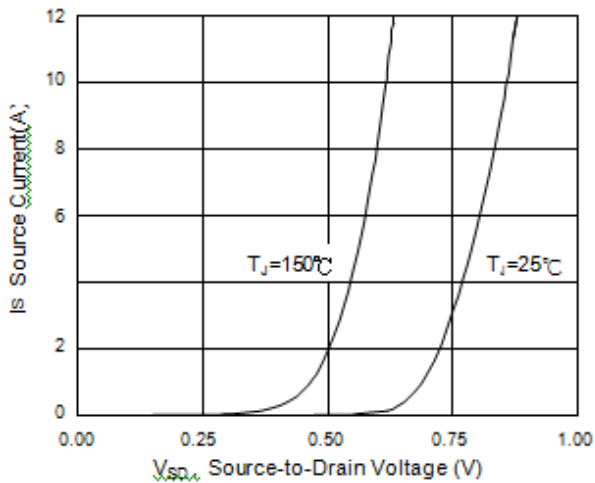


Fig. 3 Forward Characteristics of Reverse Diodes

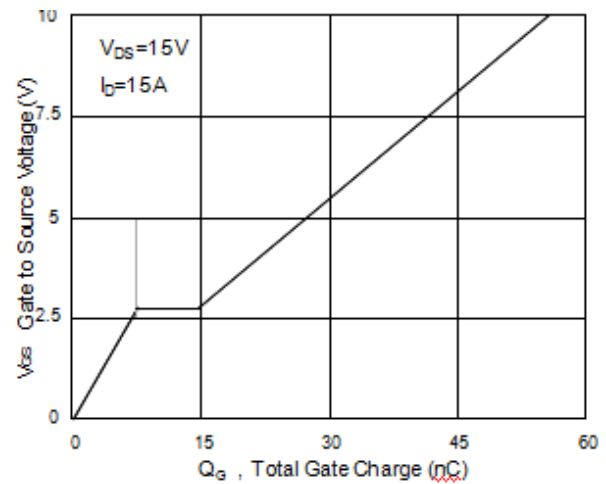


Fig. 4 Gate Charge Characteristics

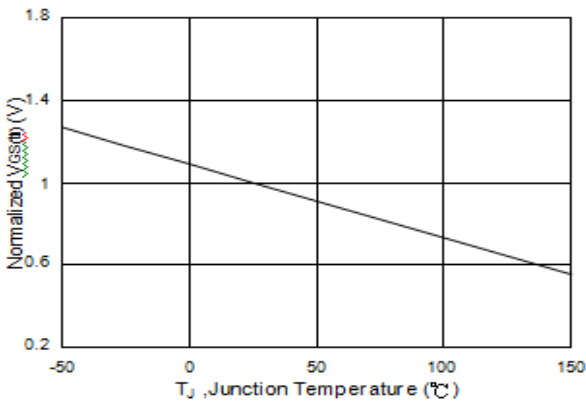


Fig. 5 Vgs vs. Junction Temperature

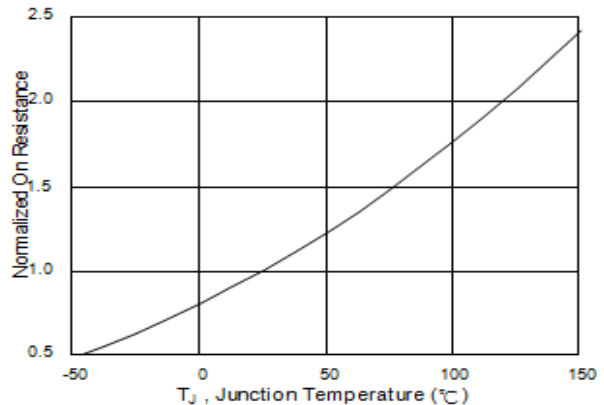


Fig. 6 On-resistance vs. Junction Temperature



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TYPICAL CHARACTERISTICS

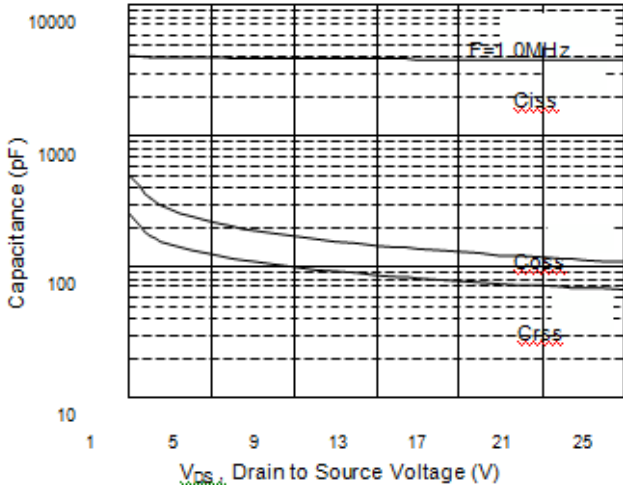


Fig. 7 Typical Capacitance Characteristics

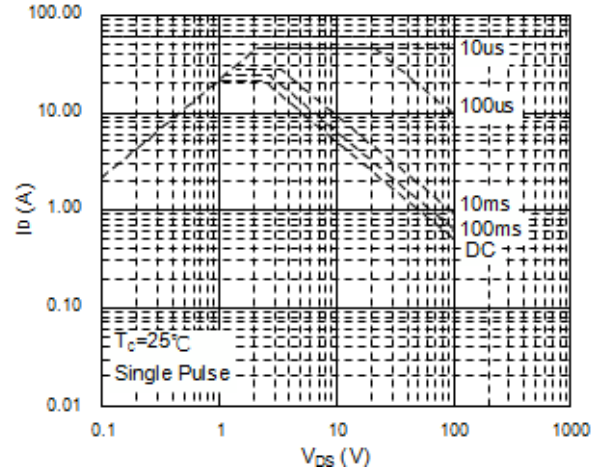


Fig. 8 Maximum Safe Operation Area

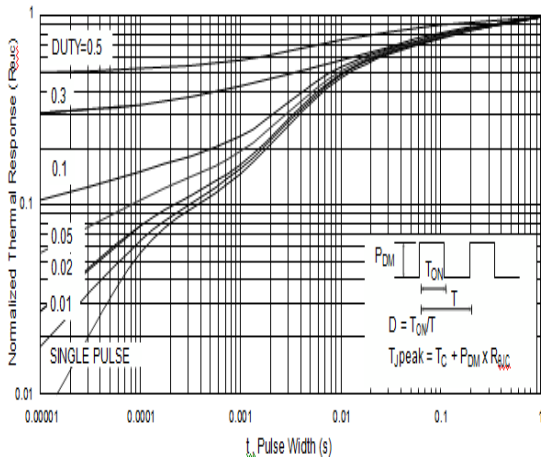


Fig. 9 Effective Transient Thermal Impedance

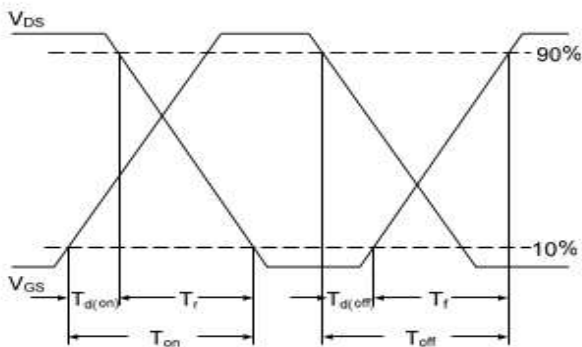


Fig. 10 Switching Time Waveform

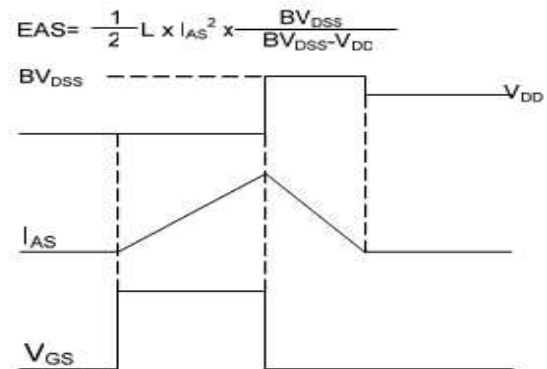


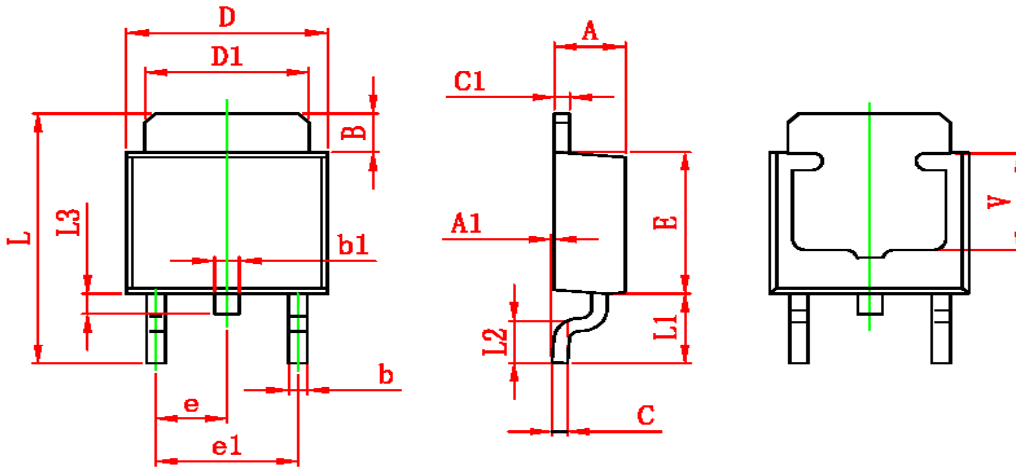
Fig. 11 Unclamped Inductive Waveform



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TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.350	0.650	0.014	0.026
V	3.80 REF		0.150 REF	



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