TOPRO
凌越科技
Topro Technology Inc.

# TP6312FE

**1/4 – To 1/11 – DUTY FIP (VFD)**
**CONTROLLER/DRIVER**

# *DataSheet*

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# TP6312FE

**1/4 – To 1/11 – DUTY FIP (VFD)
CONTROLLER/DRIVER**

## General Specification

The TP6312E is a FIP (Fluorescent lndicator Panel or Vacuum Fluorescent Display) controller/driver that is driven on a 1/4 – to 1/11 duty factor. It consists of 11 segment output lines, 6 grid output lines, 5 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the TP6312E through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device of a single-chip microcomputer.

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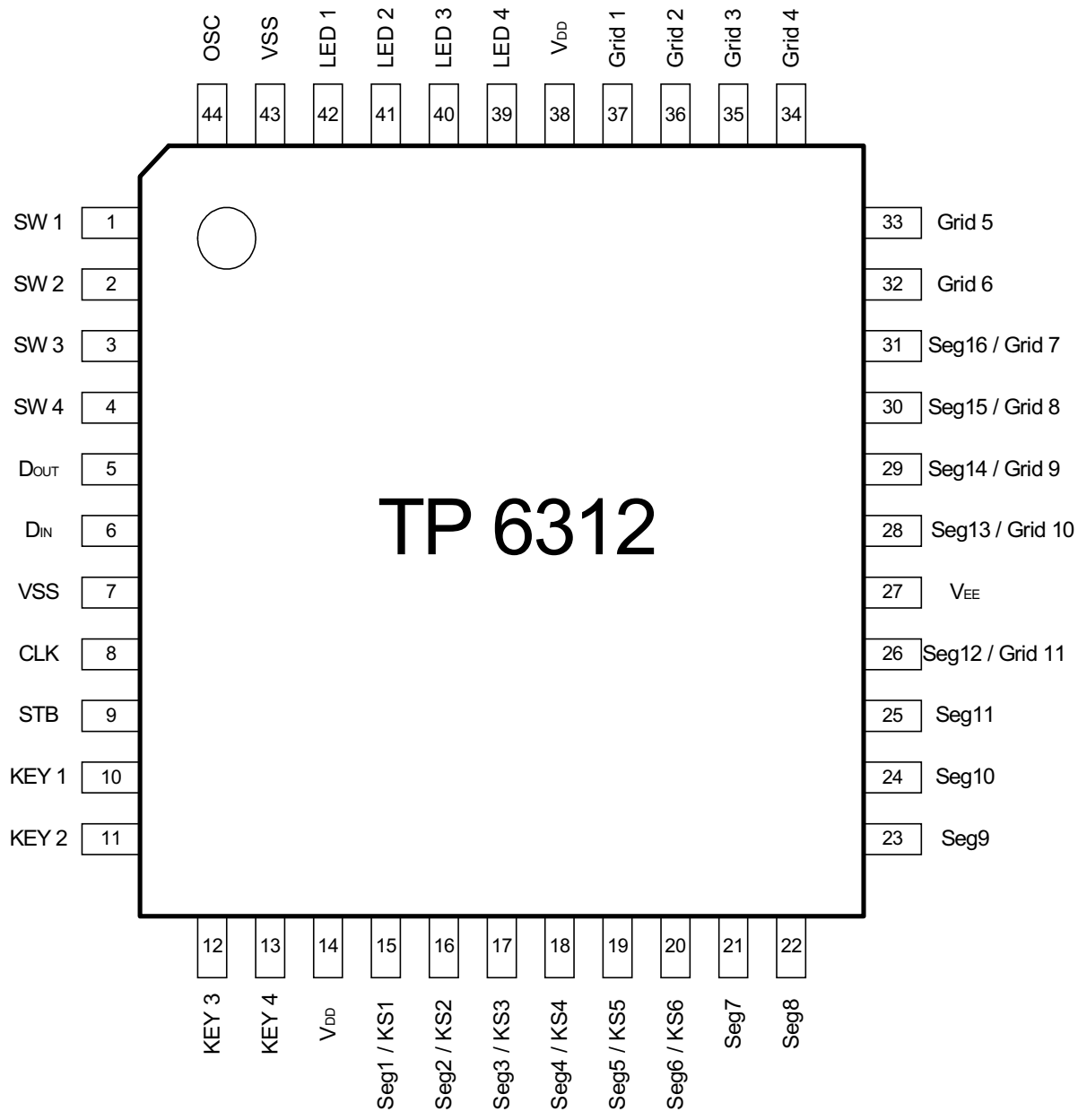
## Contents：

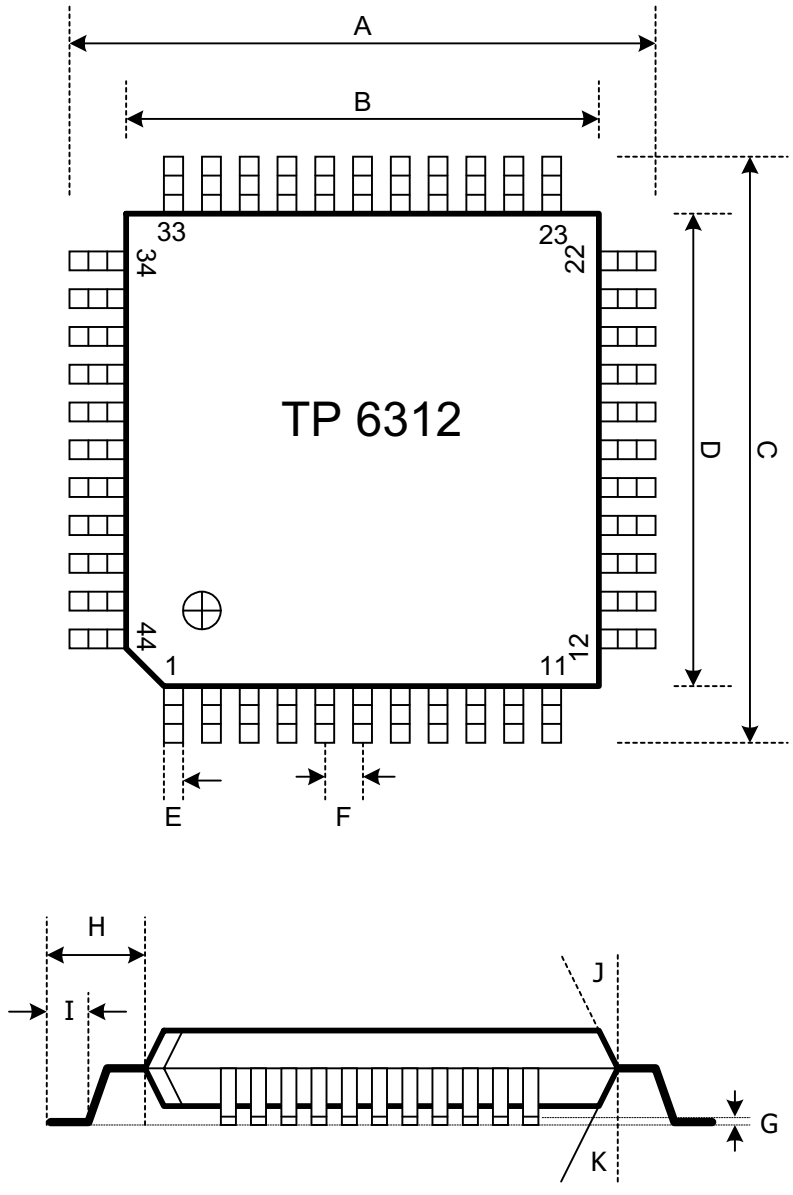
# TP6312FE

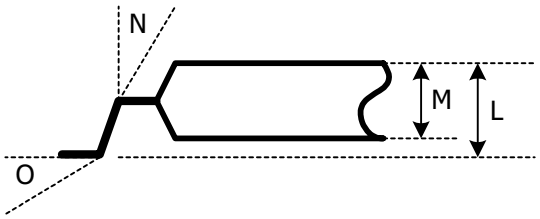
**1/4 – To 1/11 – DUTY FIP (VFD)**
**CONTROLLER/DRIVER**

## Pin Configurations and Package Type



## 44-Pin Plastic LQFP (unit : mm)






**NOTE :** Each lead centerline is located within 0.15 mm (0.006 inch) of it is true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 12.00 ± 0.2 |
| B | 10.00 BSC |
| C | 12.00 ± 0.2 |
| D | 10.00 BSC |
| E | 0.3 / 0.37 / 0.45 |
| F | 0.80 BSC |
| G | 0.05 / 0.15 |
| H | 1.0 REF |
| I | 0.45 / 0.60 / 0.75 |
| J | 12° ± 1° |
| K | 12° ± 1° |
| L | 1.60 MAX |
| M | 1.40 ± 0.05 |
| N | 0 ° MIN |
| O | 0 ° /3 ° /7 ° |

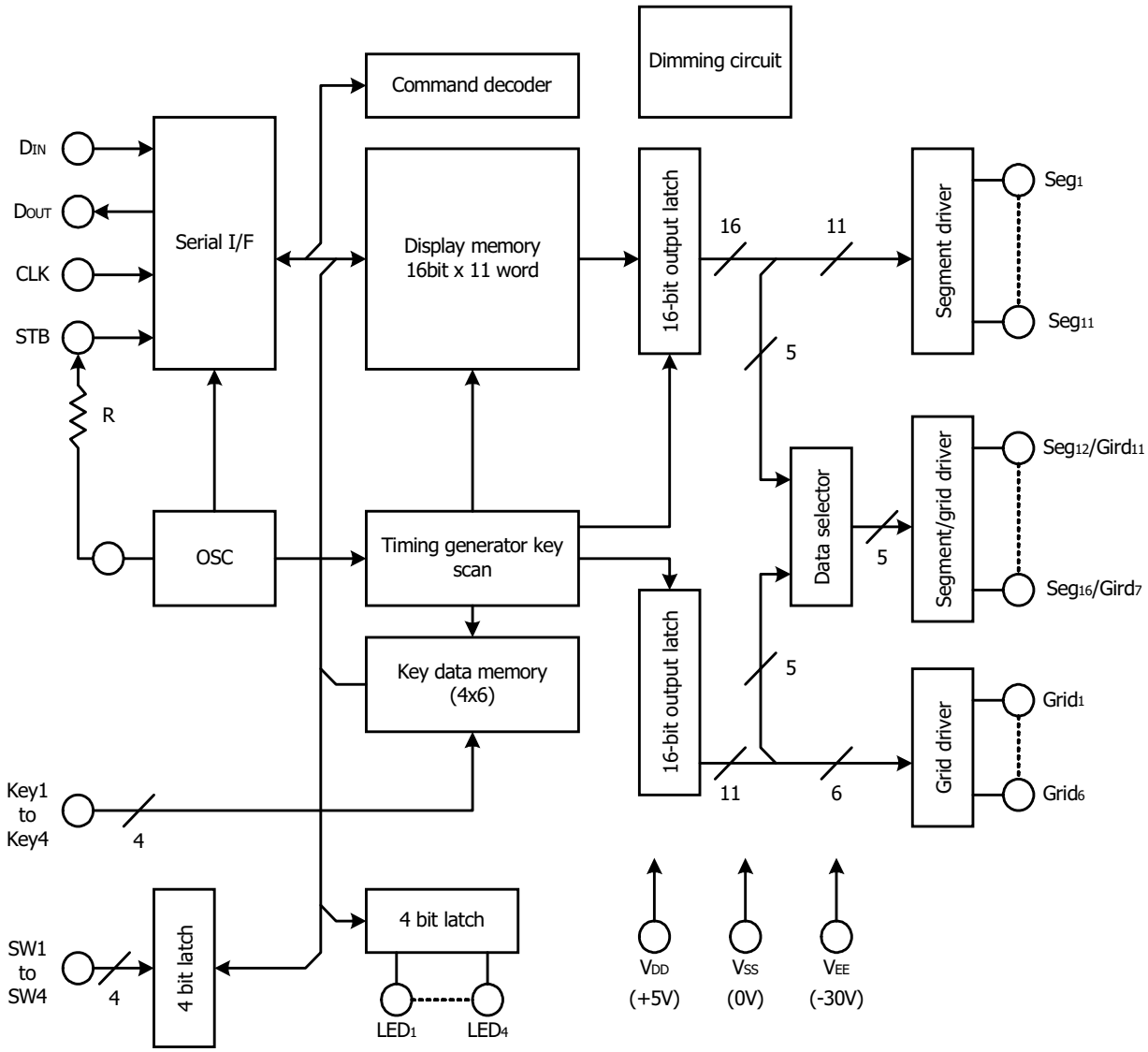
# Pin Descriptions

| Pin No | Symbol | Pin Name | Description |
|---|---|---|---|
| 6 | $D_{IN}$ | Date input | Input serial data at rising edge of shift clock, starting from the lower bit. |
| 5 | $D_{OUT}$ | Date output | Outputs serial data at falling edge of shift clock, starting from the lower bit. This is N-ch open-drain output pin. |
| 9 | STB | Strobe | Initializes the serial interface at rising or falling edge to make TP6312E waiting for reception of command. Data input after STB has fallen is processed as command. While command data is processed, current processing is stopped, and serial interface is initialized . While STB is high, CLK is ignored. |
| 8 | CLK | Clock input | Reads serial data at rising edge, and outputs data at falling edge. |
| 44 | OSC | Oscillator pin | Connect a resistor to this pin to determine the oscillation frequency to this pin. |
| 15 to 20 | $Seg_1/KS_1$ to $Seg_6/KS_6$ | High-voltage output | Segment output pins (Dual function as key source) |
| 21 to 25 | $Seg_7$ to $Seg_{11}$ | High-voltage output (segment) | Segment output pins |
| 37 to 32 | $Grid_1$ to $Grid_6$ | High-voltage output (grid) | Grid output pins |
| 26, 28 to 31 | $Seg_{11}/Grid_{11}$ to $Seg_{16}/Grid_7$ | High-voltage output (segment/grid) | These pins are selectable for segment or grid driving. |
| 42 to 39 | $LED_1$ to $LED_4$ | LED output | CMOS output. +20 mA max |
| 10 to 13 | $KEY_1$ to $KEY_4$ | Key data input | Data input to these pins is latched at the end of display cycle. |
| 1 to 4 | $SW_1$ to $SW_4$ | Switch input | These pins constitute 4-bit general-purpose input port. |
| 14, 38 | $V_{DD}$ | Logic power | 5V ± 10% |
| 7, 43 | $V_{SS}$ | Logic ground | Connect this pin to system GND. |
| 27 | $V_{EE}$ | Pull-down level | $V_{DD}$ – 35 V max |

# TP6312FE

**1/4 – To 1/11 – DUTY FIP (VFD)
CONTROLLER/DRIVER**

## Functional Block Diagram



# Function Descriptions

## Display RAM Address and Display Mode

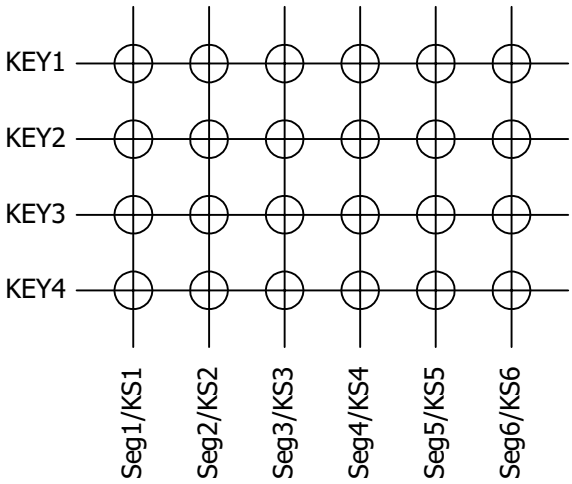
The display RAM stores the data transmitted from an external device to the TP6312E through the serial interface, and is assigned addresses as follows, in units of 8 bits:

| $Seg_1$ | $Seg_4$ | $Seg_8$ | $Seg_{12}$ | $Seg_{16}$ | |
|---|---|---|---|---|---|
| $00H_L$ | $00H_U$ | $01H_L$ | $01H_U$ | | DIG1 |
| $02H_L$ | $02H_U$ | $03H_L$ | $03H_U$ | | DIG2 |
| $04H_L$ | $04H_U$ | $05H_L$ | $05H_U$ | | DIG3 |
| $06H_L$ | $06H_U$ | $07H_L$ | $07H_U$ | | DIG4 |
| $08H_L$ | $08H_U$ | $09H_L$ | $09H_U$ | | DIG5 |
| $0AH_L$ | $0AH_U$ | $0BH_L$ | $0BH_U$ | | DIG6 |
| $0CH_L$ | $0CH_U$ | $0DH_L$ | $0DH_U$ | | DIG7 |
| $0EH_L$ | $0EH_U$ | $0FH_L$ | $0FH_U$ | | DIG8 |
| $10H_L$ | $10H_U$ | $11H_L$ | $11H_U$ | | DIG9 |
| $12H_L$ | $12H_U$ | $13H_L$ | $13H_U$ | | DIG10 |
| $14H_L$ | $14H_U$ | $15H_L$ | $15H_U$ | | DIG11 |

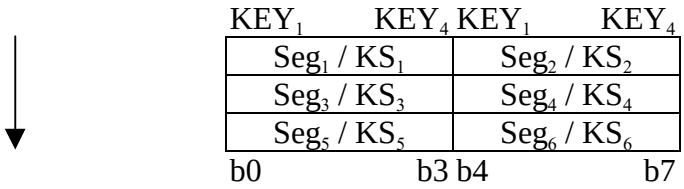
| $b_0$ | $b_3$ $b_4$ | $b_7$ |
|---|---|---|
| XX $H_L$ | XX $H_U$ | |
| Lower 4 bits | Higher 4 bits. | |

## Key Matrix and Key-Input Data Storage RAM

The key matrix is of 6 × 4 configuration, as shown below.



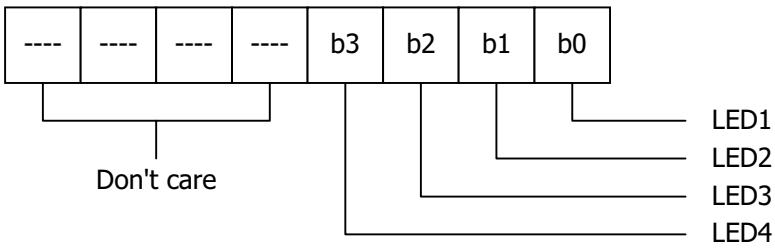

The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.




Reading sequence

## LED PORT

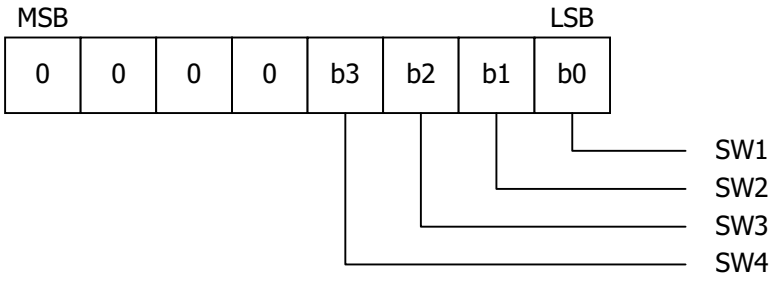
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights ; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.




On power application, all LEDs are unlit.

## SW Data

The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.




## Commands

A command sets the display mode and status of the FIP driver.

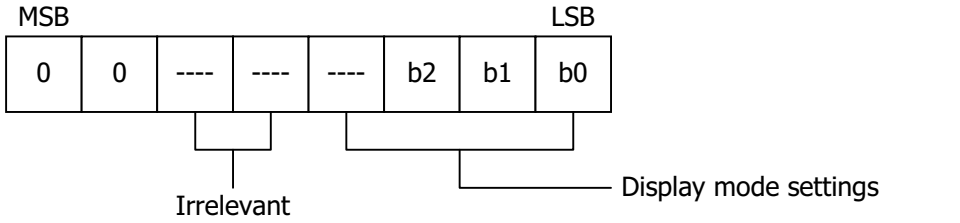
The first 1 byte input to the TP6312E through the Din pin after the STB pin has fallen is regarded as a command.

If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

**(1) Display mode setting command**

This command initializes the TP6312E and selects the number of segments and number of grids (1/4 to 1/11 duty, 11 segments to 16 segments).

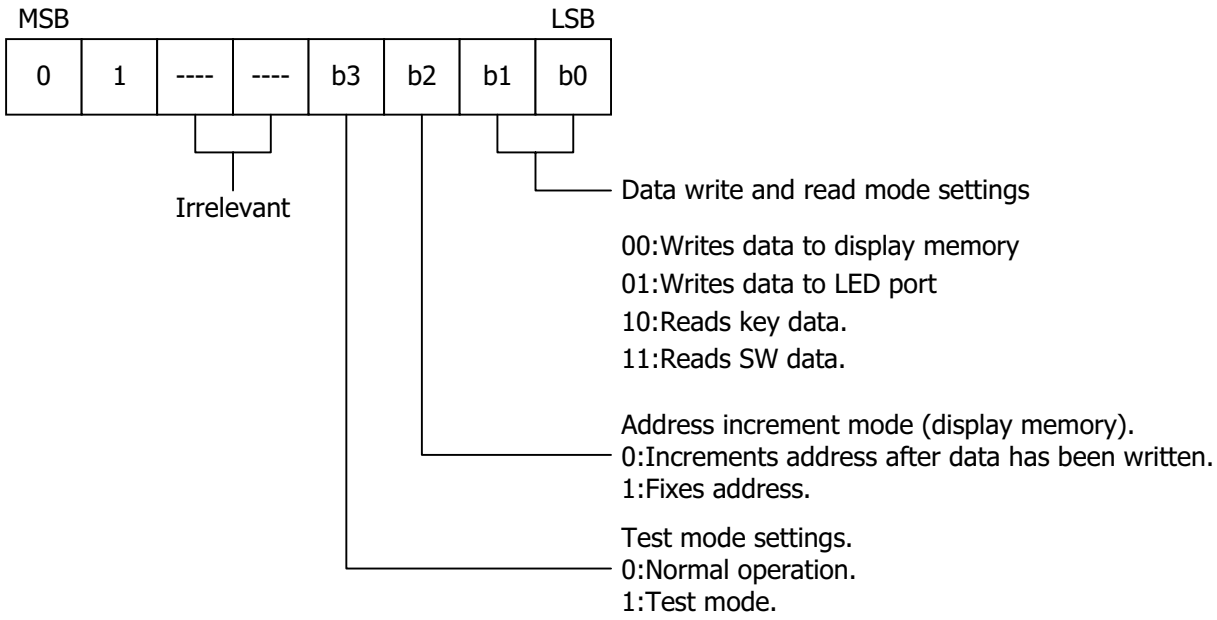
On power application, the 11-digit, 11-segment mode is selected.




000 : 4 digits, 16 segments
001 : 5 digits, 16 segments
010 : 6 digits, 16 segments
011 : 7 digits, 15 segments
100 : 8 digits, 14 segments
101 : 9 digits, 13 segments
110 : 10 digits, 12 segments
111 : 11 digits, 11 segments

**(2) Data setting commands**

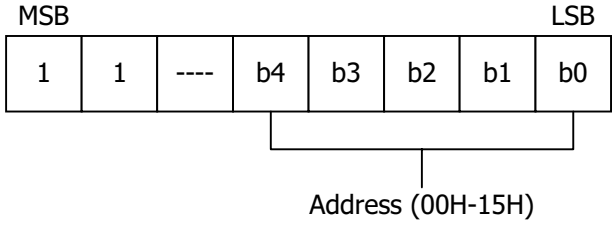
This command sets data write and read modes.




On power application, the normal operation mode and address increment mode set.

**(3) Address setting command**

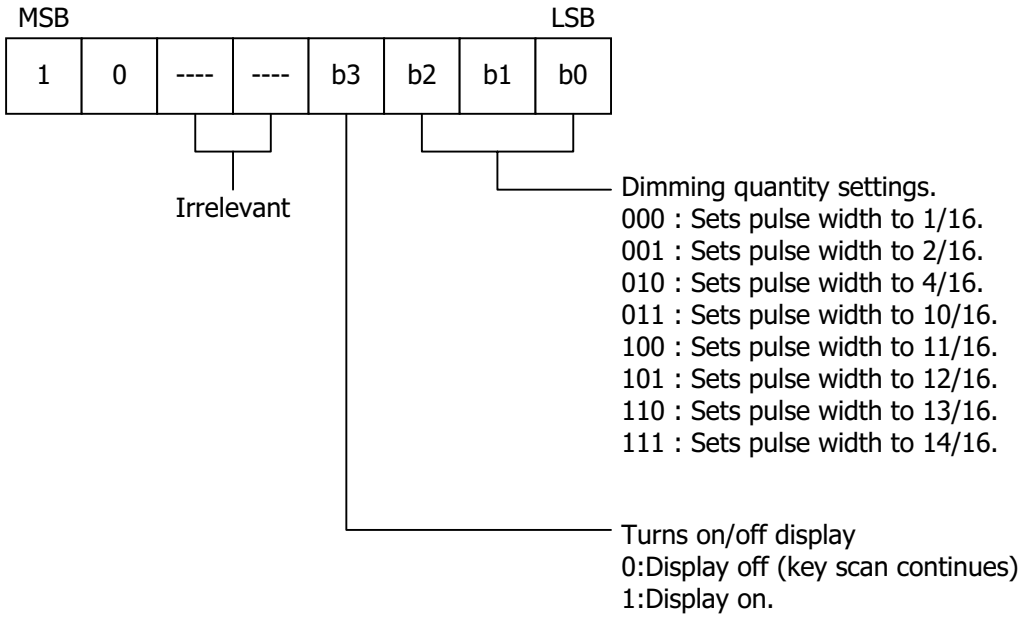
This command sets an address of the display memory.




If address 16H or higher is set, the data is ignored, unit a correct address is set.

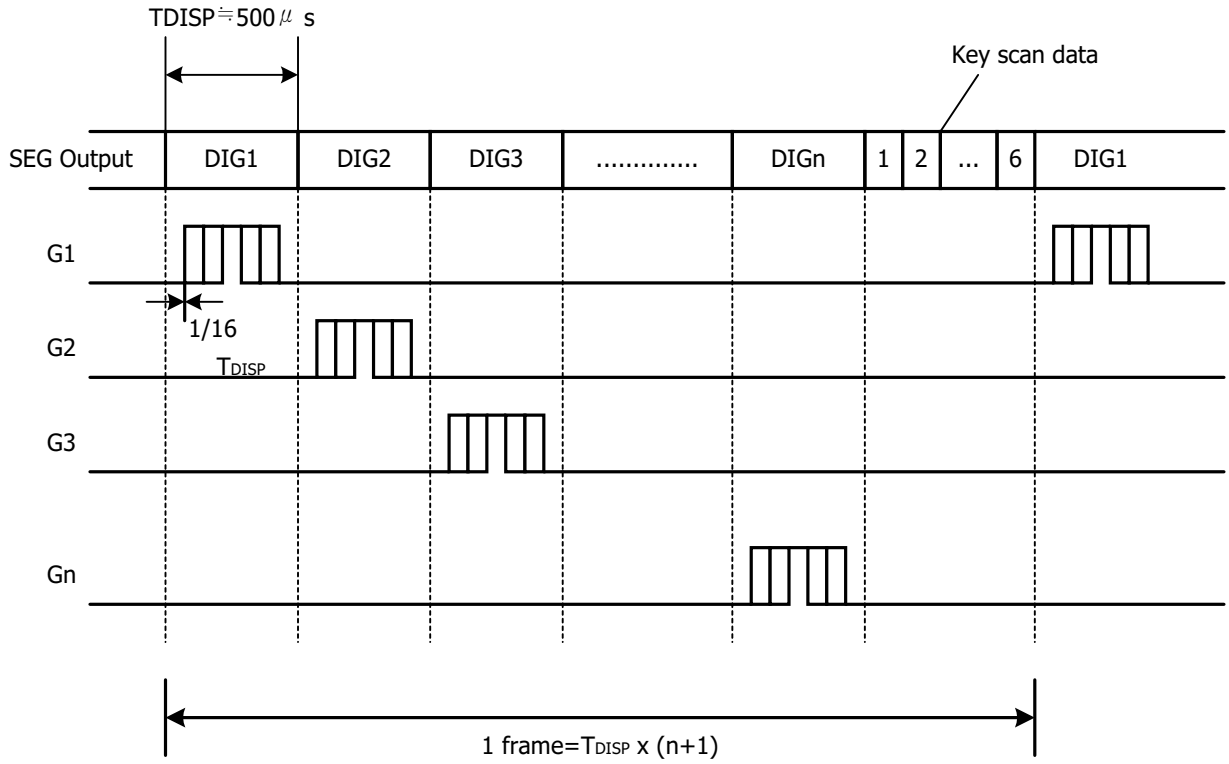
On power application, the address is set to 00H.

**(4) Display control command**




On power application, the 14/16 pulse width is set and the display is turned off.

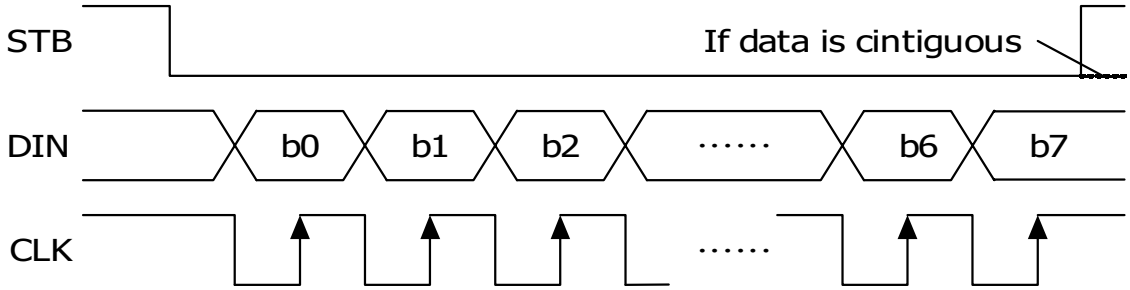
## Key Scanning and Display Timing



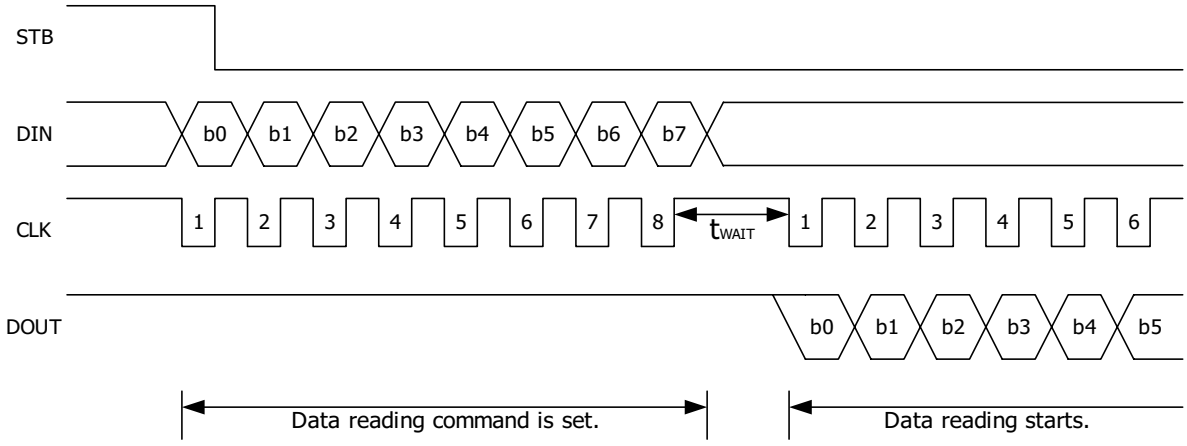

One cycle of key scanning consists of two frames, and data of 6 × 4 matrices is stored in RAM.

## Serial Communication Format

**Reception (command/data write)**




**Transmission (data read)**




Because the $D_{OUT}$ pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

* : When data is read, a wait time $t_{WAIT}$ of 1μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

# Absolute Maximum Ratings

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Logic Supply Voltage | $V_{DD}$ | -0.5 to + 0.7 | V |
| Driver Supply Voltage | $V_{EE}$ | $V_{DD}$ +0.5 to $V_{DD}$ -40 | V |
| Logic Input Voltage | $V_{i1}$ | -0.5 to $V_{DD}$ +0.5 | V |
| FIP Driver Output Voltage | $V_{o2}$ | $V_{EE}$ –0.5 to $V_{DD}$ +0.5 | V |
| LED Driver Output Current | $I_{o1}$ | +25 | mA |
| FIP Driver Output Current | $I_{o2}$ | -40 (grid)<br>-15 (segment) | mA |
| Power Dissipation | $P_D$ | 800* | mW |
| Operating Ambient Temperature | $T_{opt}$ | -40 to +85 | ℃ |
| Storage Temperature | $T_{stg}$ | -65 to +150 | ℃ |

* Derate at –6.4 mW/℃ at Ta = 25℃ or higher.

# DC Electrical Characteristic

## RECOMMENDED OPERATING CONDITION (Ta=-20℃ to +70℃, Vss=0 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V | |
| High-Level input Voltage | $V_{IH}$ | $0.6V_{DD}$ | | $V_{DD}$ | V | |
| Low-Level input Voltage | $V_{IL}$ | 0 | | $0.3V_{DD}$ | V | |
| Driver Supply Voltage | $V_{EE}$ | 0 | | $V_{DD}$-35 | V | |

Maximum power consumption $P_{MAX}$.=FIP driver dissipation + $R_L$ dissipation + LED driver dissipation + dynamic power consumption.

Where segment current = 3 mA, grid current = 15mA, and LED current = 20 mA,

FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)

$R_L$ dissipation $\fallingdotseq$ $(V_{DD}-V_{EE})^2/50$ x (segment+1) (mW)

LED driver dissipation = number of LEDs x 20(mW)

Dynamic power consumption = $V_{DD}$ x 5(mW)

## Example

Where $V_{EE}$ = -25 V, $V_{DD}$ = 5 V, and in 16-segment and 6-digit modes,

| | |
|---|---|
| FIP driver dissipation = 16 x 6 + 6/7 x 30 = | 122 |
| $R_L$ dissipation = $30^2$/50 x 17 = | 306 |
| LED driver dissipation = 4 x 20 = | 80 |
| Dynamic power consumption = 5 x 5 = | 25 |
| | Total 533 mW |

## ELECTRICAL SPECIFICATIONS(Ta= -20 to + 70°C,$V_{DD}$= 4.5 to 5.5V,$V_S$ =0V,$V_{EE}$ =$V_{DD}$ - 35V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| High-Level Output Voltage | $V_{OH1}$ | 0.9 $V_{DD}$ | | | V | $LED_1$ – $LED_4$, $I_{OH1}$ = -1 mA |
| Low-Level Output Voltage | $V_{OL1}$ | | | 1 | V | $LED_1$ – $LED_4$, $I_{OL1}$ = 20 mA |
| Low-Level Output Voltage | $V_{OL2}$ | | | 0.4 | V | $D_{OUT}$, $I_{OL2}$ = 4 mA |
| High-Level Output Current | $I_{OH21}$ | -3 | | | mA | $V_O$ = $V_{DD}$ –2V, $Seg_1$ to $Seg_{11}$ |
| High-Level Output Current | $I_{OH22}$ | -15 | | | mA | $V_O$ = $V_{DD}$ –2V,$Grid_1$ to $Grid_6$, $Seg_{12}$/$Seg_{11}$ to $Seg_{16}$/$Seg_7$ |
| Driver Leakage Current | $I_{OLEAK}$ | | | -10 | µA | $V_O$ = $V_{DD}$ - 35V, Drive off |
| Output Pull-Down Resistor | $R_L$ | 50 | 100 | 150 | kΩ | Drive output |
| Input Current | $I_i$ | | | ±1 | µA | $V_I$ = $V_{DD}$ or $V_{SS}$ |
| High-Level Input Voltage | $V_{IH}$ | 0.6 $V_{DD}$ | | | V | |
| Low-Level Input Voltage | $V_{IL}$ | | | 0.3 $V_{DD}$ | V | |
| Hysteresis Voltage | $V_H$ | | 0.35 | | V | CLK, $D_{IN}$, STB |
| Dynamic Current Consumption | $I_{DDdyn}$ | | | 5 | mA | Under no load, display off |

# AC Electrical Characteristic

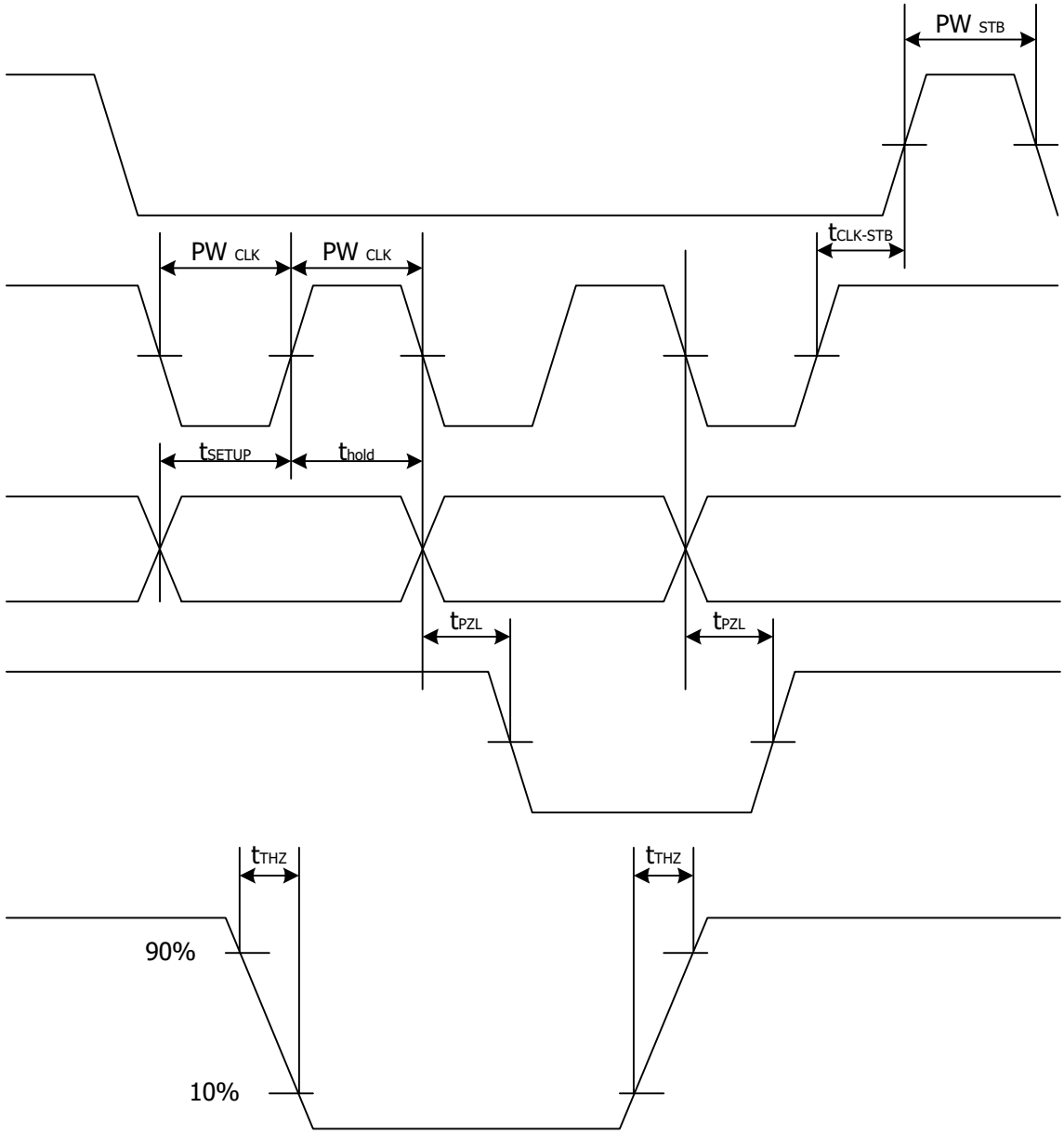
## SWITCHING CHARACTERISTICS(Ta = -20 to +70°C, $V_{DD}$ = 4.5 to 5.5V, $V_{EE}$ = -30V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| Oscillation Frequency | fOSC | 350 | 500 | 650 | kHz | R = 56kΩ | |
| Propagation Delay Time | tPLZ | | | 300 | ns | CLK ⇒ DOUT<br>CL = 15pF,RL = 10kΩ | |
| | tPZL | | | 100 | ns | | |
| Rise Time | tTZH1 | | | 2 | µs | CL = 300 PF | Seg1 to Seg11 |
| | tTZH2 | | | 0.5 | µs | | Grid1 to Grid6<br>Seg12/Grid11 to Seg16/Grid7 |
| Fall Time | tTHZ | | | 120 | µs | CL = 300 pF, Segn, Gridn | |
| Maximum Clock Frequency | fmax | 1 | | | MHz | Duty = 50% | |
| Input Capacitance | C1 | | | 15 | pF | | |

## TIMING CONDITIONS(Ta = -20 to +70°C, $V_{DD}$ = 4.5 to 5.5V)

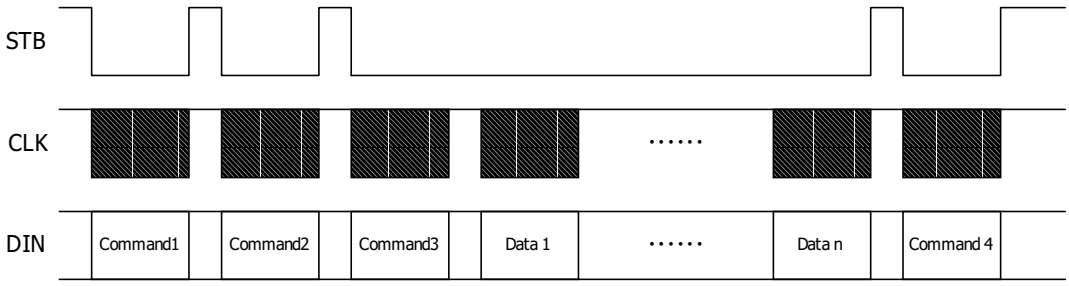
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Pulse Width | PWCLK | 400 | | | ns | |
| Strobe Pulse Width | PWSTB | 1 | | | µs | |
| Data Setup Time | tSETUP | 100 | | | ns | |
| Data Hold Time | tHOLD | 100 | | | ns | |
| Clock-Strobe Time | tCLK-STB | 1 | | | µs | CLK ↑ → STB ↑ |
| Wait Time | tWAIT | 1 | | | µs | CLK ↑ → CLK ↓ |

## Switching Characteristic Waveform



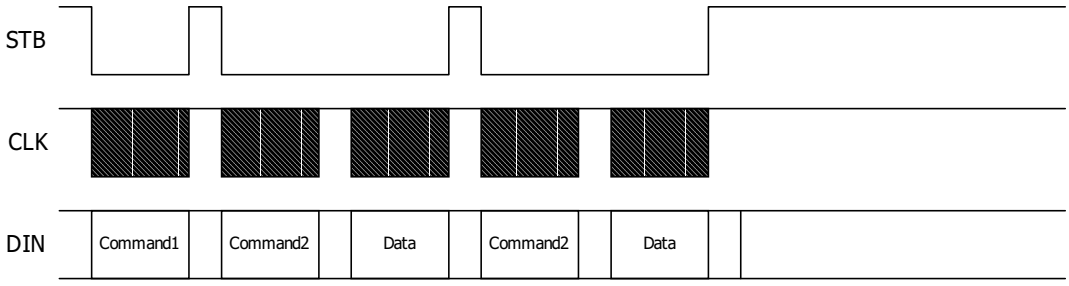
# Application Notes

**Updating display memory by incrementing address.**




Command1: sets display mode
Command2: sets data
Command3: sets address
Data 1 to n : transfers display data (22 bytes max.)
Command4: controls display

**Updating specific address**




Command1: sets data
Command2: sets address
Data: display data