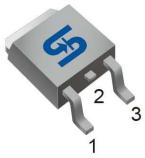
TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM19N20

200V N-Channel Power MOSFET

TO-252 (DPAK)



Pin Definition:
1. Gate
2. Drain
3. Source

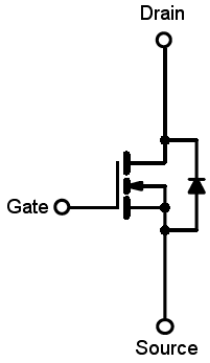
PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
200	92 @ V_{GS} =10V	18

Features

- Advanced Trench Technology
- Low $R_{DS(ON)}$ 92mΩ (Max.)
- Low gate charge typical @ 55nC (Typ.)
- Low Crss typical @ 73pF (Typ.)

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM19N20CP ROG	TO-252	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current @ T_C=25℃	I_D	18	A
Drain Current Pulsed (Note 1)	I_{DM}	72	A
Avalanche Current	I_{AS}	8	A
Avalanche Energy, L=10mH	E_{AS}	320	mJ
Maximum Power Dissipation @ T_C=25℃	P_D	48	W
Storage Temperature Range	T_{STG}	-55 to +150	℃
Operating Junction Temperature Range	T_J	-55 to +150	℃

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R\Theta_{JC}$	2.6	°C/W
Thermal Resistance - Junction to Ambient	$R\Theta_{JA}$	50	°C/W

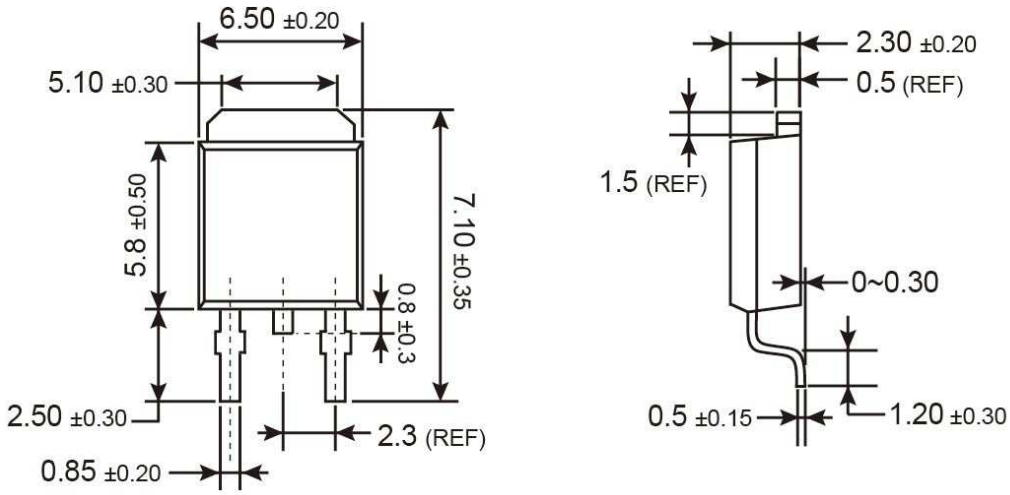
Notes: Surface mounted on FR4 board t ≤ 10sec

Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	200	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 10A	$R_{DS(ON)}$	--	80	92	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	2	--	4	V
Zero Gate Voltage Drain Current	V_{DS} = 160V, V_{GS} = 0V	I_{DSS}	--	--	1	uA
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Dynamic						
Total Gate Charge	V_{DS} = 100V, I_D = 10A, V_{GS} = 10V	Q_g	--	55	--	nC
Gate-Source Charge		Q_{gs}	--	18	--	
Gate-Drain Charge		Q_{gd}	--	17	--	
Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	2300	--	pF
Output Capacitance		C_{oss}	--	145	--	
Reverse Transfer Capacitance		C_{rss}	--	73	--	
Switching						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 100V, R_G = 3Ω	$t_{d(on)}$	--	17	--	nS
Turn-On Rise Time		t_r	--	12	--	
Turn-Off Delay Time		$t_{d(off)}$	--	28	--	
Turn-Off Fall Time		t_f	--	10	--	
Drain-Source Diode Characteristics and Maximum Rating						
Drain-Source Diode Forward Voltage	V_{GS}=0V, I_S=10A	V_{SD}	--	--	1.3	V
Reverse Recovery Time	I_S = 10A, T_J=25°C dI/dt = 100A/us	t_{fr}	--	82	--	nS
Reverse Recovery Charge		Q_{fr}	--	276	--	nC

Notes:
1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. $R\theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R\theta_{JC}$ is guaranteed by design while $R\theta_{CA}$ is determined by the user's board design. $R\theta_{JA}$ shown below for single device operation on FR-4 in still air

TO-252 Mechanical Drawing



Unit: Millimeters

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