UBA2211

Half-bridge power IC family for CFL lamps

Rev. 1 — 28 June 2010 Objective data sheet

1. General description

The UBA2211 family of integrated circuits are a range of high voltage monolithic ICs for driving Compact Fluorescent Lamps (CFL) in half-bridge configurations. The family is specifically designed to provide easy integration of lamp loads across a range of burner power and mains voltages.

Patented technologies and integrated protection types:

- **Preheat state:**
  - Preheat applications: Adjustable current controlled preheat mode technology enables the preheat time (t_{ph}) to be set. This mode is triggered during start up.
  - Non-preheat applications: Glow-time control minimizes electrode damage just after ignition of the lamp.
- **Saturation Current Protection (SCP):** This protection is active during ignition ensuring the lamp inductor can operate at the saturation current limit without exceeding the current ratings of the integrated half-bridge power transistors.
- **RMS current control:** The IC internally calculates the RMS current and changes the frequency (f_{osc}) to ensure the RMS current remains constant. RMS current control is active in the burn state ensuring a constant half-bridge burner current and IC dissipation. The nominal half-bridge burner current is set using the sense resistor (R_{SENSE}).
- **OverTemperature Protection (OTP) and Capacitive Mode Protection (CMP):** Overtemperature and capacitive mode protection monitor the application ensuring, in non-standard conditions, correct system shutdown and a safe condition at the burner's end-of-life.

2. Features and benefits

2.1 System integration

- Integrated half-bridge power transistors
  - UBA2211: generic controller for 220 V markets
  - UBA2211A: 220 V; 13.5 Ω; 0.9 A maximum ignition current
  - UBA2211B: 220 V; 9 Ω; 1.35 A maximum ignition current
  - UBA2211C: 220 V; 6.6 Ω; 1.85 A maximum ignition current
- Integrated bootstrap diode
- Integrated high voltage supply

2.2 Burner lifetime

- Current controlled preheat with adjustable preheat time
- Minimum glow time control to support cold start
- Lamp power independent from mains voltage variations
- Lamp inductor saturation protection during ignition

2.3 Safety

- Overtemperature protection
- Capacitive mode protection
- Overpower control
- System shutdown at burner end of life

2.4 Ease of use

- Adjustable operating frequency for easy fit with various burners
- Each device in the family incorporates the same controller functionality ensuring easy power scaling and roll-out across a complete range of CFLs

3. Applications

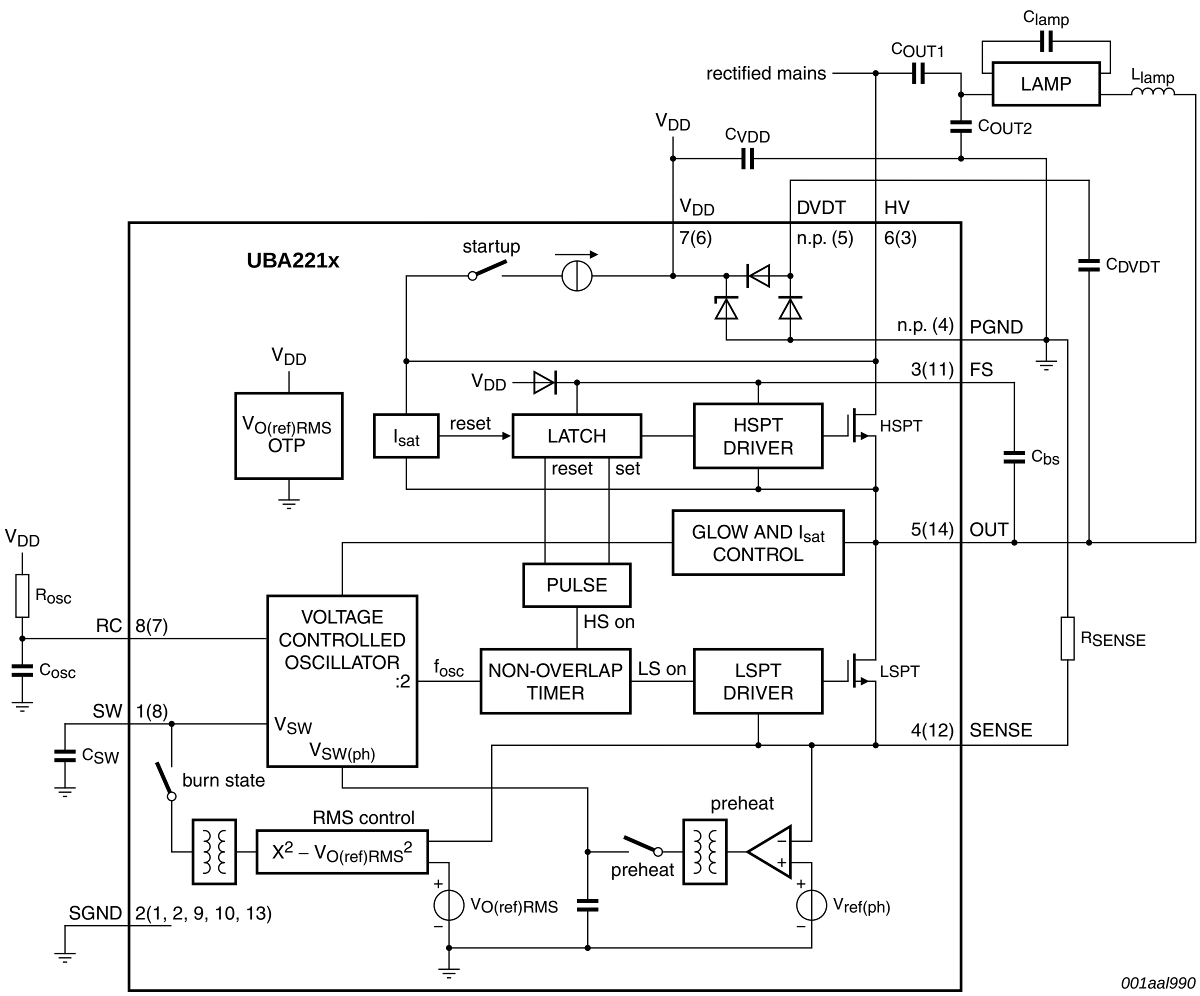
- Compact Fluorescent Lamps up to 25 W for indoor and outdoor applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA2211P/N1	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
UBA2211AP/N1			
UBA2211BP/N1			
UBA2211CP/N1			
UBA2211T/N1	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
UBA2211AT/N1			
UBA2211BT/N1			
UBA2211CT/N1			

5. Block diagram



n.p. in the diagram means not present in DIP8 package

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

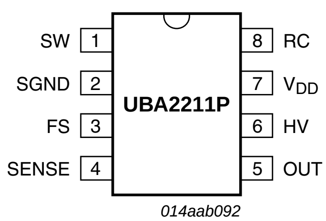


Fig 2. Pin configuration for UBA2211XP (SOT97-1)

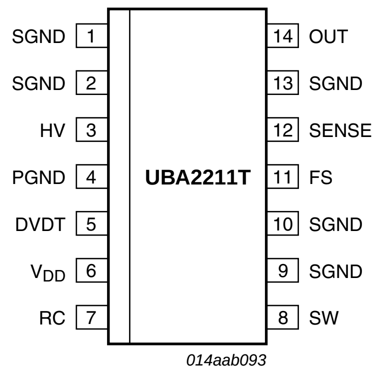


Fig 3. Pin configuration for UBA2211XT (SOT108-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	UBA2211XP	UBA2211XT	
SW	1	8	sweep timing and VCO input
SGND	2	1, 2, 9, 10, 13	signal ground
FS	3	11	high-side floating supply output
SENSE	4	12	voltage sense for preheat and RMS control
OUT	5	14	half-bridge output
HV	6	3	high-voltage supply
V_{DD}	7	6	internal low-voltage supply output
RC	8	7	internal oscillator input
DVDT	n.p.	5	DVDT supply input
PGND	n.p.	4	DVDT supply ground

7. Functional description

7.1 Supply voltage

The UBA2211 family is powered using the start-up current source and the V_{DD} supply. When the voltage on pin HV increases, the V_{DD} capacitor (C_{VDD}) is charged using the internal JFET current source. The voltage on pin V_{DD} rises until V_{DD} equals $V_{DD(start)}$. The start-up current source is then disabled. The half-bridge starts switching causing the charge pump activate and in turn supply V_{DD}.

The amount of current flowing towards V_{DD} equals $V_{HV} \times C_{DVDT} \times f$ where f represents the momentary frequency. The charge pump consists of an external half-bridge capacitor (C_{DVDT}). The SO14 package contains two internal diodes with an internal Zener diode. However, with the DIP8 package, these diodes must be mounted externally. The Zener diode ensures the V_{DD} voltage cannot rise above the maximum V_{DD} rating.

The DVDT supply has its own ground pin (PGND) to prevent large peak currents from flowing through the external small signal ground pin (SGND).

The start-up current source is enabled when the voltage on pin V_{DD} is below $V_{DD(stop)}$.

7.2 Start-up state

When the supply voltage on pin V_{DD} increases, the IC enters the start-up state. In the start-up state the High-Side Power Transistor (HSPT) is switched off and the Low-Side Power Transistor (LSPT) is switched on. The circuit is reset and the capacitors on the bootstrap pin FS (C_{bs}) and the low-voltage supply pin V_{DD} (C_{VDD}) are charged. Pins RC and SW are switched to ground.

When pin V_{DD} is above $V_{DD(start)}$, the start-up state is exited and the preheat state is entered. If the voltage on pin V_{DD} falls below $V_{DD(stop)}$, the system returns to the start-up state.

Remark: If OTP is active, the IC remains in the start-up state for as long as this is the case. The V_{DD} voltage slowly oscillates between $V_{DD} = V_{DD(stop)}$ and $V_{DD} = V_{DD(start)}$.

7.3 Reset

A DC reset circuit is incorporated in the high-side driver. The high-side transistor is switched off when the voltage on pin FS is below the high-side lockout voltage.

7.4 Oscillation control

The oscillation frequency is based on the 555-timer function. A self oscillating circuit is created comprising the external components: resistors R_{osc}, R_{SENSE} and capacitor C_{osc}. The nominal oscillating frequency is determined by R_{osc} and C_{osc}.

An internal divider $0.5 \times f_{osc(int)}$ is used to generate the accurate 50 % duty cycle. The divider sets the bridge frequency at half the oscillator frequency.

Signal V_{SW} is generated by the input on pin SW and it is used to determine the frequency in all states except preheat. Signal $V_{SW(ph)}$ is an internally generated signal used to determine the frequency during the preheat state.

The output voltage of the bridge changes with the falling edge of the signal on pin RC. The nominal half-bridge frequency is shown in Equation 1:

$$f_{osc(nom)} = \frac{1}{k_{osc} \times R_{osc} \times C_{osc}} \tag{1}$$

The maximum frequency is 2.5 × $f_{osc(nom)}$ and is set at V_{SW}. An overview of the oscillator, internal LSPT and HSPT drive signals and the output is shown in Figure 4.

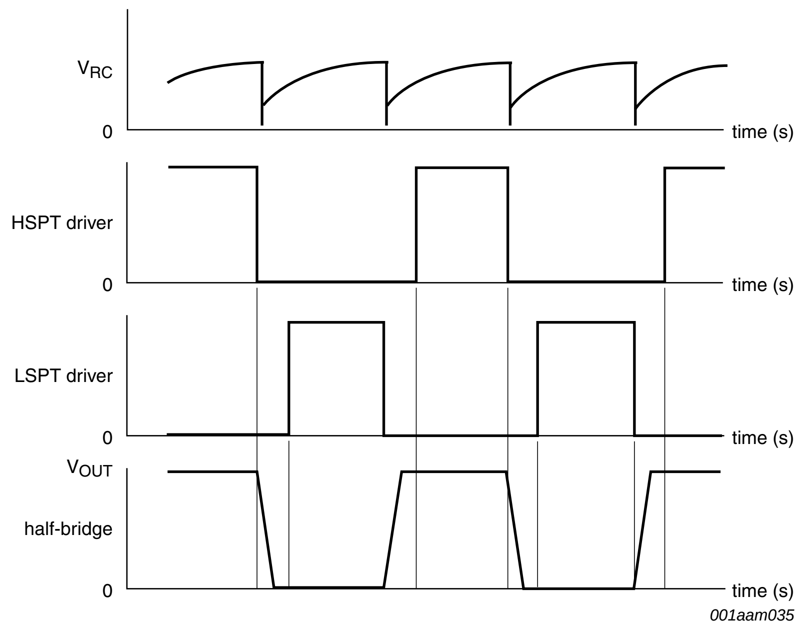


Fig 4. Oscillator, HSPT/LSPT drivers and output signals

7.5 Preheat state

As described in Section 7.2, the IC enters the preheat state when the voltage on pin V_{DD} is above $V_{DD(start)}$ and OTP is not active. The capacitor on pin SW (C_{SW}) is charged by the sweep current (I_{SW}). The preheat Operational Transconductance Amplifier (OTA) is enabled and the half-bridge circuit starts oscillating.

The preheat current is monitored using the external R_{SENSE} resistor. The OTA controls the frequency using output voltage $V_{SW(ph)}$ so that the peak voltage across R_{SENSE} equals the internal reference voltage ($V_{ref(ph)}$). The peak voltage is the voltage at the end of the LSPT conduction time. The preheat peak current through the lamp filament is calculated as shown in Equation 2:

$$I_{ph(peak)} = \frac{V_{ref(ph)}}{R_{SENSE}} \tag{2}$$

The preheat time is set by the external capacitor (C_{SW}). The preheat state ends when the down-going C_{SW} voltage equals $V_{SW(ph)}$; see Figure 4.

If during the preheat time, capacitive mode is sensed, the internal V_{SW} HIGH node is discharged and the frequency sweep restarts at f_{max}.

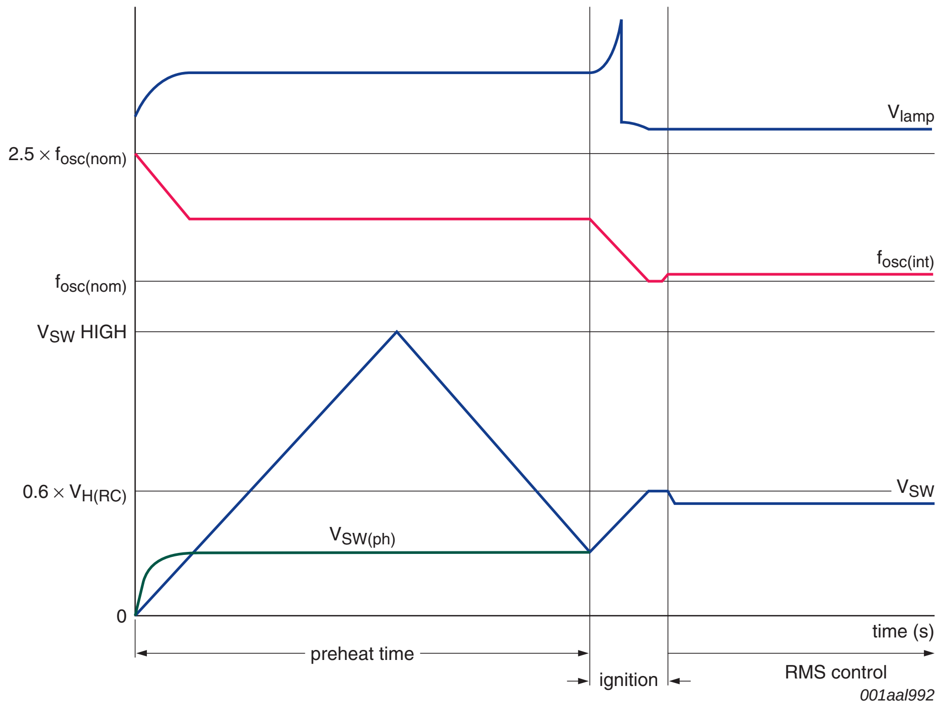


Fig 5. $f_{osc(nom)}$, V_{SW}, $V_{SW(ph)}$ **and** V_{lamp} **plotted against time**

7.6 Ignition state

The ignition state is entered after the preheat state has finished. The capacitor on pin SW (C_{SW}) is charged by I_{SW} up to $0.6 \times V_{H(RC)}$ which corresponds to the frequency $f_{osc(nom)}$.

During this frequency sweep, the resonance frequency is reached resulting in the ignition of the lamp (see Figure 4). The resonance frequency is set by the lamp inductor (L_{lamp}) and lamp capacitor (C_{lamp}). The ignition state ends when the voltage on pin SW (V_{SW}) reaches $0.6 \times V_{H(RC)}$.

7.7 Steady state

In the steady state, the RMS current control is active. This control sets the frequency so that the RMS voltage across the sense resistor (R_{SENSE}) is equal to $V_{O(ref)RMS}$. This ensures the current through the power switches and through the lamp is constant. This results in constant IC dissipation and temperature at a fixed ambient temperature.

During one oscillator clock cycle, the voltage on pin SENSE (V_{SENSE}) is squared and converted into a positive current. This discharge current is added to the capacitor C_{SW}.

During the other oscillator clock cycle, the input of the squarer is connected to the internal reference voltage $V_{O(ref)RMS}$. This voltage is squared and converted into a negative current. This charge current is also added to capacitor C_{SW}. When both currents are equal, then Equation 3 is true:

$$\frac{1}{T_{osc}} \times \int_{0}^{T_{osc}} V_{SENSE^2(t)DT} = \frac{1}{T_{osc}} \times \int_{0}^{T_{osc}} V_{O(ref)RMS^2 DT} \quad (3)$$

Where T_{osc} equals the operating frequency f_{osc} / 1.

Taking the square root of both sides results in Equation 4:

$$\sqrt{\frac{1}{T_{osc}} \times \int_{0}^{T_{osc}} V_{SENSE^2(t)DT}} = \sqrt{\frac{1}{T_{osc}} \times \int_{0}^{T_{osc}} V_{O(ref)RMS^2 DT}} \quad (4)$$

or

$$RMS\ V_{SENSE} = V_{O(ref)RMS} = R_{SENSE} \times I_{LSPT} \quad (5)$$

A constant current flows through the power switches and the lamp which is defined by the internal reference voltage ($V_{O(ref)RMS}$) and the external R_{SENSE} resistor.

7.8 Non-overlap time

The non-overlap time is defined as the time when both MOSFETs are not conducting. The non-overlap time is fixed internally.

7.9 OverTemperature Protection (OTP)

OTP is active in all states. When the die temperature reaches the OTP activation threshold ($T_{th(act)otp}$), the oscillator is stopped and the power switches (LSPT/HSPT) are set to the startup state. When the oscillator is stopped, the DVDT supply no longer generates the supply current I_{DVDT}. Voltage V_{DD} gradually decreases and the start-up state is entered as described in Section 7.2 on page 5. OTP is reset when the temperature < $T_{th(rel)otp}$.

7.10 Minimum glow time control

If the preheat time is set too short or omitted, the lamp electrodes do not have the correct temperature in the ignition state. This results in instant light but also in a reduced switching lifetime because when the electrode temperature is too low electrode sputtering and damage occur. The minimum glow time control minimizes electrode damage by ensuring maximum power use during the glow phase to heat the electrodes heat as quickly as possible (see Figure 6).

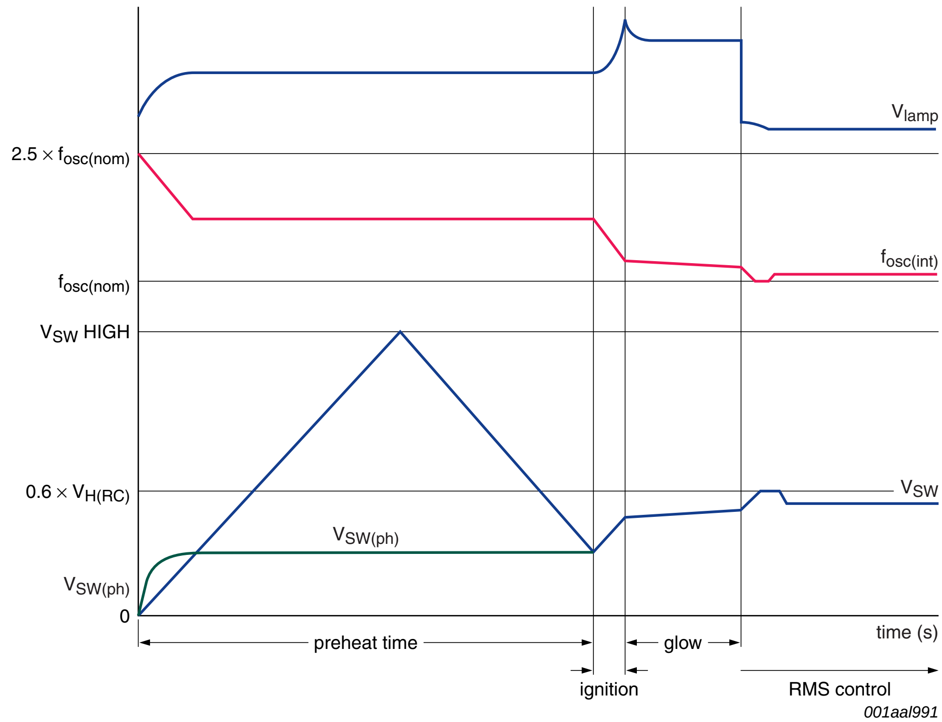


Fig 6. **$f_{osc(nom)}$, V_{SW}, $V_{SW(ph)}$ and V_{lamp} plotted against time. The glow time control is active as t_{ph} is too short to preheat the electrodes**

7.11 Saturation Current Protection (SCP)

A critical parameter in the design of the lamp inductor is its saturation current. When the momentary inductor exceeds its saturation current, the inductance drops significantly. If this happens, the inductor current and the current flowing through the LSPT and HSPT power switches increases rapidly. This can cause the current to exceed the half-bridge power transistors maximum ratings.

Saturation of the lamp inductor is likely to occur in cost-effective and miniaturized CFLs. The UBA2211 family internally monitors the power transistor current. When this current exceeds the momentary rating of the internal half-bridge power transistors, the conduction time is reduced and the frequency is slowly increased (by discharging C_{SW}). This causes the system to balance at the edge of the current rating of the power switches.

7.12 Capacitive Mode Protection (CMP)

When capacitive mode is detected, capacitor C_{SW} is discharged causing the frequency to increase. The system sets itself to the operating point where capacitive mode switching is minimized. CMP is active during the ignition state and in the steady state.

If capacitive mode is sensed during the preheat time, the oscillator restarts at f_{max}. CMP could be triggered by an end of lamp life condition when a lamp electrode is broken.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{HV}	voltage on pin HV	operating		-	373	V
		mains transients during 0.5 s		-	550	V
V_{FS}	voltage on pin FS			V_{HV}	V_{HV} + 14	V
V_{DD}	supply voltage	DC supply		0	14	V
V_{SENSE}	voltage on pin SENSE			–5	+5	V
V_{RC}	voltage on pin RC	I_{RC} < 1 mA		0	V_{DD}	V
V_{SW}	voltage on pin SW	I_{SW} < 1 mA		0	V_{DD}	V
I_{OUT}	current on pin OUT	T_j < 125 °C	[1]			
		UBA2211AX		–0.9	+0.9	A
		UBA2211BX		–1.35	+1.35	A
		UBA2211CX		–1.65	+1.65	A
I_{DVDT}	current on pin DVDT	T_j < 125 °C		–0.9	+0.9	A
SR	slew rate	repetitive output on pin OUT		–4	+4	V/ns
T_j	junction temperature			–40	+150	°C
T_{amb}	ambient temperature			–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM:	[2]			
		pins HV, FS, OUT		-	1000	V
		pins SW, RC, VDD, DVDT		-	2500	V
		MM:	[3]			
		all pins		-	250	V

[1] X where the last letter is P or T.

[2] In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[3] In accordance with the Machine Model (MM): equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor and a 0.75 μH inductor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	95	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	[1]	16	K/W

[1] In accordance with IEC 60747-1

10. Characteristics

Table 5. Characteristics

T_j = 25 °C; all voltages are measured with respect to SGND; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-voltage supply							
V_{HV}	voltage on pin HV	t < 0.5 s; I_{HV} < 30 mA		0	-	550	V
V_{FS}	voltage on pin FS	t < 0.5 s; I_{HV} < 30 mA		0	-	564	V
Low-voltage supply							
Start-up state							
I_{HV}	current on pin HV	V_{HV} = 100 V		-	0.85	-	mA
$V_{DD(start)}$	start supply voltage	oscillation start		10.7	11.7	12.7	V
$V_{DD(stop)}$	stop supply voltage	oscillation stop		8	8.5	9	V
$V_{DD(hys)}$	hysteresis of supply voltage	start – stop		3	3.5	4	V
$V_{DD(reg)}$	regulation supply voltage			-	12	-	V
I_{sink}	sink current	capability of VDD regulator		6	-	-	mA
Output stage							
R_{on}	on-state resistance	high-side transistor:	[1]				
		UBA2211AX; V_{HV} = 310 V; I_D = 100 mA		-	13.5	-	Ω
		UBA2211BX; V_{HV} = 310 V; I_D = 100 mA		-	9.3	-	Ω
		UBA2211CX; V_{HV} = 310 V; I_D = 100 mA		-	6.6	-	Ω
		low-side transistor:	[1]				
		UBA2211AX; I_D = 100 mA		-	13.5	-	Ω
		UBA2211BX; I_D = 100 mA		-	8.2	-	Ω
		UBA2211CX; I_D = 100 mA		-	6.6	-	Ω
V_{Fd}	diode forward voltage	high-side transistor body; I_F = 100 mA		-	1.3	-	V
		low-side transistor body; I_F = 100 mA		-	1.3	-	V
$V_{Fd(bs)}$	bootstrap diode forward voltage	I_F = 1 mA		-	1.1	-	V
t_{no}	non-overlap time			1.05	1.35	1.65	µs
V_{FS}	voltage on pin FS	lockout voltage		3.6	4.2	4.8	V
I_{FS}	current on pin FS	V_{HV} = 310 V; V_{FS} = 12 V		10	14	18	µA

Table 5. Characteristics *…continued*

T_j = 25 °C; all voltages are measured with respect to SGND; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{sat}	saturation current	high-side transistor:	[1]				
		UBA2211AX; V_{DS} = 30 V; $T_j \leq$ 125 °C; V_{HV} = 310 V		0.90	-	-	A
		UBA2211BX; V_{DS} = 30 V; $T_j \leq$ 125 °C; V_{HV} = 310 V		1.35	-	-	A
		UBA2211CX; V_{DS} = 30 V; $T_j \leq$ 125 °C; V_{HV} = 310 V		1.85	-	-	A
		low-side transistor:	[1]				
		UBA2211AX; V_{DS} = 30 V; $T_j \leq$ 125 °C		0.90	-	-	A
		UBA2211BX; V_{DS} = 30 V; $T_j \leq$ 125 °C		1.35	-	-	A
		UBA2211CX; V_{DS} = 30 V; $T_j \leq$ 125 °C		1.85	-	-	A
Internal oscillator							
$f_{osc(int)}$	internal oscillator frequency	$V_{SW} = V_{DD}$		-	-	60	kHz
$f_{osc(nom)}$	nominal oscillator frequency	R_{osc} = 100 kΩ; C_{osc} = 220 pF; $V_{SW} = V_{DD}$		40.05	41.32	42.68	kHz
$\Delta f_{osc(nom)}/\Delta T$	nominal oscillator frequency variation with temperature	R_{osc} = 100 kΩ; C_{osc} = 220 pF; ΔT = –20 to +150 °C		-	2	-	%
k_H	high-level trip point factor			0.371	0.384	0.397	
k_L	low-level trip point factor			0.028	0.032	0.036	
$V_{H(RC)}$	HIGH-level voltage on pin RC	trip point; $V_{H(RC)} = k_H \times V_{DD}$		4.08	4.22	4.37	V
$V_{L(RC)}$	LOW-level voltage on pin RC	trip point; $V_{L(RC)} = k_l \times V_{DD}$		0.308	0.352	0.396	V
K_{osc}	oscillator constant	R_{osc} = 100 kΩ; C_{osc} = 220 pF		1.065	1.1	1.135	
Preheat function							
$V_{ref(ph)}$	preheat reference voltage			-	500	-	mV
t_{ph}	preheat time	C_{SW} = 100 nF		-	1.2	-	s
RMS current control function							
$V_{O(ref)RMS}$	RMS reference output voltage			262	285	308	mV
OTP function							
$T_{th(act)otp}$	overtemperature protection activation threshold temperature			155	175	190	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature			85	100	115	°C

[1] X where the last letter is P or T.

11. Application information

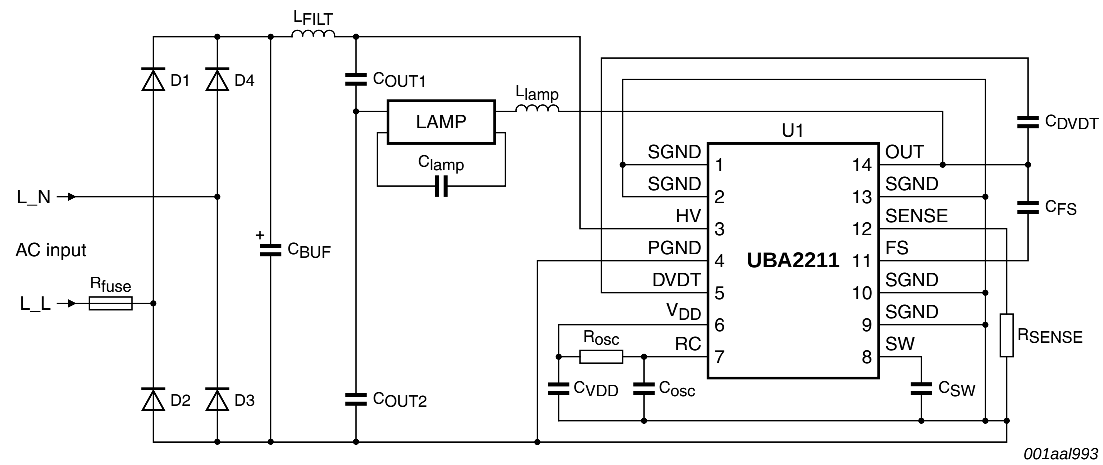
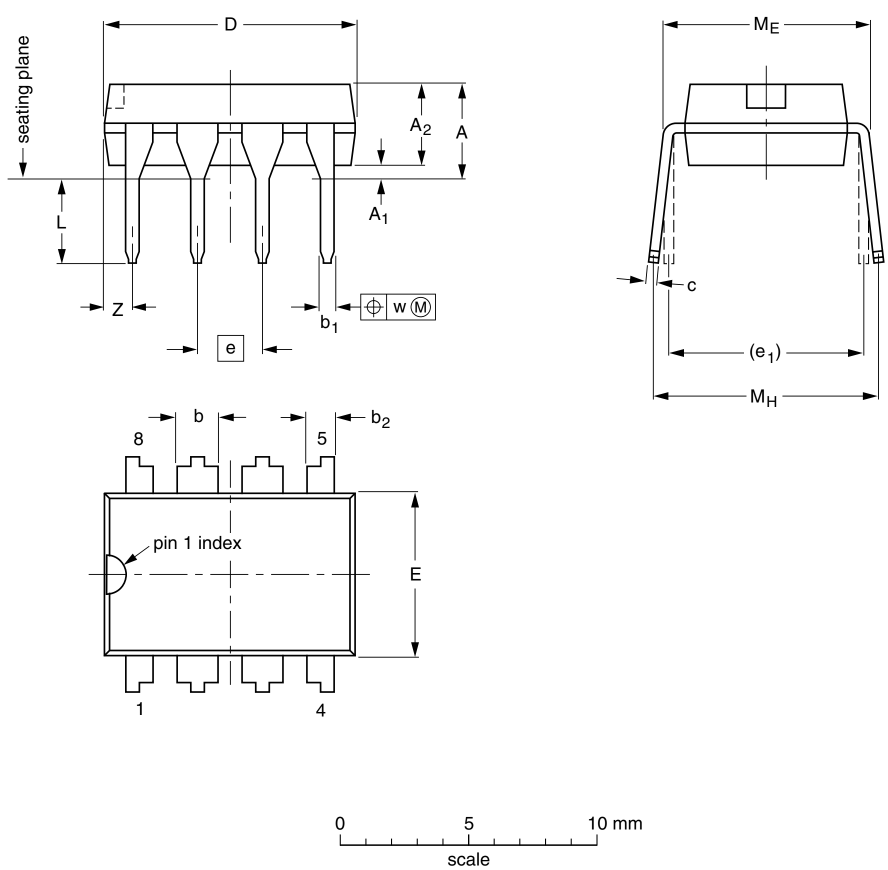


Fig 7. Application diagram

12. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

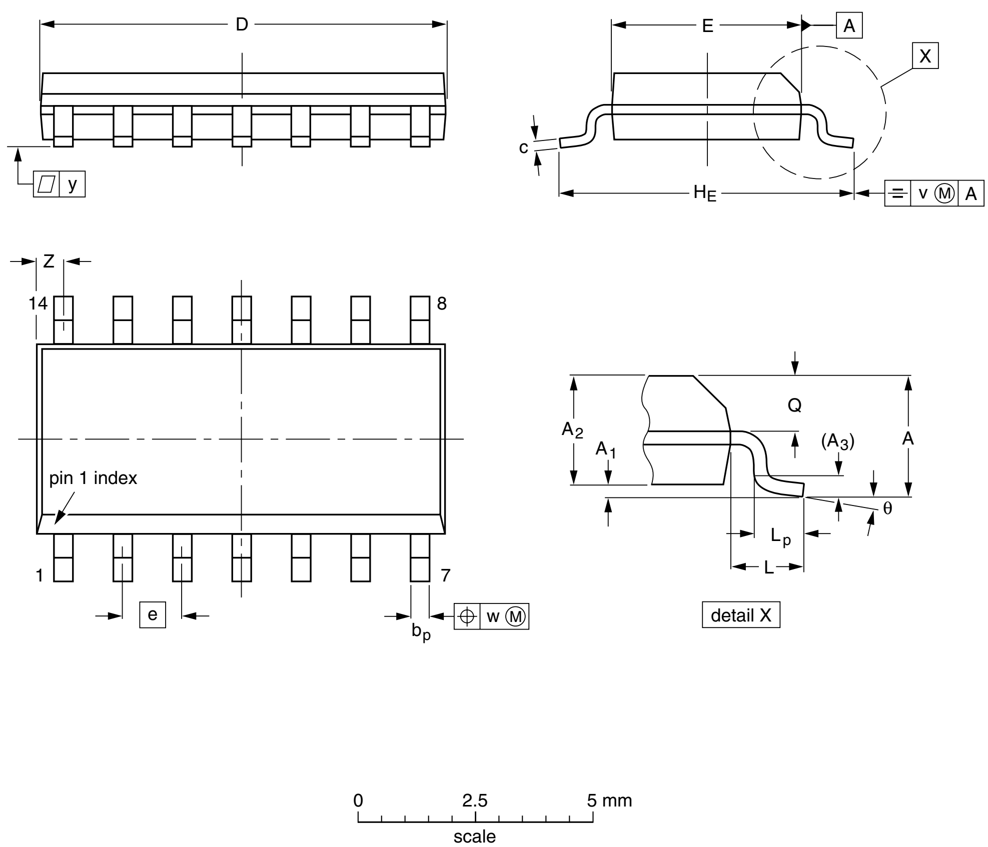
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT97-1 (DIP8)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2211 v1	20100628	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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