ROHM

STRUCTURE Silicon monolithic integrated circuits

PRODUCT SERIES 3-phase blushless motor driver for polygon mirror motor

TYPE **BD6406FM**

FUNCTION
- 3-phase MOS direct PWM drive
- Built-in PLL control circuit
- Built-in Power save(Hall bias)
- Built-in Over current protect

○Absolute maximum ratings (Ta=25℃)

Item	Symbol	Limit	Unit
Supply voltage	V_{CC}	36	V
LD pin applied voltage	V_{LD}	33	V
FG pin applied voltage	V_{FG}	7	V
Power dissipation	P_d	2200 *1	mW
Hall signal input voltage	V_{HALL}	7	V
Input voltage for control pin (CLK, SS, SB)	V_{CTL}	7	V
Maximum output current	I_{OUT}	2000 *2	mA
Operating temperature range	T_{opr}	-25～+75	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	150	℃

*1 70mm×70mm×1.6mm glass epoxy board. Derating is done at 17.6mW/℃ for operating above Ta=25℃.

*2 Do not, however exceed Pd, ASO and Tjmax=150℃.

○Operating Condition(Ta=-25～+75℃)

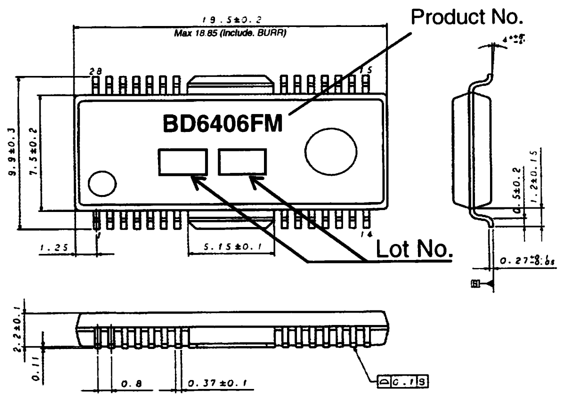
Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	18	24	28	V
5V constant voltage output current	I_{REG}	0	-	20	mA
HB pin input current	I_{HB}	0	-	20	mA
LD pin applied voltage	I_{HB}	0	-	30	V
LD pin output current	V_{LD}	0	-	15	mA
FG pin applied voltage	I_{LD}	0	-	5	V
FG pin output current	V_{FG}	0	-	15	mA

This product described in this specification isn't judged whether it applies to COCOM regulations.
Please confirm in case of export.
This product isn't designed for protection against radioactive rays.

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply voltage1	I_{CC1}	2.6	4.3	6.0	mA	SS="LOW"
Supply voltage2	I_{CC2}	2.5	4.2	5.9	mA	SS="HIGH"
5V constant voltage output						
Output voltage	V_{REG}	4.65	5.00	5.35	V	
Output, Block						
Output ON resistance	$R_{ON(H+L)}$	-	2.0	2.6	Ω	1.0A total of high and low sides
Forward voltage of diode on low side	V_{D1}	0.70	1.10	1.55	V	I_{OUT}=-1.0A
Forward voltage of diode on high side	V_{D2}	0.70	1.10	1.55	V	I_{OUT}=1.0A
Hall comparator						
In-phase input voltage range	V_{ICM}	1.5	-	3.5	V	
Hysteresis width	ΔV_{IN}	15	24	42	mV	
FG output						
Low output voltage	V_{FGL}	-	0.15	0.50	V	I_{FG}=10mA
Phase comparison output						
High output voltage	V_{PDH}	4.45	4.9	-	V	I_{PD}=-100μA
Low output voltage	V_{PDL}	-	0.2	0.3	V	I_{PD}=100μA
LD output						
Low output voltage	V_{LDL}	-	0.15	0.50	V	I_{LD}=10mA
Integral amplifier						
High output voltage	V_{ERH}	3.5	4.1	-	V	I_{EO}=-500μA
Current limiting circuit						
Limiter voltage	V_{RNF}	0.450	0.5	0.550	V	
CLK pin						
External input frequency	F_{CKI}	0.1	-	10	KHz	
High level input voltage	V_{CKIH}	3.0		5.0	V	CLK="HIGH"
Low level input voltage	V_{CKIL}	0	-	1.5	V	CLK="LOW"
Low level input current	I_{CKIL}	-75	-50	-25	μA	CLK="LOW"
SS pin						
High level input voltage	V_{SSIH}	3.0	-	5	V	SS="HIGH"
Low level input voltage	V_{SSIL}	0	-	1.5	V	SS="LOW"
Low level input current	I_{SSIL}	-75	-50	-25	μA	SS="LOW"
SB pin						
High level input voltage	V_{SBIH}	3.0	-	5	V	SS="HIGH" Free run
Low level input voltage	V_{SBIL}	0	-	1.5	V	SB="LOW" Short Brake
Low level input current	I_{SBIL}	-75	-50	-25	μA	SB="LOW"
PWM						
Oscillating frequency	F_{PWM}	130	200	270	KHz	C_{PWM}=220pF
PRO_CLK						
CLK cycle for protection circuit	T_{PCLK}	13	20	27	msec	C_{PRO_CLK}=0.1μF
Hall bias						
Hall bias voltage	V_{HB}	0.65	0.8	0.95	V	I_{HB}=10mA

○Package outline



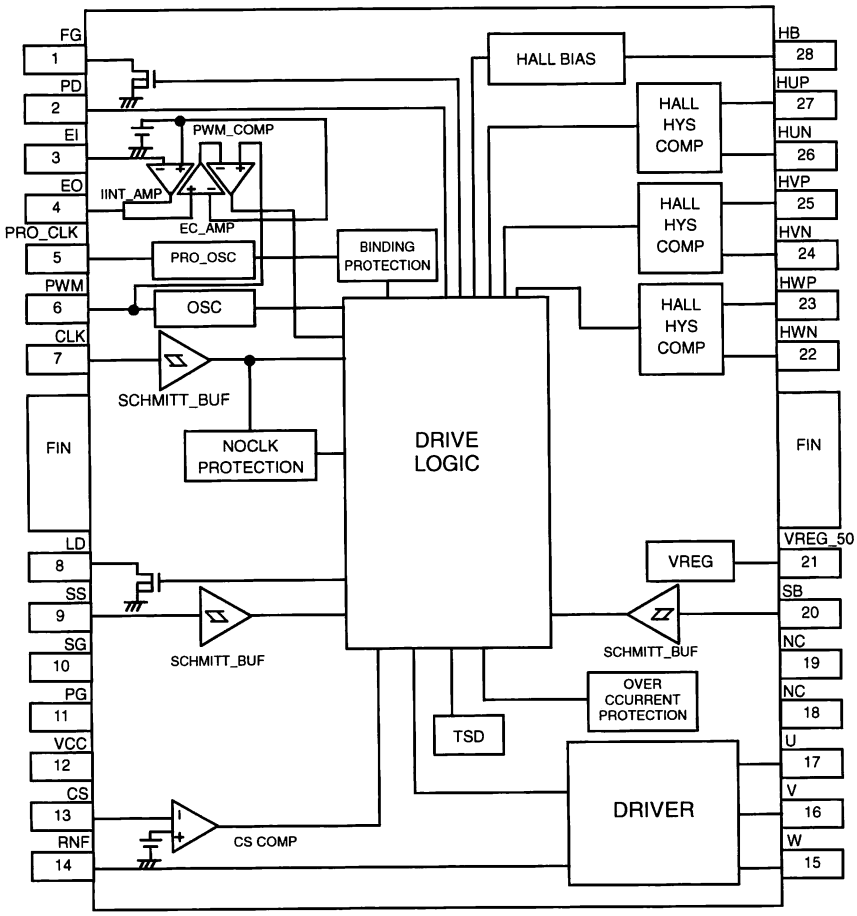
HSOP-M28 (Unit: mm)

○Pin No / Pin name

Pin No	Pin name	Pin No	Pin name
1	FG	15	W
2	PD	16	V
3	EI	17	U
4	EO	18	NC
5	PRO_CLK	19	NC
6	PWM	20	SB
7	CLK	21	VREG_50
FIN	GND	FIN	GND
8	LD	22	HWN
9	SS	23	HWP
10	SG	24	HVN
11	PG	25	HVP
12	VCC	26	HUN
13	CS	27	HUP
14	RNF	28	HB

NC : Non Connection

○Block diagram



○Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC is equipped with FIN heat dissipation terminals, but dissipation efficiency can be improved by applying heat dissipation treatment in this area. It is important to consider actual usage conditions and to take as large a dissipation pattern as possible.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

Notes

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