FAIRCHILD SEMICONDUCTOR®

June 2013

FDMC8360L

N-Channel Shielded Gate Power Trench® MOSFET

40 V, 80 A, 2.1 mΩ

Features

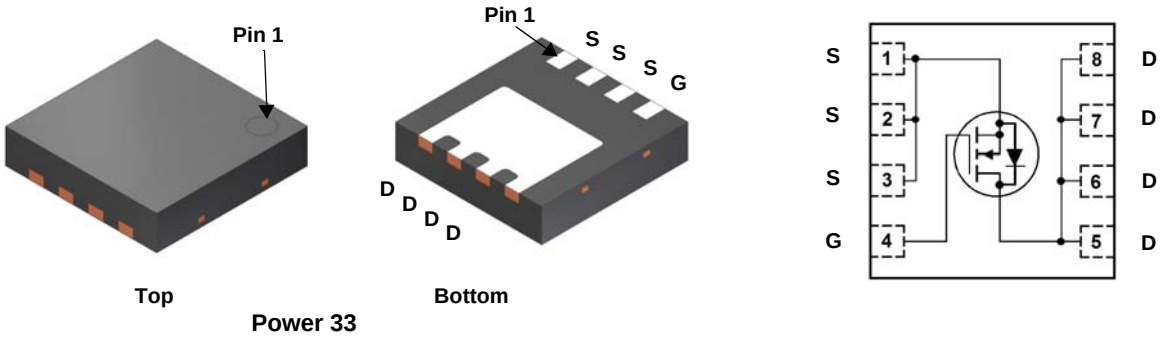
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 2.1 mΩ at V_{GS} = 10 V, I_D = 27 A
- Max $r_{DS(on)}$ = 3.1 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion



Top Bottom

Power 33

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				40	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	-Continuous	T_C = 25 °C		80	A
		-Continuous	T_A = 25 °C	(Note 1a)	27	
		-Pulsed		(Note 4)	240	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	294	mJ
P_D	Power Dissipation		T_C = 25 °C		54	W
	Power Dissipation		T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8360L	FDMC8360L	Power33	13 ”	12 mm	3000 units

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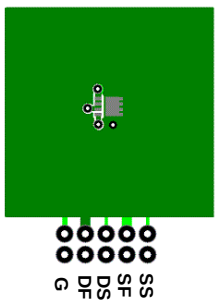
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 27 A		1.6	2.1	mΩ
		V_{GS} = 4.5 V, I_D = 22 A		2.3	3.1	
		V_{GS} = 10 V, I_D = 27 A, T_J = 125 °C		2.2	2.9	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 27 A		138		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		4140	5795	pF
C_{oss}	Output Capacitance			1230	1725	pF
C_{rss}	Reverse Transfer Capacitance			36	60	pF
R_g	Gate Resistance		0.1	0.9	2.7	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 27 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		15	28	ns
t_r	Rise Time			6.7	14	ns
$t_{d(off)}$	Turn-Off Delay Time			38	60	ns
t_f	Fall Time			5.3	11	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 20 V, I_D = 27 A		57	80	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 20 V, I_D = 27 A		26	37	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 27 A		11		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 20 V, I_D = 27 A		5.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 27 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 27 A, di/dt = 100 A/μs		49	80	ns
Q_{rr}	Reverse Recovery Charge			29	46	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 294 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 14 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 44 A.

4. Pulsed Id limited by junction temperature, td<=100 μS, please refer to SOA curve for more details.

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Typical Characteristics T_J = 25 °C unless otherwise noted

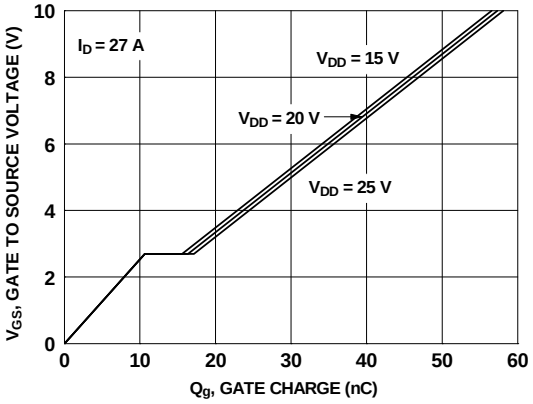


Figure 7. Gate Charge Characteristics

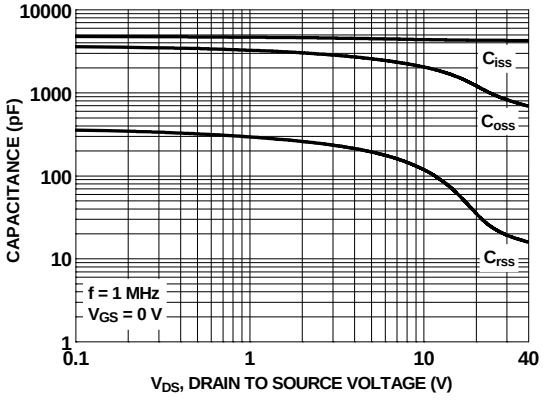


Figure 8. Capacitance vs Drain to Source Voltage

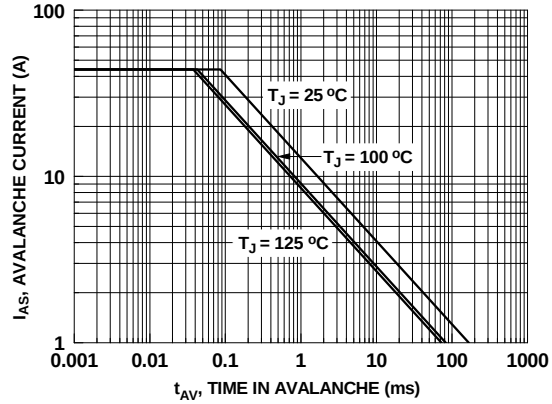


Figure 9. Unclamped Inductive Switching Capability

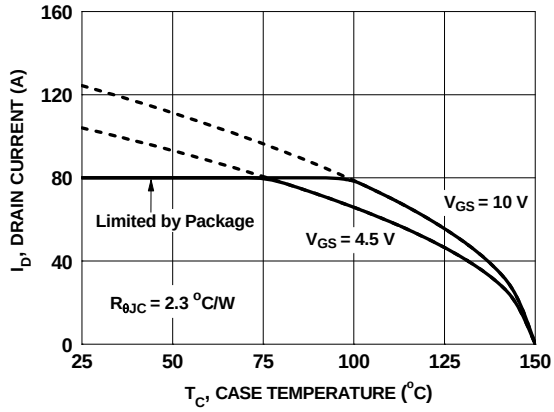


Figure 10. Maximum Continuous Drain Current vs Case Temperature

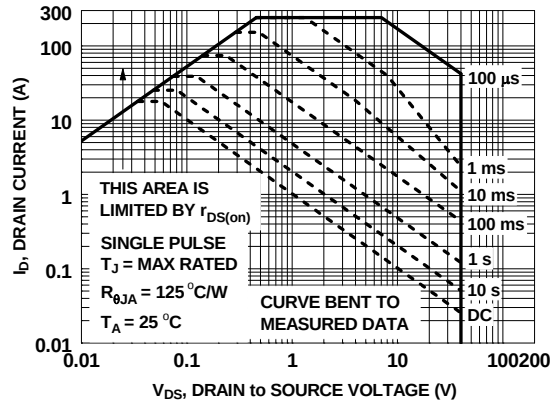


Figure 11. Forward Bias Safe Operating Area

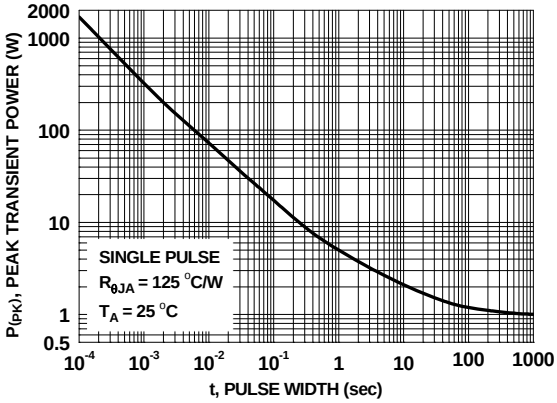
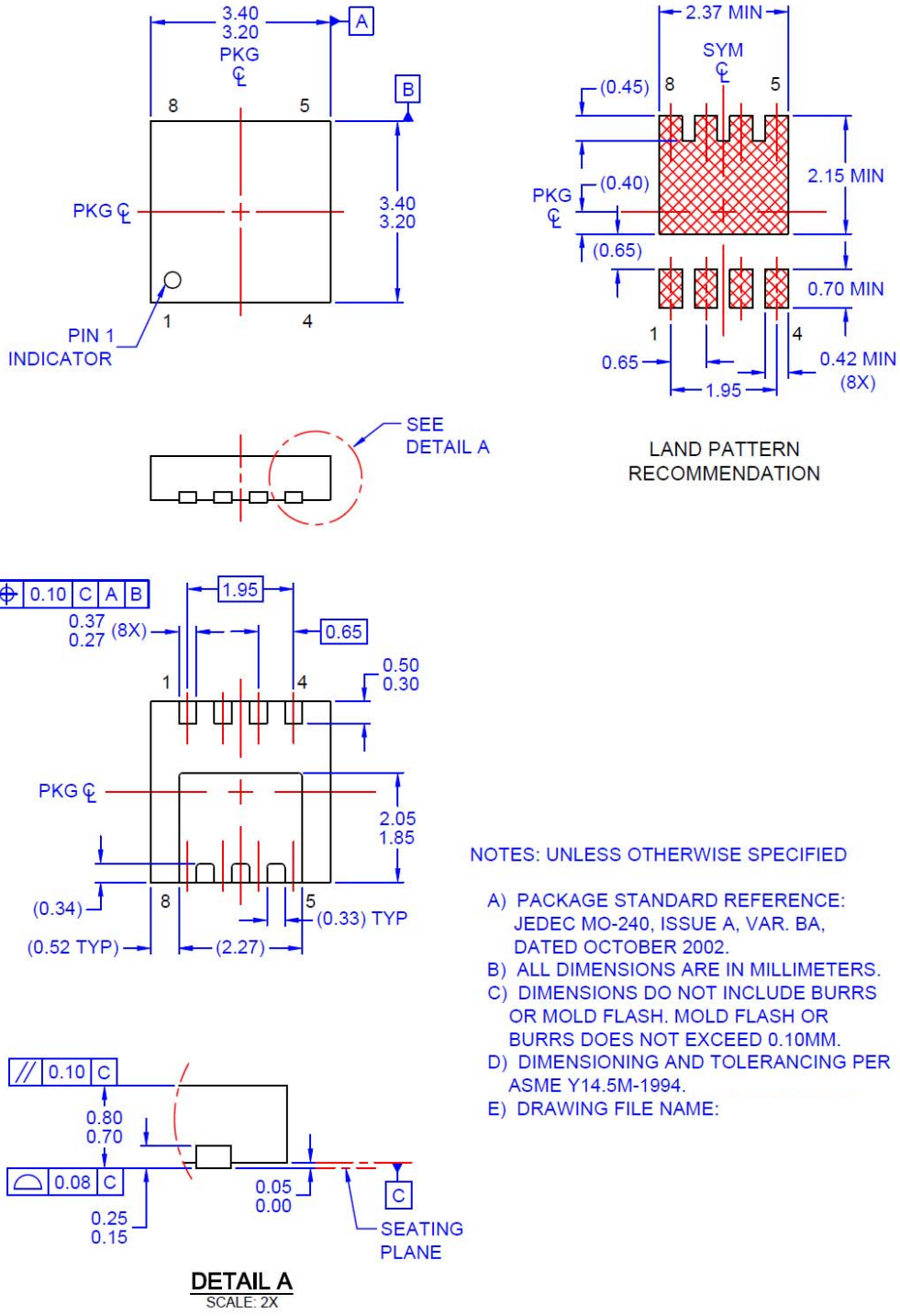


Figure 12. Single Pulse Maximum Power Dissipation

Dimensional Outline and Pad Layout



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D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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