MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

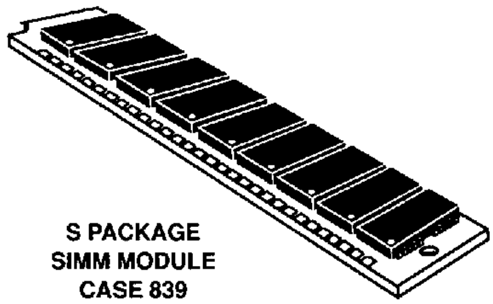
T-46-23-18

MCM94000A
MCM9L4000A

Advance Information

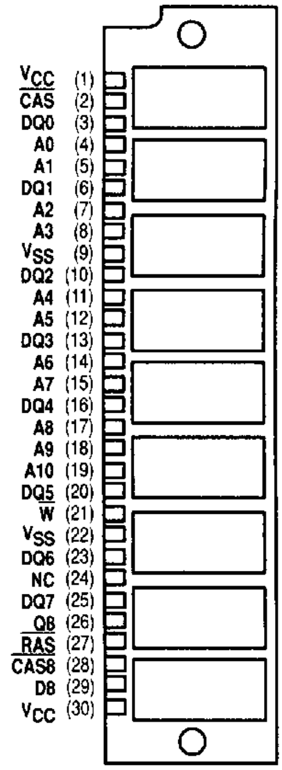
4Mx9 Bit Dynamic Random Access Memory Module

The MCM94000AS is a 36M, dynamic random access memory (DRAM) module organized as 4,194,304 × 9 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of nine MCM54100A DRAMs housed in a 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54100A is a CMOS high speed, dynamic random access memory organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology.



S PACKAGE
SIMM MODULE
CASE 839

30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM94000AS/9L4000AS)

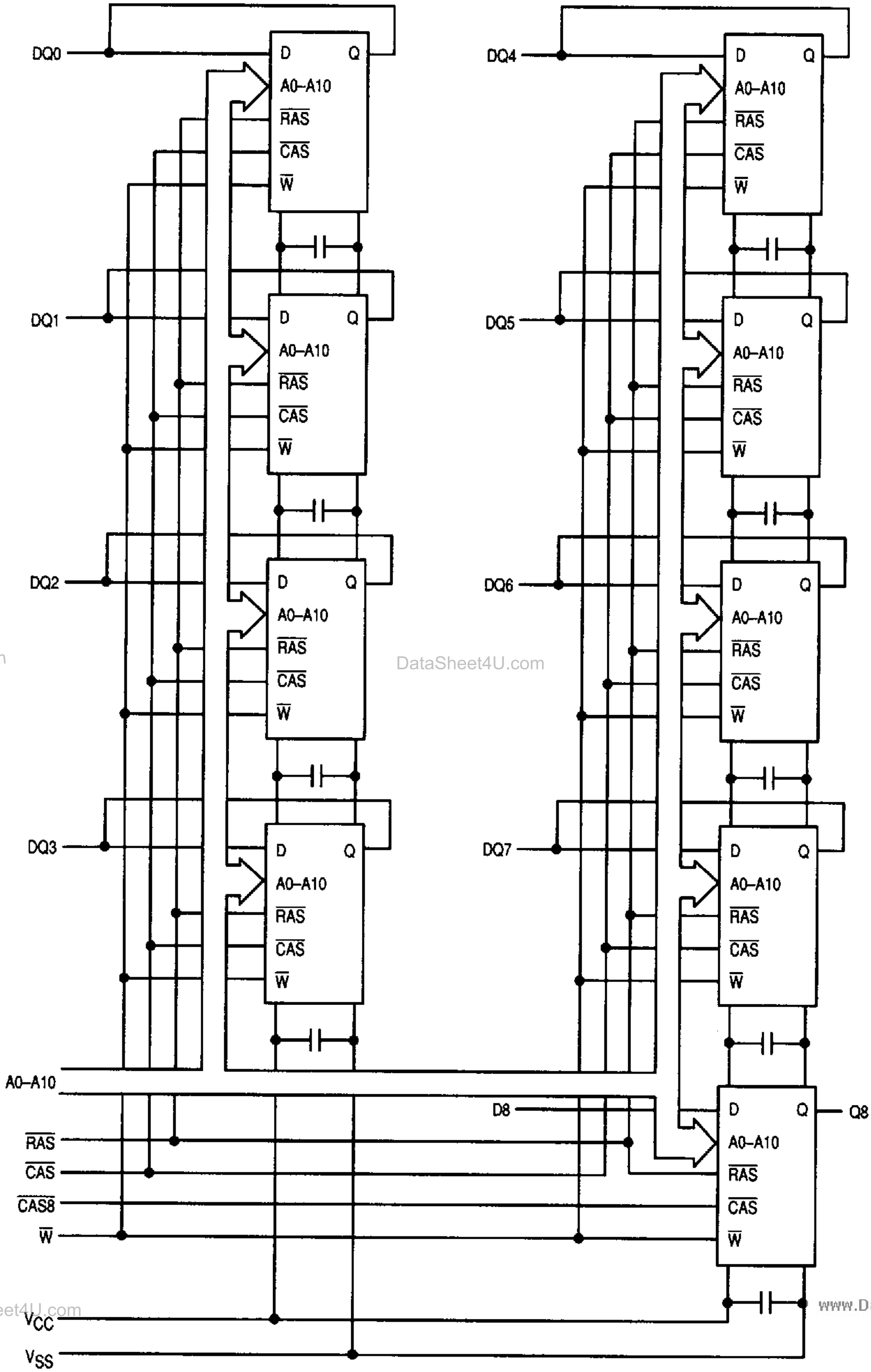


- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM94000A = 16 ms
  MCM9L4000A = 128 ms
- Consists of Nine 4M × 1 DRAMs and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM94000AS-60 = 60 ns (Max)
  MCM94000AS-70 = 70 ns (Max)
  MCM94000AS-80 = 80 ns (Max)
  MCM94000AS-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM94000AS-60 and MCM9L4000AS-60 = 5.94 W (Max)
  MCM94000AS-70 and MCM9L4000AS-70 = 4.95 W (Max)
  MCM94000AS-80 and MCM9L4000AS-80 = 4.21 W (Max)
  MCM94000AS-10 and MCM9L4000AS-10 = 3.72 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 99 mW (Max)
  CMOS Levels (MCM94000A) = 50 mW (Max)
  (MCM9L4000A) = 10 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM94000AS), Pin Connector (MCM94000L, or Low Height Pin Connector (MCM94030LH)

PIN NAMES	
A0–A10	Address Inputs
DQ0–DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	–1 to +7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.3	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	–1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM94000A-60, t_{RC} = 110 ns		—	1080		
MCM94000A-70, t_{RC} = 130 ns		—	900		
MCM94000A-80, t_{RC} = 150 ns		—	765		
MCM94000A-10, t_{RC} = 180 ns		—	675		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}			mA	2
MCM94000A-60, t_{RC} = 110 ns		—	1080		
MCM94000A-70, t_{RC} = 130 ns		—	900		
MCM94000A-80, t_{RC} = 150 ns		—	765		
MCM94000A-10, t_{RC} = 180 ns		—	675		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2, 3
MCM94000A-60, t_{PC} = 45 ns		—	540		
MCM94000A-70, t_{PC} = 45 ns		—	540		
MCM94000A-80, t_{PC} = 50 ns		—	450		
MCM94000A-10, t_{PC} = 60 ns		—	405		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM94000A	I_{CC5}	—	9	mA	
MCM9L4000A		—	1.8		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM94000A-60, t_{RC} = 110 ns		—	1080		
MCM94000A-70, t_{RC} = 130 ns		—	900		
MCM94000A-80, t_{RC} = 150 ns		—	765		
MCM94000A-10, t_{RC} = 180 ns		—	675		
V_{CC} Power Supply Current, Battery Backup Mode—MCM9L4000A Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W} = V_{CC} - 0.2$ V; DQ = $V_{CC} - 0.2$ V, 0.2 V or Open; A0–A10 = $V_{CC} - 0.2$ V or 0.2 V) t_{RAS} = Min to 1 µs	I_{CC7}	—	2.7	mA	2, 4
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	–90	90	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(O)}$	–20	20	µA	
Output High Voltage (I_{OH} = –5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	55	pF	5
	D8, $\overline{CAS8}$		17	pF	5
Input/Output Capacitance	DQ0–DQ7	$C_{I/O}$	22	pF	5
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	17	pF	5

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.
5. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = IΔt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		94000A-60 9L4000A-60		94000A-70 9L4000A-70		94000A-80 9L4000A-80		94000A-10 9L4000A-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	180	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	100	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	100	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	55	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	25	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	25	75	ns	11

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

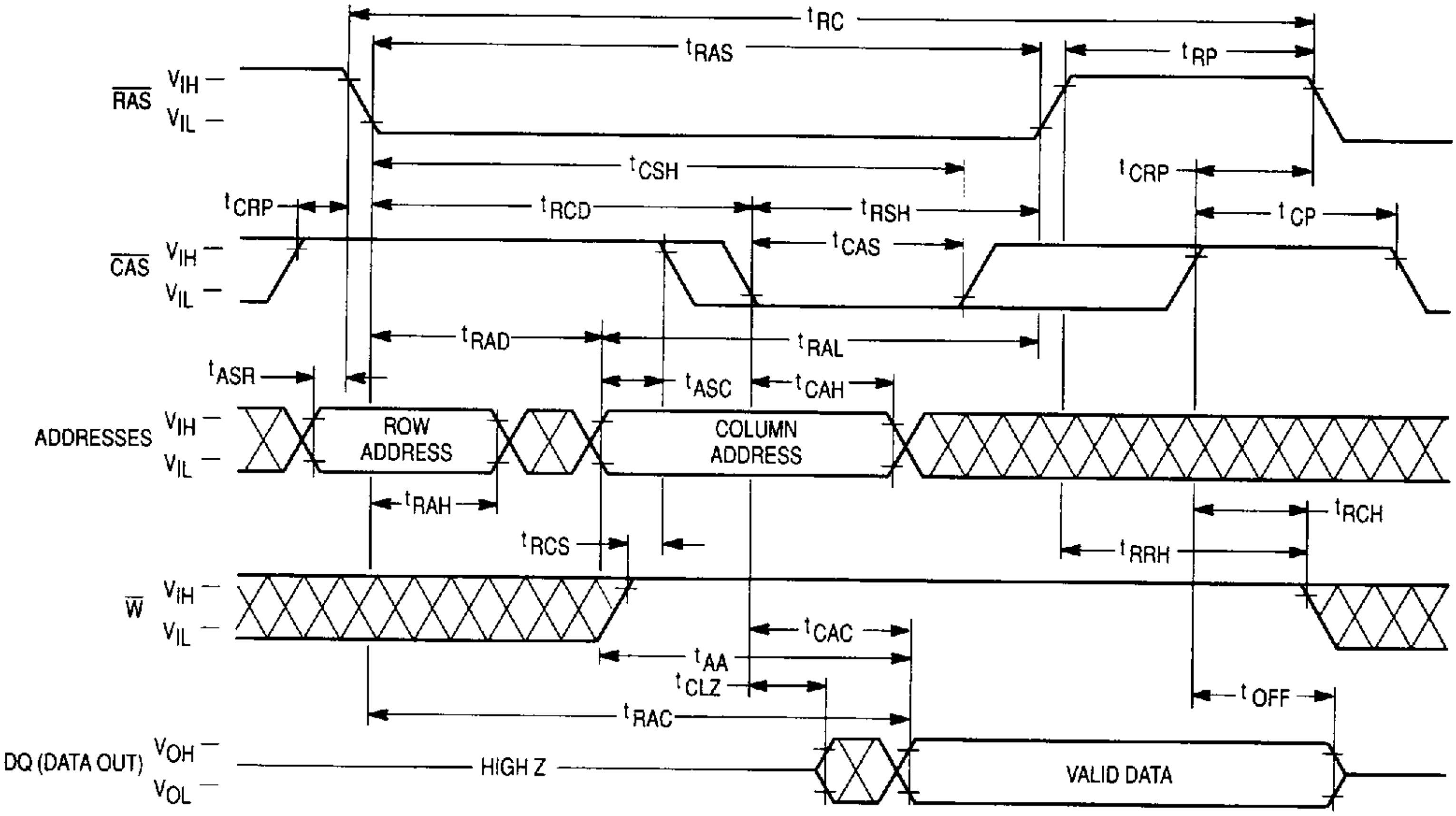
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		94000A-60 9L4000A-60		94000A-70 9L4000A-70		94000A-80 9L4000A-80		94000A-10 9L4000A-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	20	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	20	—	ns	14
Refresh Period MCM94000A MCM9L4000A	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	50	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	10	—	ns	

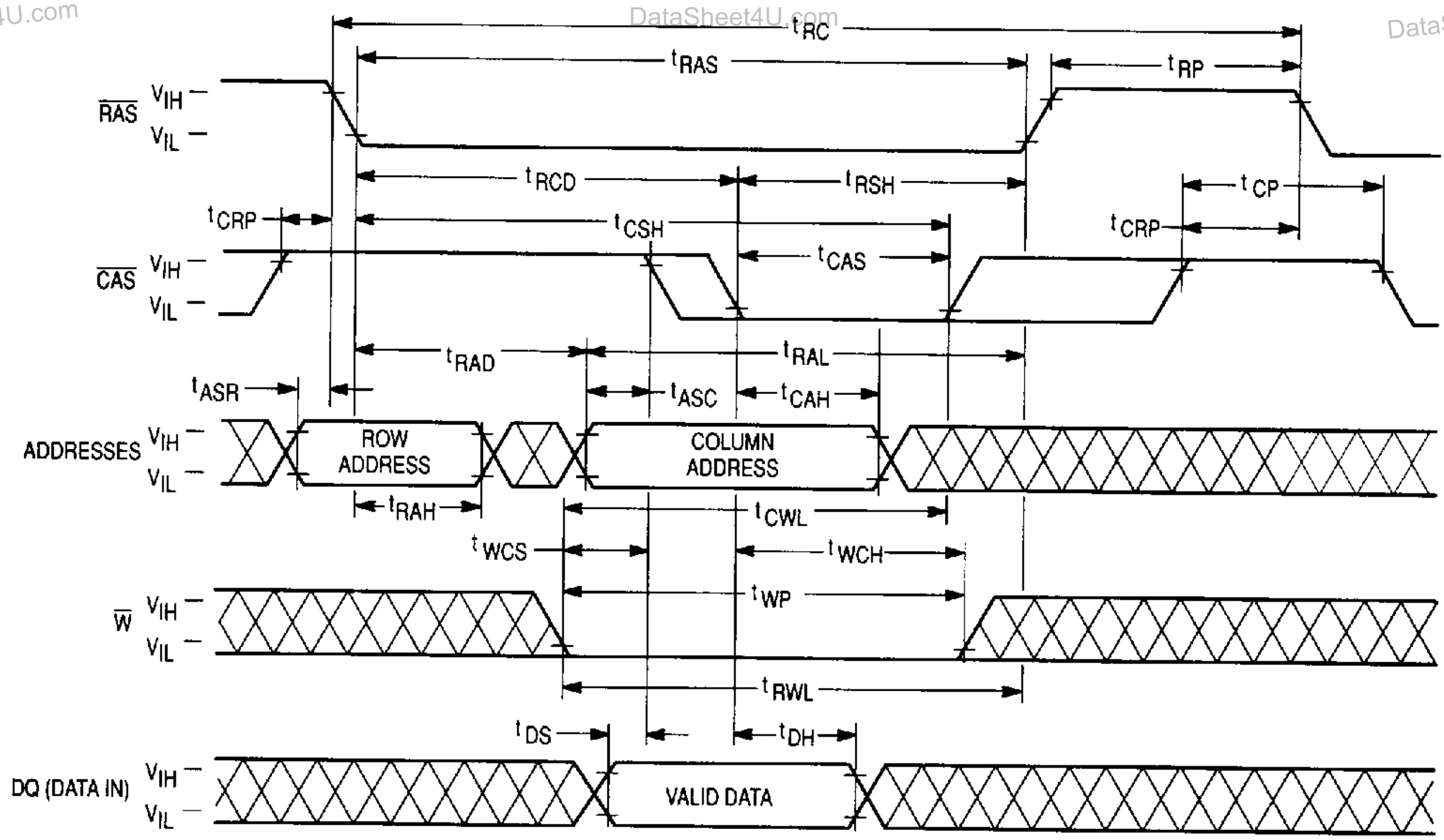
NOTES:

12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

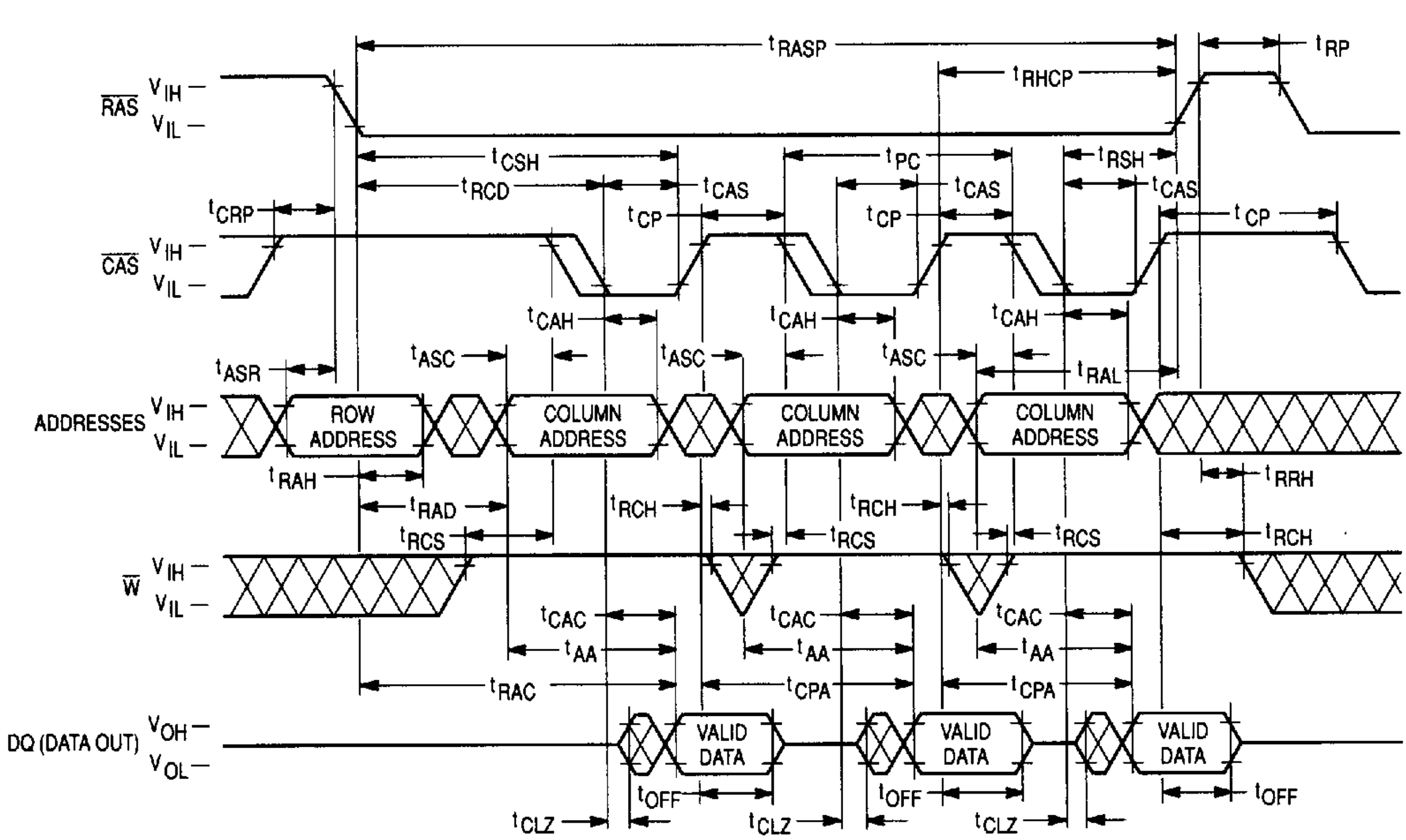
READ CYCLE



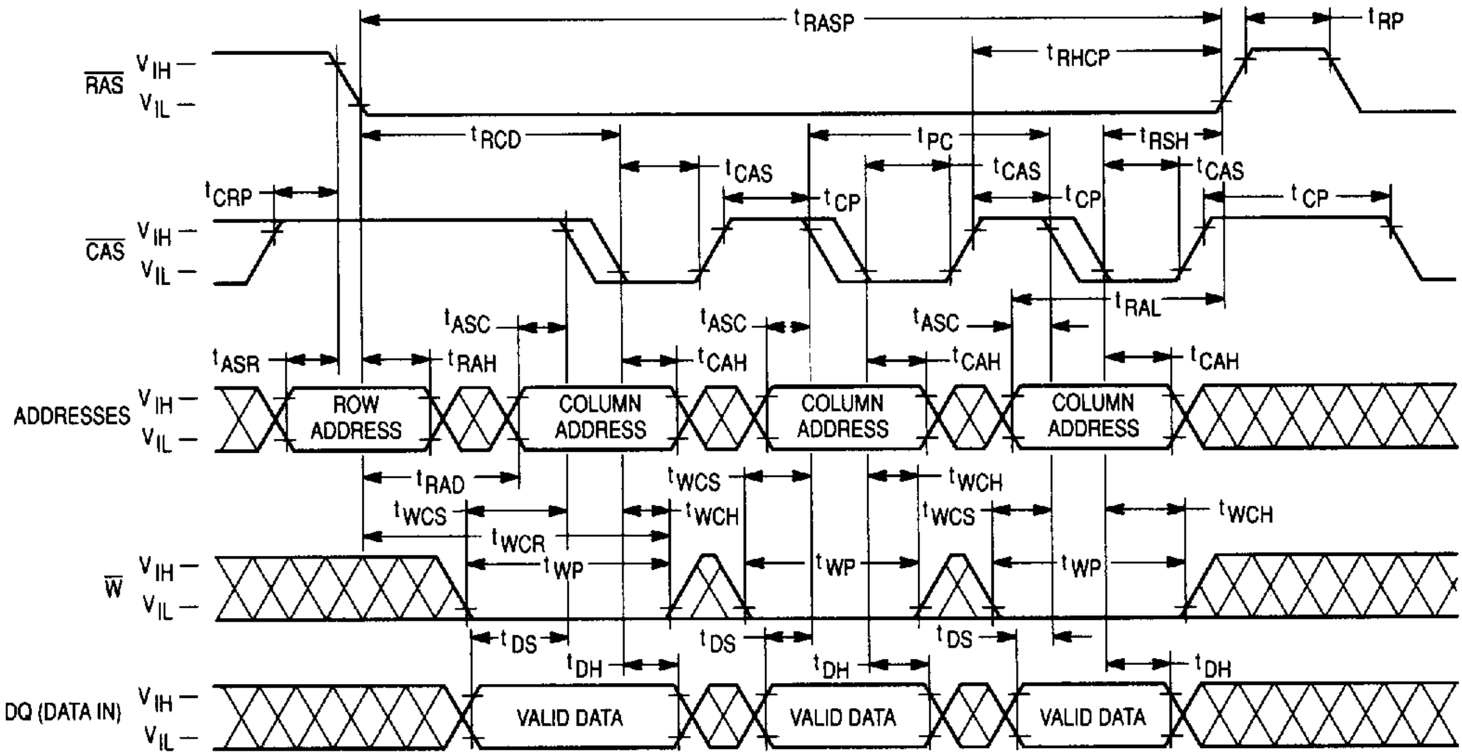
EARLY WRITE CYCLE



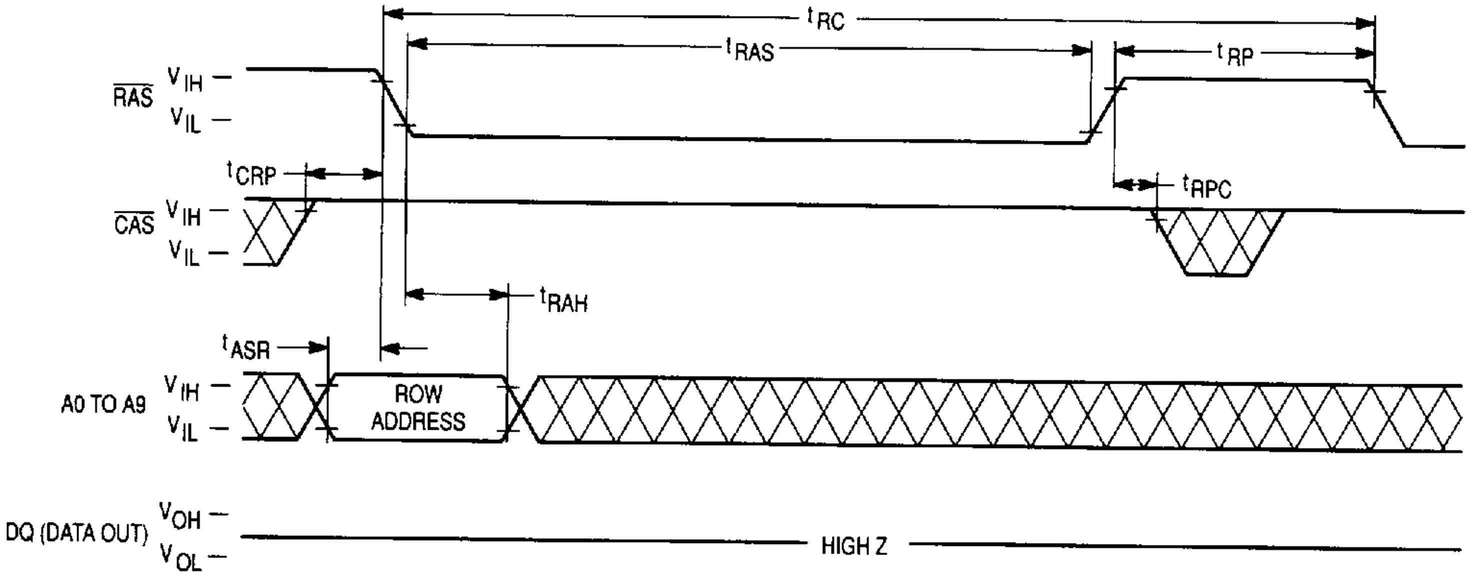
FAST PAGE MODE READ CYCLE



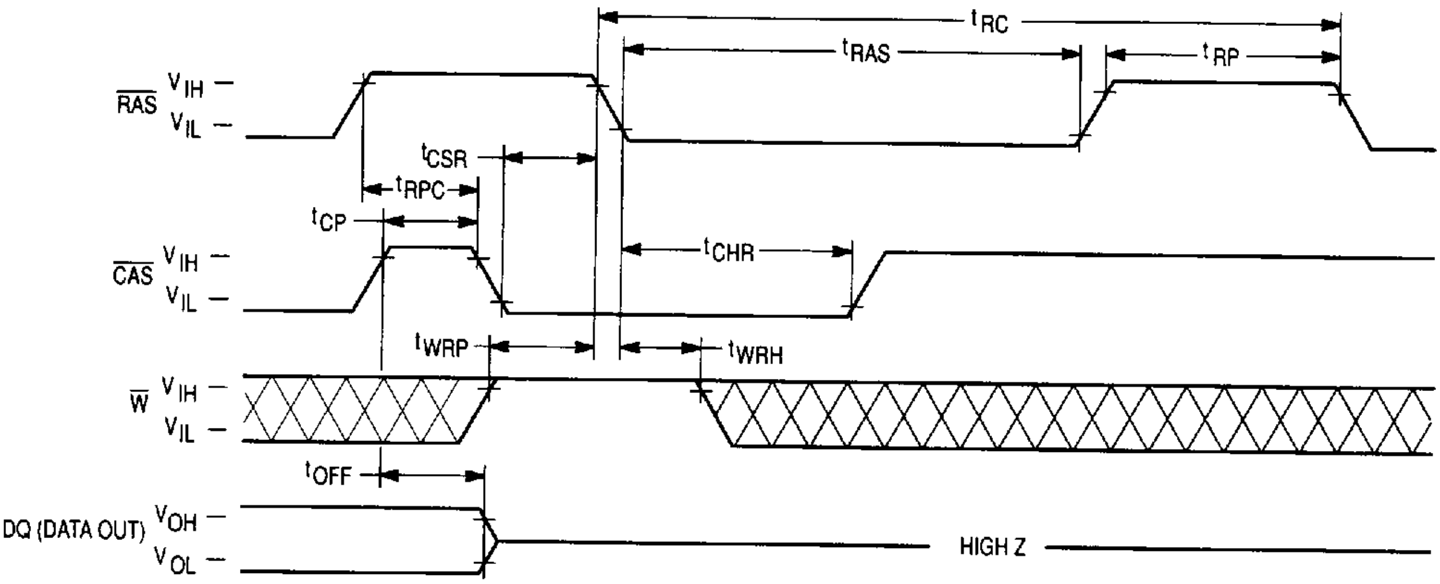
FAST PAGE MODE EARLY WRITE CYCLE



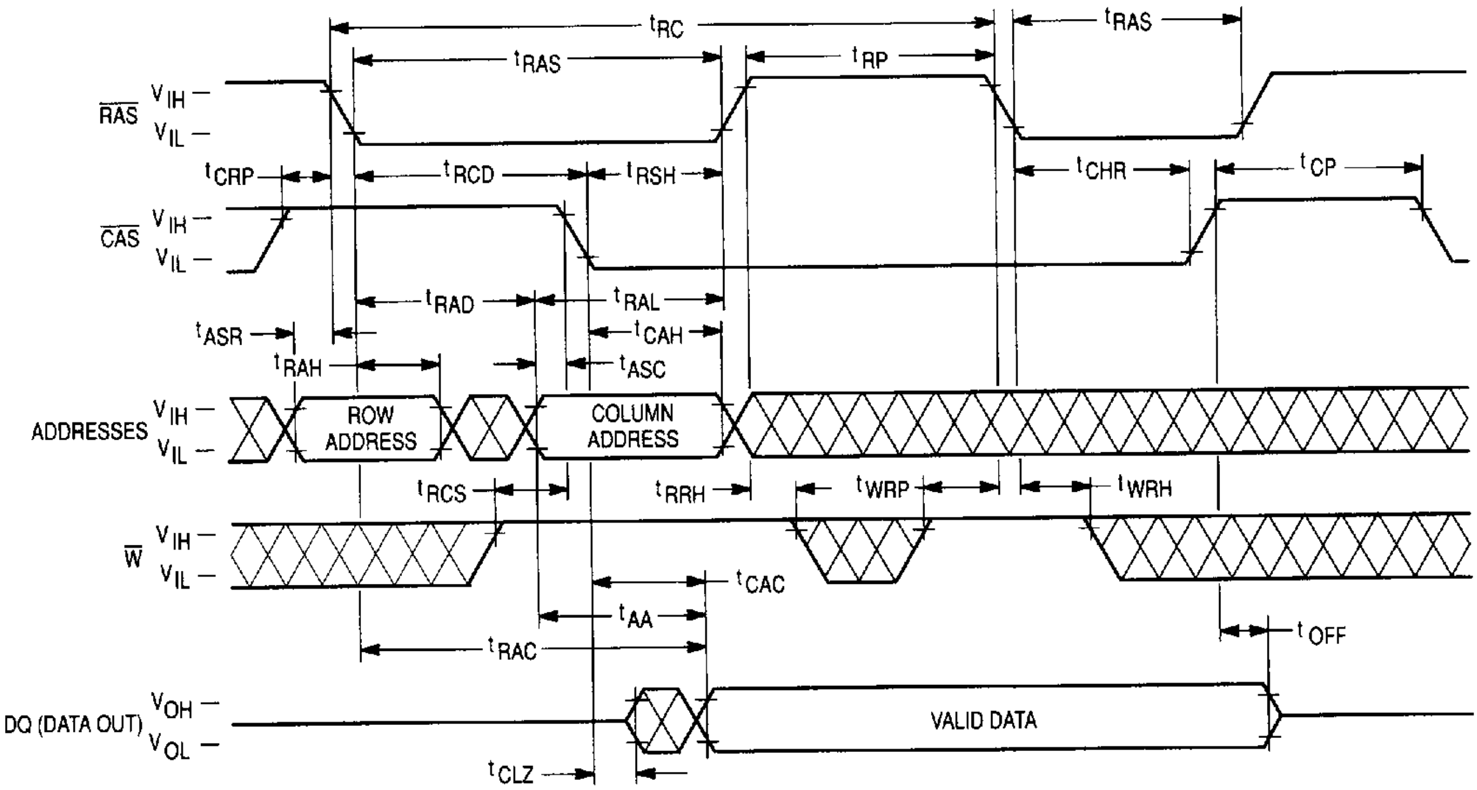
RAS ONLY REFRESH CYCLE
(W and A10 are Don't Care)



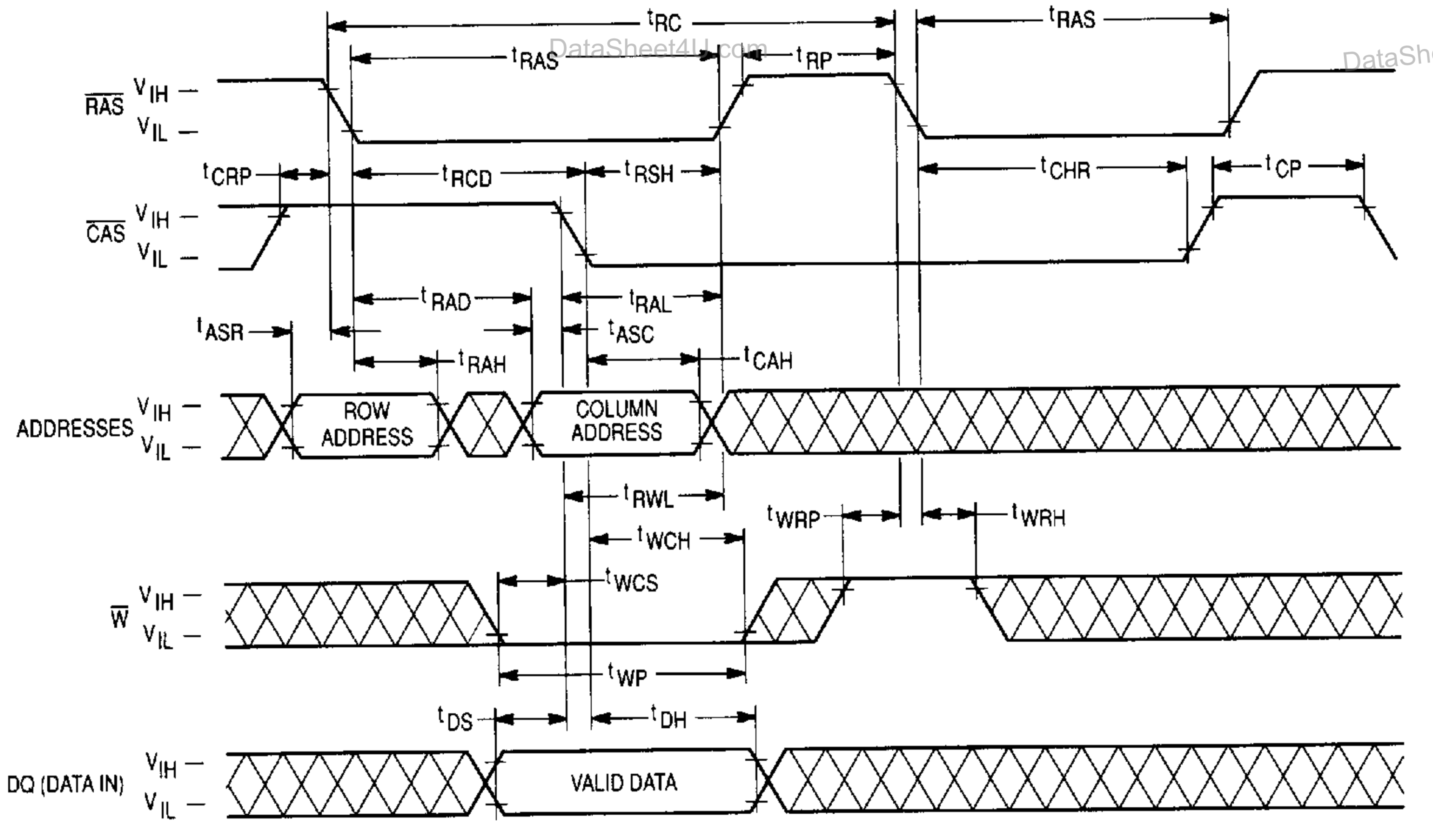
CAS BEFORE RAS REFRESH CYCLE
(A0 to A10 are Don't Care)



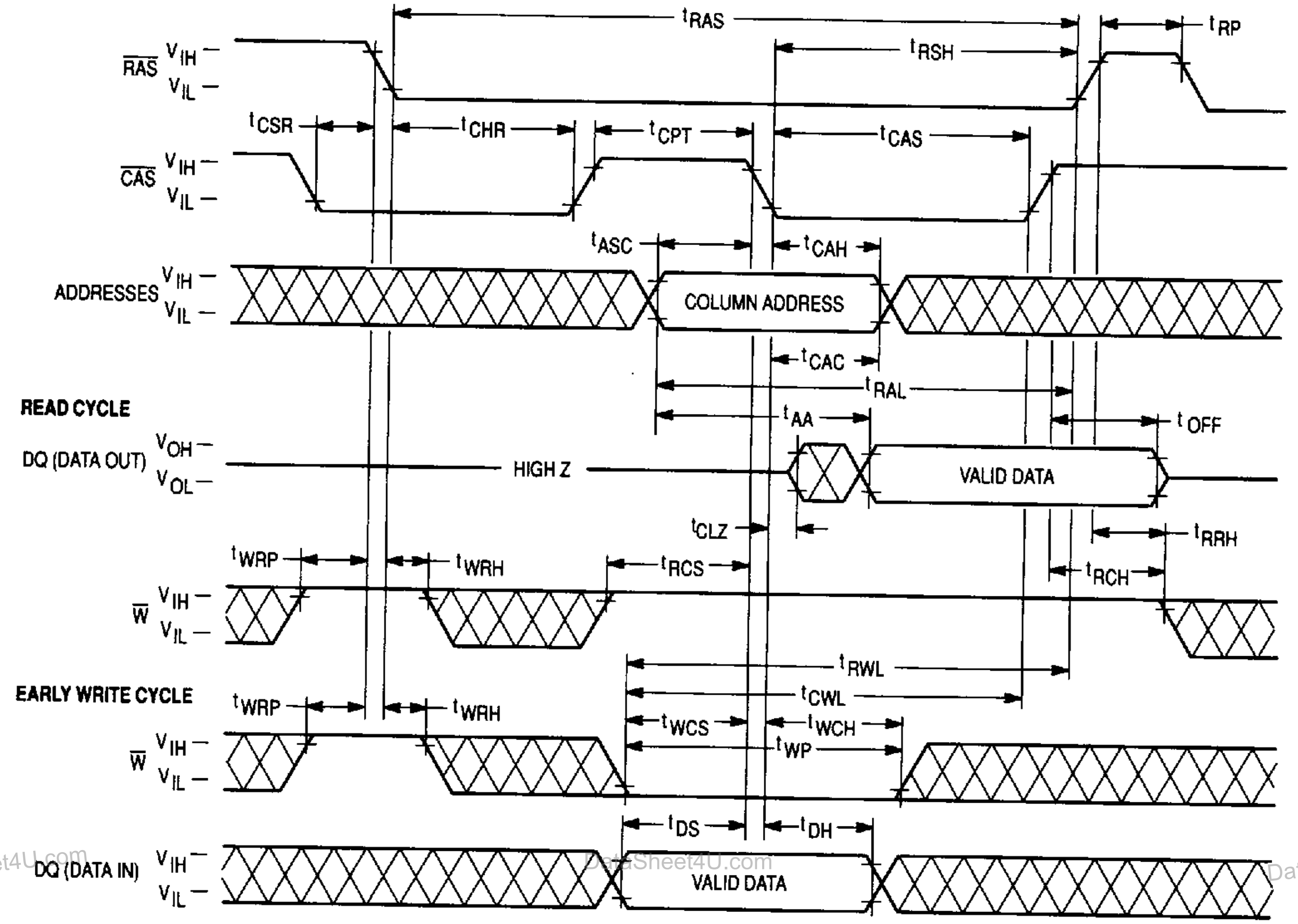
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode.**

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operation is covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed inconsecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM94000A require refresh every 16 milliseconds, while refresh time for the MCM9L4000A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM94000A, and 124.8 microseconds for the MCM9L4000A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM94000A and 128 milliseconds on the MCM9L4000A.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle.** Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

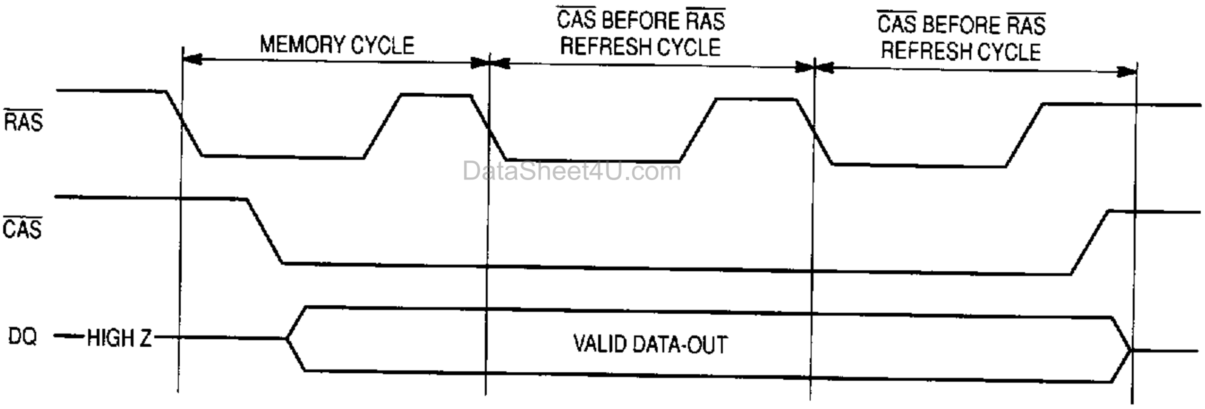


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 94000A or 9L4000A X XX

- MCM — Motorola Memory Prefix
- 94000A or 9L4000A — Part Number
- X — Package (AS = SIMM, L = SIP, LH = Low Height SIP)
- XX — Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns, 10 = 100 ns)

Full Part Numbers—

MCM94000AS60	MCM94000L60	MCM94030LH60
MCM94000AS70	MCM94000L70	MCM94030LH70
MCM94000AS80	MCM94000L80	MCM94030LH80
MCM94000AS10	MCM94000L10	MCM94030LH10
MCM9L4000AS60	MCM9L4000L60	MCM9L4030LH60
MCM9L4000AS70	MCM9L4000L70	MCM9L4030LH70
MCM9L4000AS80	MCM9L4000L80	MCM9L4030LH80
MCM9L4000AS10	MCM9L4000L10	MCM9L4030LH10

