# MP6211/MP6212

## 3.3V/5V, Single-Channel 1A Current-Limited Power Distribution Switches

## DESCRIPTION

The MP6211/MP6212 single-channel Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP6211/MP6212 Analog switch has 90mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP6211/MP6212 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP6211/MP6212 is available in an 8-PIN MSOP and SOIC package with exposed pad.

## FEATURES

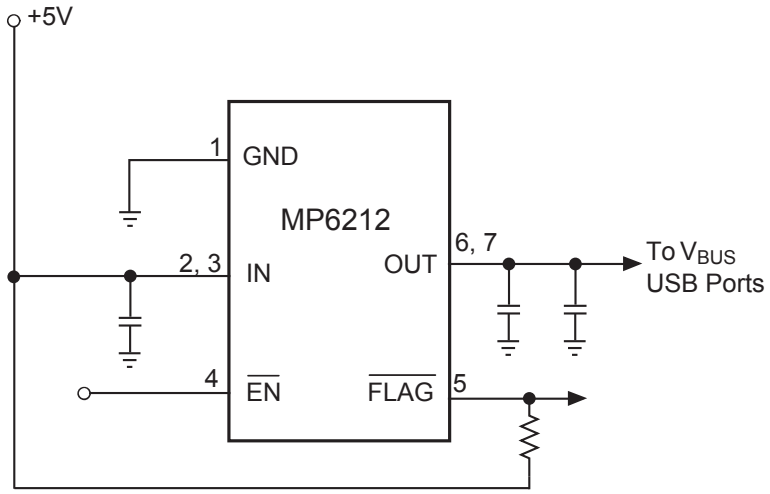
- 1A Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 90mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- MSOP8E and SOIC8E package
- UL Recognized: E322138

## APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- USB Power Distribution



## TYPICAL APPLICATION




SINGLE-CHANNEL

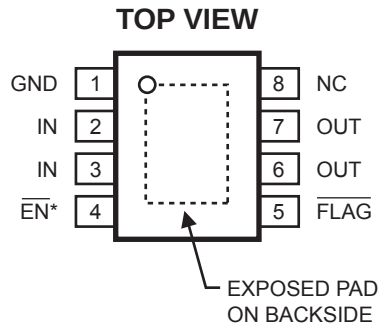
UL Recognized Component

## ORDERING INFORMATION

| Part Number* | Enable S | witch | Maximum Continuous Load Current | Typical Short-Circuit Current @ $T_A$=25C | Package | Top Marking | Temperature |
|---|---|---|---|---|---|---|---|
| MP6211DN | Active High | Single | 1.0A | 1.5A | SOIC8E | 6211D | –40°C to +85°C |
| MP6211DH | Active High | Single | 1.0A | 1.5A | MSOP8E | | |
| MP6212DN | Active Low | Single | 1.0A | 1.5A | SOIC8E | 6212D | |
| MP6212DH | Active Low | Single | 1.0A | 1.5A | MSOP8E | | |

* For Tape & Reel, add suffix –Z (eg. MP6211_MP6212DN–Z). For RoHS Compliant Packaging, add suffix –LF. (eg. MP6211_MP6212DN–LF–Z)

## PACKAGE REFERENCE




MP6211_MP6212

Single-Channel

(* EN is active high for MP6211)

## ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +6.0V
EN, FLAG, OUT to GND .....-0.3V to +6.0V
Continuous Power Dissipation. ($T_A$ = +25°C) (2)
SOIC8E ..... 2.5W
MSOP8E ..... 2.3W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature.....–65°C to +150°C
Operating Temperature.....–40°C to +85°C

| ***Thermal Resistance*** (3) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| SOIC8E | 50 | 10 °C/W |
| MSOP8E | 55 | 12 °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7 4-layer PCB.

## ELECTRICAL CHARACTERISTICS (4)

**$V_{IN}$=5V, $T_A$=+25°C, unless otherwise noted.**

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| IN Voltage Range | 2.7 | | | 5.5 | V |
| Supply Current | Single Channel | | 90 | 120 | µA |
| Shutdown Current | Device Disable, $V_{OUT}$=float, $V_{IN}$=5.5V | | 1 | | µA |
| Off Switch Leakage | Device Disable, $V_{IN}$=5.5V | | 1 | | µA |
| Current Limit | | 1.1 | 1.5 | 2.2 | A |
| Trip Current | Current Ramp (slew rate≤100A/s) on Output | 1.7 | | 2.4 | A |
| Under-voltage Lockout | Rising Edge | 1.95 | | 2.65 | V |
| Under-voltage Hysteresis | | | 250 | | mV |
| FET On Resistance | $I_{OUT}$=100mA (-40°C≤$T_A$≤85°C) | | 90 | 130 | mΩ |
| EN Input Logic High Voltage | 2 | | | | V |
| EN Input Logic Low Voltage | | | | 0.8 | V |
| FLAG Output Logic Low Voltage | $I_{SINK}$=5mA | | | 0.4 | V |
| FLAG Output High Leakage Current | $V_{IN}$=$V_{FLAG}$=5.5V | | | 1 | µA |
| Thermal Shutdown | | | 140 | | °C |
| Thermal Shutdown Hysteresis | | | 20 | | °C |
| $V_{OUT}$ Rising Time, Tr (5) | $V_{IN}$=5.5V, CL=1uF, RL=5.5Ω | | 0.9 | | ms |
| | $V_{IN}$=2.7V, CL=1uF, RL=5.5Ω | | 1.7 | | ms |
| $V_{OUT}$ Falling Time, Tf (6) | $V_{IN}$=5.5V, CL=1uF, RL=5.5Ω | | | 0.5 | ms |
| | $V_{IN}$=2.7V, CL=1uF, RL=5.5Ω | | | 0.5 | ms |
| Turn On Time, Ton (7) | $C_L$=100µF, RL=5.5Ω | | | 3 | ms |
| Turn Off Time, Toff (8) | $C_L$=100µF, RL=5.5Ω | | | 10 | ms |
| FLAG Deglitch Time | | 4 | 8 | 15 | ms |
| ENx Input Leakage | | 1 | | | µA |
| Reverse Leakage Current | OUT=5.5V, IN=GND | | 0.2 | | µA |

**NOTES:**

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90%.
6) Measured from 90% to 10%
7) Measured from (50%) EN signal to (90%) output signal.
8) Measured from (50%) EN signal to (10%) output signal.

## PIN FUNCTIONS

| SOIC8 MSOP8E | Name | Description |
|---|---|---|
| 1 | GND Expose Pad | Ground. Connect exposed pad to GND plane for optimal thermal performance. |
| 2, 3 | IN | Input Voltage. Accepts 2.7V to 5.5V input. |
| 4 | $\overline{EN}$ | Enable Input, Active Low: (MP6212), Active High: (MP6211) |
| 5 | $\overline{FLAG}$ | IN-to-OUT Over-current, active-low output flag. Open-Drain. |
| 6, 7 | OUT | Power-Distribution Switch Output. |
| 8 | N/C | No Connect. Not internally connected. |

## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = +25ºC, unless otherwise noted.**

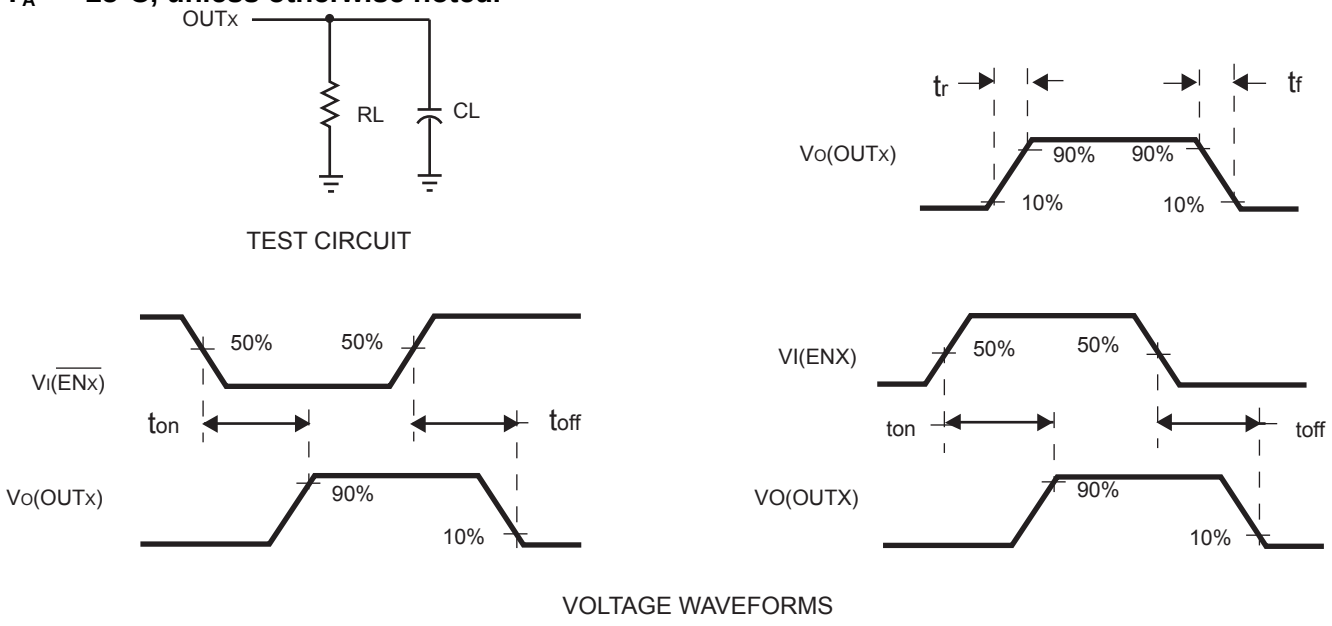


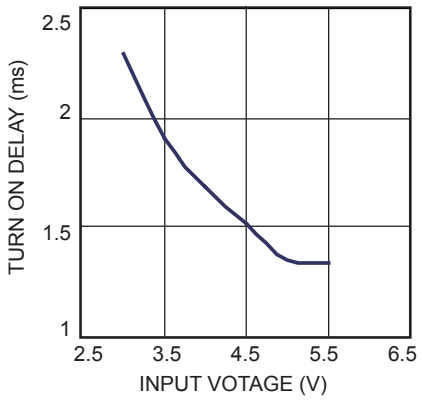

**Figure 1—Test Circuit and Voltage Waveforms**

## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$=5.5V, $C_L$=2.2uF, $T_A$ = +25ºC, unless otherwise noted.**

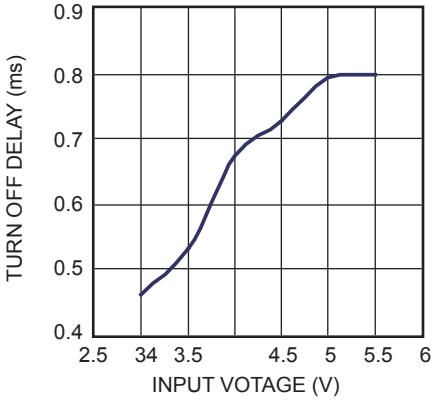
### Turn on Delay vs. Input Voltage

$V_{EN}$=5V, $R_L$=5.5Ω



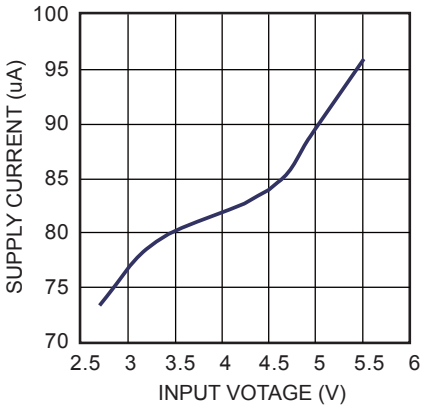

### Turn off Delay vs. Input Voltage

$V_{EN}$=5V, $R_L$=5.5Ω



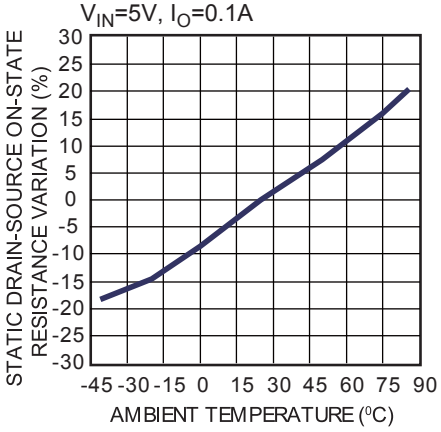

### Supply Current, Output Enabled vs. Input Voltage

$V_{EN}$=5V



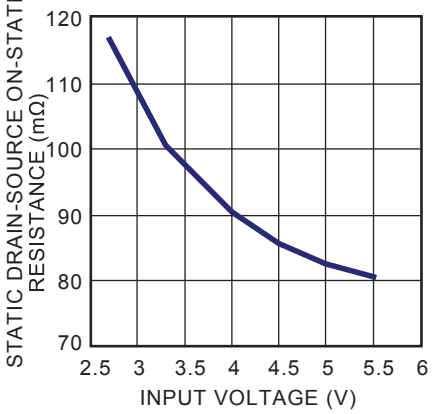

### Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

$V_{IN}$=5V, $I_O$=0.1A



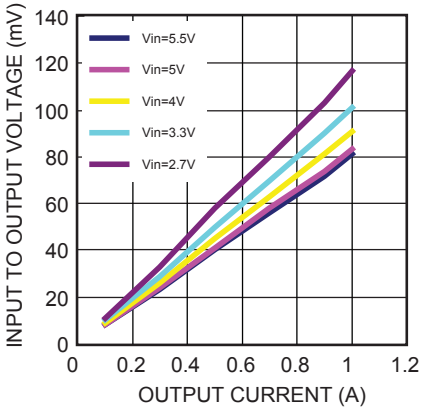

### Static Drain-Source On-State Resistance vs. Input Voltage

$V_{EN}$=5V, $I_{OUT}$=1A



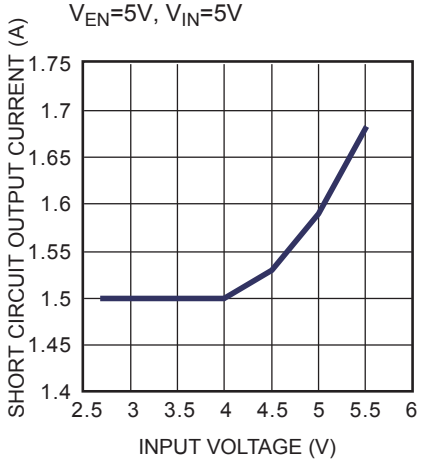

### Input to Output Voltage vs. Load Current

$V_{EN}$=5V



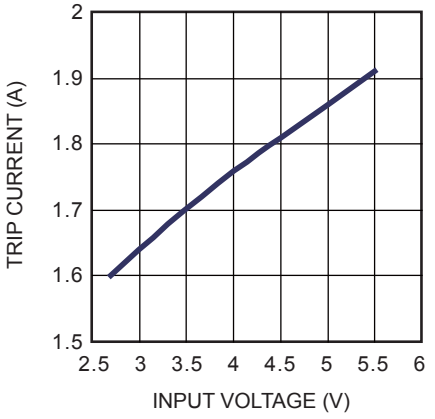

### Short Circuit Output Current vs. Input Voltage

$V_{EN}$=5V, $V_{IN}$=5V



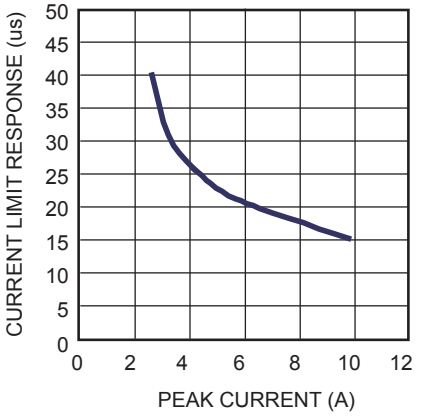

### Threshold Trip Current vs. Input Voltage

$V_{EN}$=5V




### Current Limit Response Time vs. Peak Current

$V_{EN}$=5V

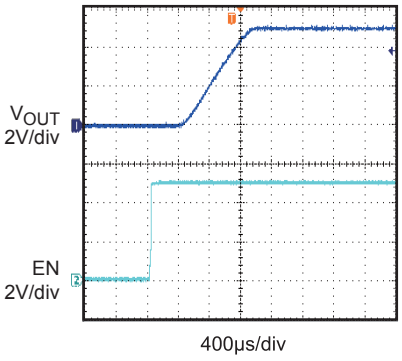


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$=5.5V, $T_A$ = +25ºC, unless otherwise noted.**

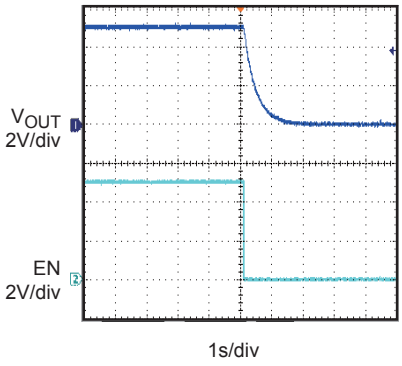
### Turn On Delay and Rise Time with 0.1uF Load

$V_{EN}$=5V, $C_L$=0.1uF



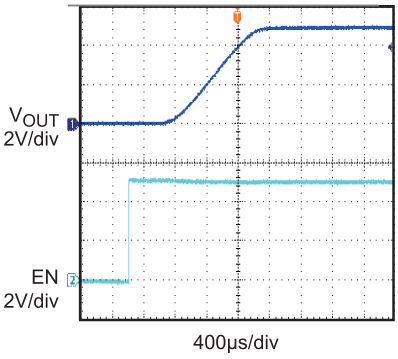

### Turn Off Delay and Fall Time with 0.1uF Load

$V_{EN}$=5V, $C_L$=0.1uF



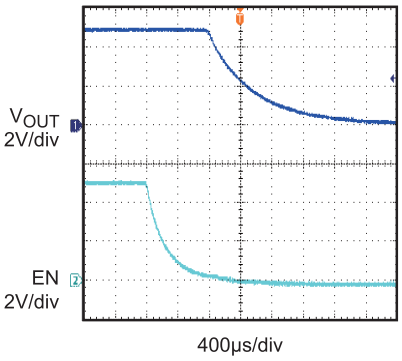

### Turn on Delay and Rise Time with 1uF Load

$V_{EN}$=5V, $R_L$=5.5Ω, $C_L$=1uF



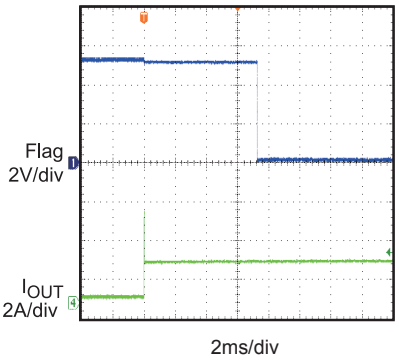

### Turn off Delay and Fall Time with 1uF Load

$V_{EN}$=5V, $R_L$=5.5Ω, $C_L$=1uF



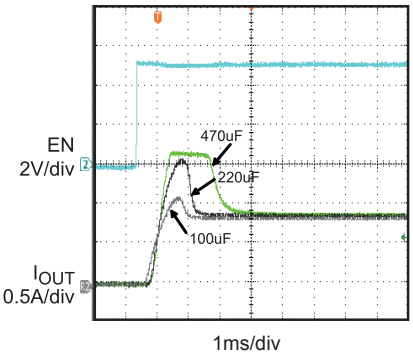

### 1Ω Load Connected to Enabled Device

$V_{EN}$=5V, $C_L$=1uF



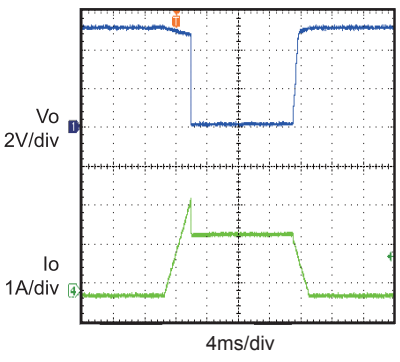

### Inrush Current with Different Load Capacitance

$V_{EN}$=5V, $R_L$=5.5Ω, Start up by EN



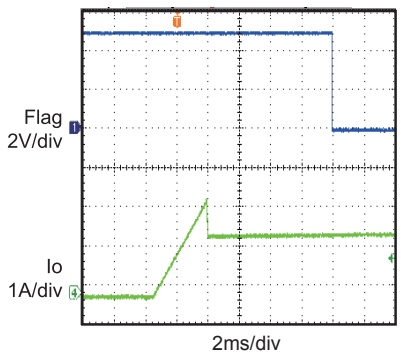

### Threshold Trip Current with Ramped Load on Enabled Device

$V_{EN}$=5V, $C_L$=1uF



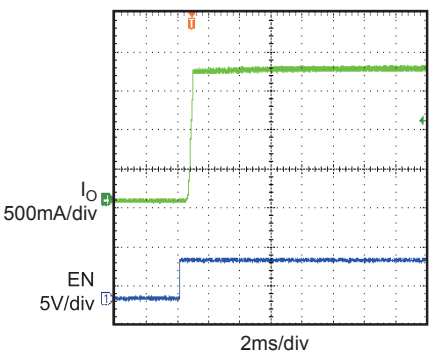

### Ramped Load on Enabled Device

$V_{EN}$=5V, $C_L$=1uF




### Short Circuit Current, Device Enabled into Short

$V_{EN}$=5V, $C_L$=1uF



## FUNCTION BLOCK DIAGRAM

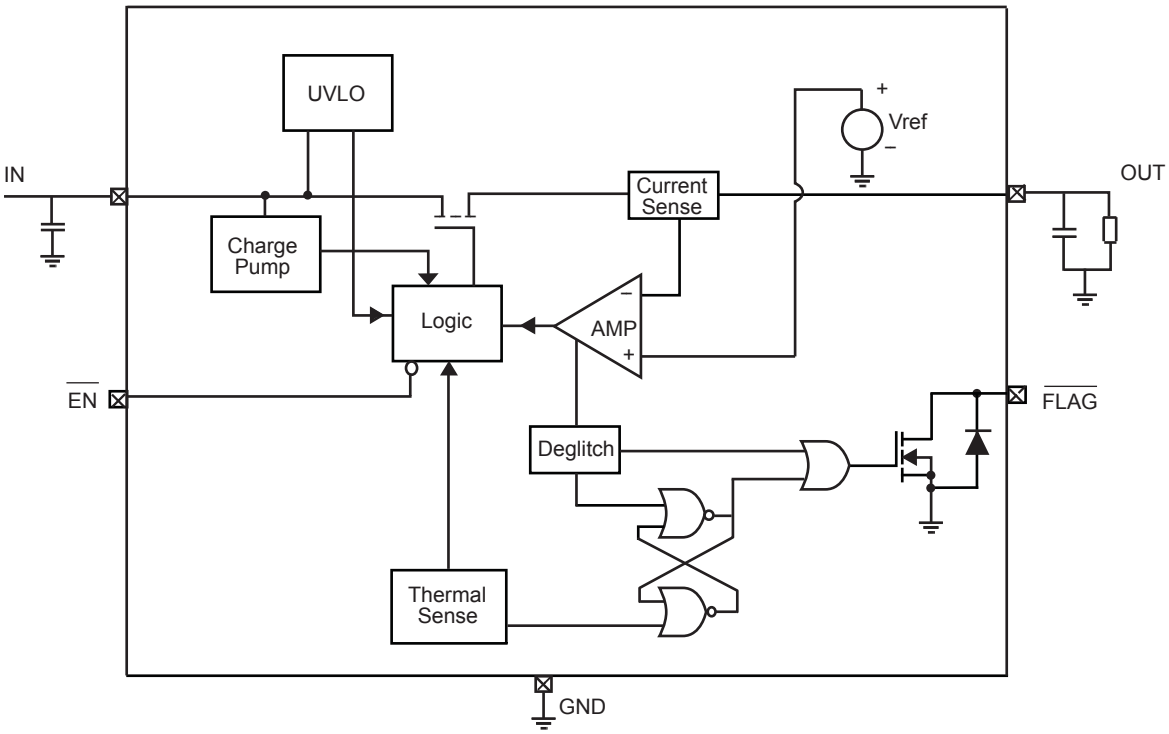



**Figure 2—Functional Block Diagram**

## DETAILED DESCRIPTION

### Over Current

When the load exceeds trip curre nt (minimu m threshold current triggering co nstant-current mode) or a short is pr esent, MP6211/MP621 2 switches into to a const ant-current mode (current limit value). MP6211/MP6212 will be shutdown only if the overcurrent condit ion stays lo ng enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the d evice is ena bled or inpu t applied. MP MP6211/MP6212 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enab led. After the cu rrent-limit circuit ha s been tripped (reached the trip current threshold), t he device switches into constant-current mode. However, high cu rrent ma y flow for a short perio d of time before the current-limit circuit can react.
3) Output current has bee n gradually increased beyond the recommend ed operatin g current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exce eded. The MP6211/ MP6212 is capable of delivering current up to the trip cur rent thresh old without damaging the device. Once the trip threshold has been reached, t he device switches into its constant-current mode.

### Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch t imeout. This is used to e nsure that no false fau lt signals are reported. This intern al deglitch circuit elimina tes the ne ed for extend components. The FLAG pin is n ot deglitche d during an over temp. or a voltage lockout.

### Thermal Protection

The purpose of thermal protect ion is to prevent damage in the IC by allowing exceptive current to flow and he ating the ju nction. The die temp. is internally monitored un til the ther mal limit i s reached. Once this temp. is reached, the sw itch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

### Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage t o ensure tha t the MP6211/6212 is operat ing correctly. This UVLO circuit a lso ensures t hat there is no operation until the input voltage reaches the minimum spec.

### Enable

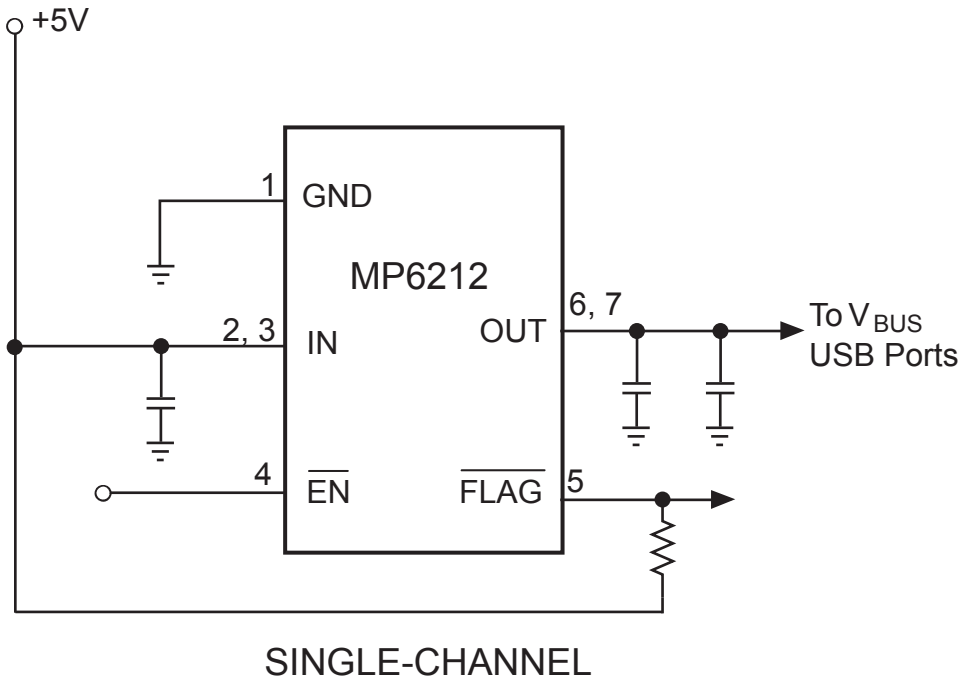
The logic p in disab les the ch ip t o reduce t he supply current. The device will oper ate once th e enable sign al reaches t he appropriate level. The input is compatible with both COMS and TTL.

## APPLICATION INFORMATION

### Power-Supply Considerations

Over 10 µF capacitor between IN and GND is recommended. This pr ecaution re duces power-supply transients that may cause ringing on the input and improves the immunit y of t he device to short-circuit transients.

In order to achieve smaller output load transie nt ripple, pla cing a high-value electro lytic capacit or on the out put pin(s) is recommended when th e load is heavy.

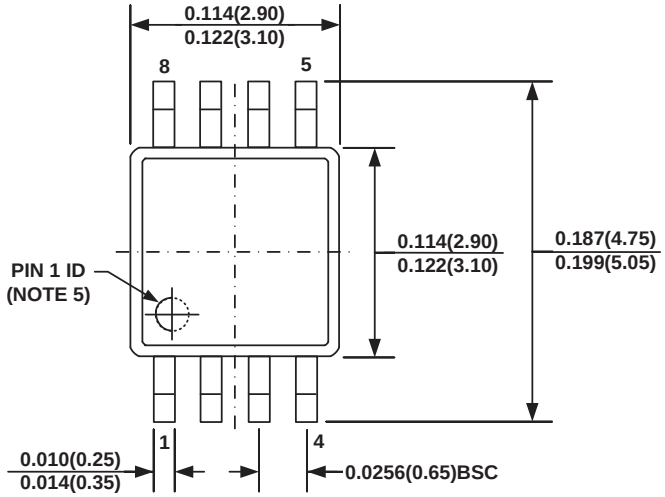



SINGLE-CHANNEL

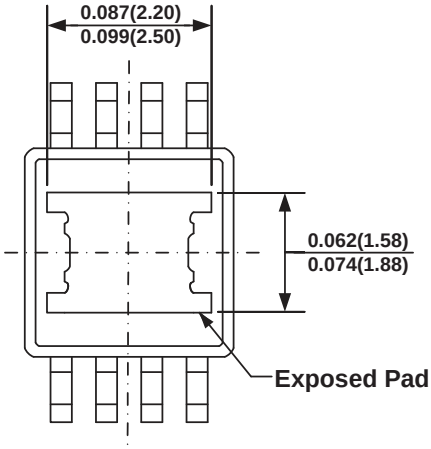
**Figure 3—Application Circuit**

# PACKAGE INFORMATION

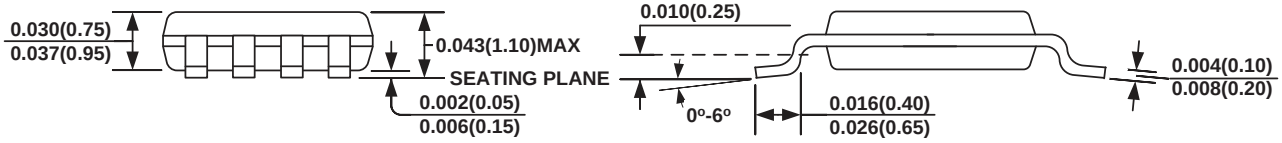
## MSOP8E (EXPOSED PAD)




TOP VIEW

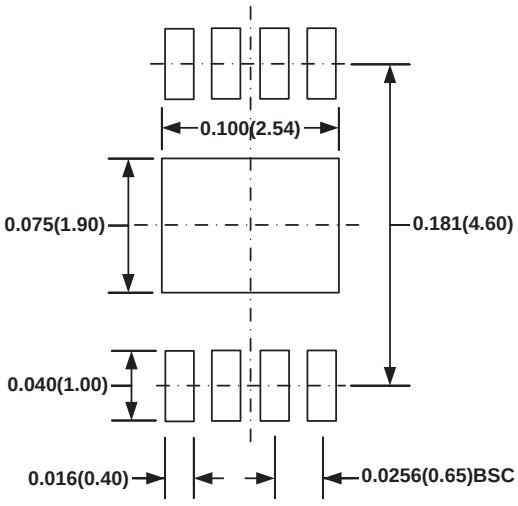



BOTTOM VIEW




FRONT VIEW

SIDE VIEW

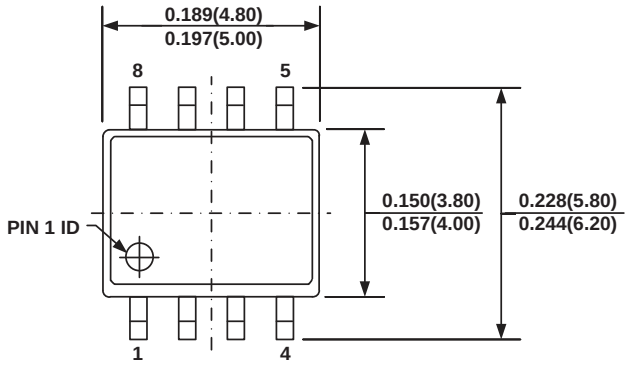



RECOMMENDED LAND PATTERN

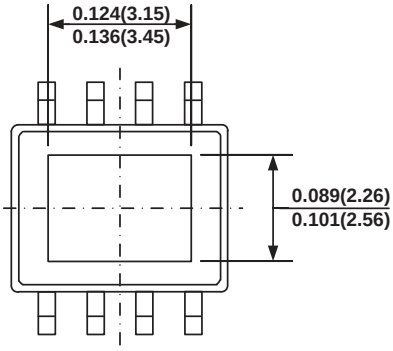
**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
7) DRAWING IS NOT TO SCALE.

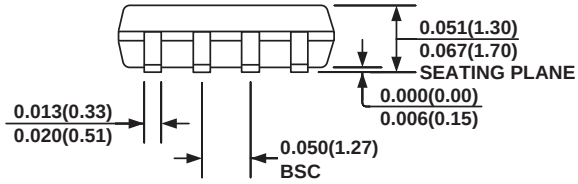
## SOIC8E (EXPOSED PAD)



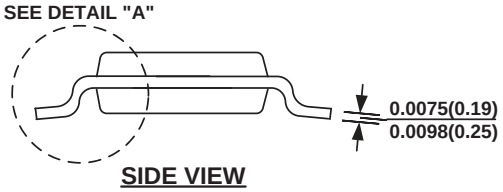

TOP VIEW



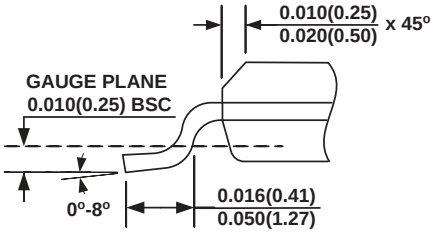

BOTTOM VIEW



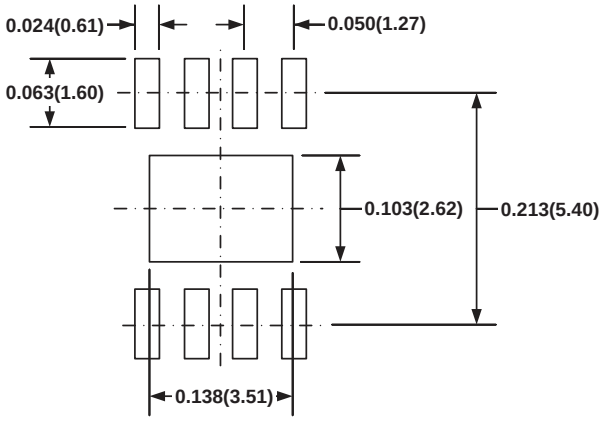

FRONT VIEW




SIDE VIEW




DETAIL "A"




RECOMMENDED LAND PATTERN

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.