

Dual Half Bridge Driver with Boost Converter

■ GENERAL DESCRIPTION

The **NJW4813** is a dual half bridge driver with boost converter IC.

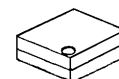
Output voltage boost from Li-ion battery and a 5V power supply and can drive a piezo device by two half bridge drivers.

The NJW4813 is able to stable startup by soft start function in boost SW.REG.

The dual half bridge driver improves control characteristics from a microcomputer in response to independent signal input in each channel.

The input frequency operates to 300kHz and in the case of failure, it can output a fault flag.

■ PACKAGE OUTLINE



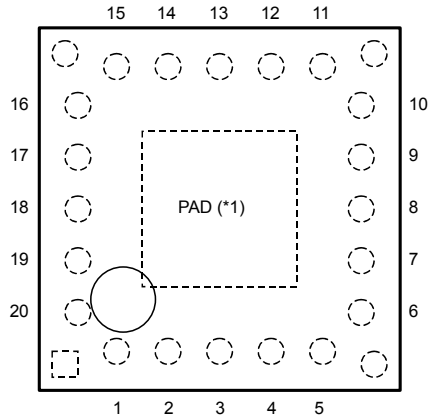
NJW4813SE3

■ FEATURES

- | | | |
|---|---|---|
| <ul style="list-style-type: none"> ● Boost Converter Block | <ul style="list-style-type: none"> Output Switch Voltage Switching Current PWM Control Operating Voltage Range Oscillation Frequency Range Soft Start Function Over Current Protection | <ul style="list-style-type: none"> 40V max. 1A min. 2.7 to 5.5V 380k to 810kHz 17ms typ. |
| <ul style="list-style-type: none"> ● Half Bridge Driver Block | <ul style="list-style-type: none"> Internal 2-Channel Half Bridge Each Channel Operates Individually Output Switch Peak Current Operating Voltage Range Switching Frequency Output Shut Down Control Over Current Protection Fault Indicator Output | <ul style="list-style-type: none"> +280 / -250mA typ. 8.0 to 35V 300kHz max. |
| <ul style="list-style-type: none"> ● Under Voltage Lockout ● Built-in Thermal Shutdown ● Standby Function ● Package Outline | <ul style="list-style-type: none"> NJW4813SE3 : PCSP20-E3 | <ul style="list-style-type: none"> |

NJW4813

■ PIN CONFIGURATION



< Top View >

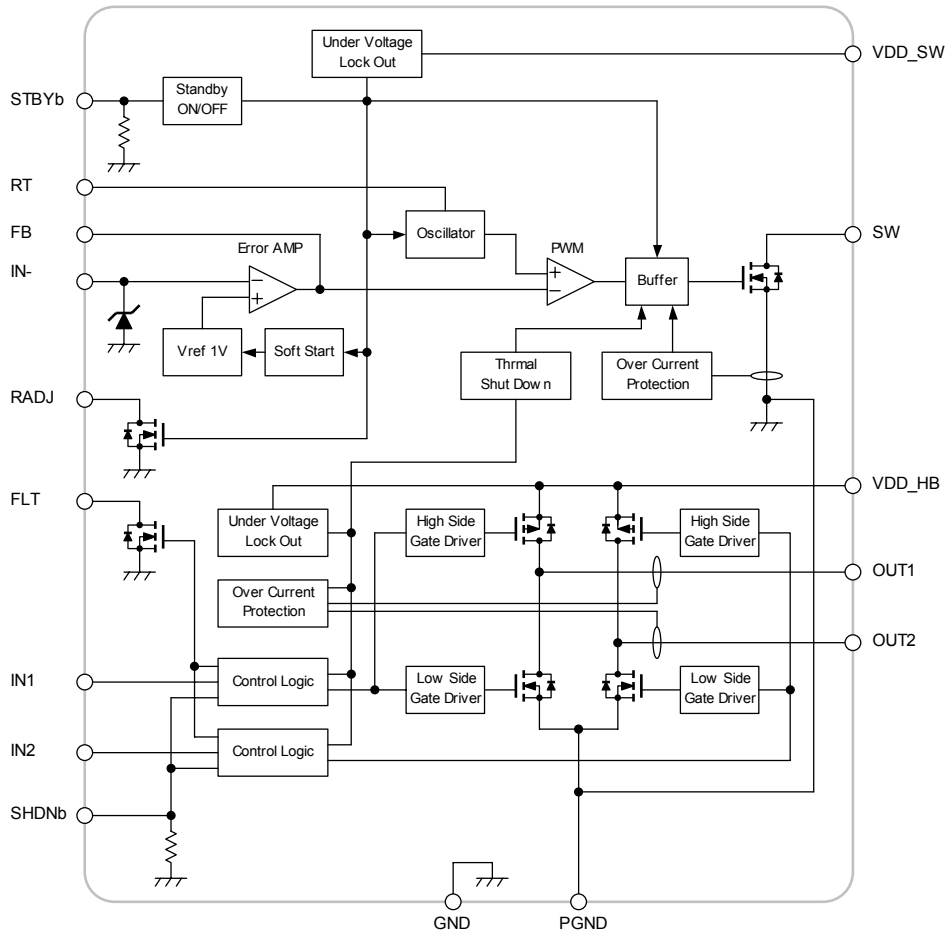
PIN FUNCTION

- | | |
|-----------|------------|
| 1. VDD_SW | 11. VDD_HB |
| 2. STBYb | 12. OUT1 |
| 3. SHDNb | 13. PGND |
| 4. IN1 | 14. PGND |
| 5. IN2 | 15. SW |
| 6. FLT | 16. SW |
| 7. RT | 17. NC |
| 8. GND | 18. RADJ |
| 9. PGND | 19. FB |
| 10. OUT2 | 20. IN- |

(*1) The PAD is not connected to an IC chip electrically.

NJW4813SE3

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Boost Converter Block			
Supply Voltage	V_{DD_SW}	+6	V
SW pin Voltage	V_{SW}	+40	V
RADJ pin Voltage	V_{RADJ}	+6 (*2)	V
IN- pin Voltage	V_{IN-}	-0.3 to +6 (*2)	V
STBYb pin Voltage	V_{STBYb}	-0.3 to +6 (*2)	V
Half Bridge Driver Block			
Supply Voltage	V_{DD_HB}	+40	V
SHDNb pin Voltage	V_{SHDNb}	-0.3 to +6 (*2)	V
Input Voltage	V_{IN1} V_{IN2}	-0.3 to +6 (*2)	V
FLT pin Voltage	V_{FLT}	-0.3 to +6	V
Power Dissipation	P_D	The back pad is mounted. 560 (*3) 980 (*4) The back pad is not mounted. 550 (*3) 850 (*4)	mW
Junction Temperature Range	T_j	-40 to +150	°C
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(*2): When Supply voltage is less than +6V, the absolute maximum voltage is equal to the Supply voltage.

(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm

This product may be damaged with electric static discharge (ESD).

Please handle with care to avoid these damages.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Boost Converter Block					
Supply Voltage	V_{DD_SW}	2.7	—	5.5	V
STBYb pin Voltage	V_{STBYb}	0	—	V_{DD_SW}	V
Timing Resistor	R_T	95	100	146	kΩ
Oscillating Frequency	f_{OSC}	380	700	810	KHz
Half Bridge Driver Block					
Supply Voltage	V_{DD_HB}	8	—	35	V
Output Switch DC Current	I_{OM}	0	—	20	mA
SHDNb pin Voltage	V_{SHDNb}	0	—	V_{DD_SW}	V
Input Voltage	V_{IN1}, V_{IN2}	0	—	V_{DD_SW}	V
FLT pin Voltage	V_{FLT}	0	—	5.5	V

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■ ELECTRICAL CHARACTERISTICS

Boost Converter Block

(Unless otherwise noted, $V_{DD_SW}=V_{STBYb}=3.7V$, $R_T=100k\Omega$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Under Voltage Lockout Block

UVLO Release Voltage	V_{RUVLO_SW}		2.1	2.4	2.7	V
UVLO Operate Voltage	V_{DUVLO_SW}		2.0	2.2	2.5	V
UVLO Hysteresis Voltage	ΔV_{UVLO_SW}	$V_{RUVLO_SW} - V_{DUVLO_SW}$	–	0.2	–	V

Soft Start Block

Soft Start Time	T_{SS}	$V_B=0.95V$	8	17	28	ms
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Oscillator Block

Oscillation Frequency	f_{OSC}		630	700	770	kHz
Oscillation Frequency deviation (Supply voltage)	f_{DV}	$V_{DD_SW}=3.0$ to $5.5V$	–	1	–	%
Oscillation Frequency deviation (Temperature)	f_{DT}	$T_a= -40$ to $+85^\circ C$	–	3	–	%

Error Amplifier Block

Reference Voltage	V_B	Short IN- and FB, Measuring IN- Pin	-1.0%	1.00	+1.0%	V
Input Bias Current	I_B	$V_B=1.0V$	-0.1	–	+0.1	μA
Open Loop Gain	A_V		–	80	–	dB
Gain Bandwidth	G_B		–	1	–	MHz
Output Source Current	I_{OM+}	$V_{FB}=1V$, $V_{IN-}=0.9V$	8	16	24	μA
Output Sink Current	I_{OM-}	$V_{FB}=1V$, $V_{IN-}=1.1V$	0.9	1.4	4	mA
IN- pin Clamp Voltage	V_{CLIN-}	$V_{STBYb}=0V$, $V_{DD_SW}=5.5V$, $I_{CLIN-}=10\mu A$	4.8	5.2	5.6	V
RADJ pin FET ON Resistance	R_{ON_RADJ}	$I_{RADJ}=0.1mA$	–	200	280	Ω
RADJ pin FET Leak Current	I_{LEAK_RADJ}	$V_{STBYb}=0V$, $V_{RADJ}=3.3V$	–	–	1	μA

PWM Compare Block

Maximum Duty Cycle	M_{AXDUTY}	$V_{IN-}=0.9V$	82	87	92	%
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Output Block

Output ON Resistance	R_{ON_SW}	$I_{SW}=100mA$	–	0.6	1.2	Ω
Switching Current Limit	I_{LMT_SW}		1	2	–	A
Switching Leak Current	I_{LEAK_SW}	$V_{STBYb}=0V$, $V_{SW}=40V$	–	–	1	μA

■ ELECTRICAL CHARACTERISTICS

Half Bridge Driver Block

(Unless otherwise noted, $V_{DD_SW}=3.7V$, $V_{DD_HB}=25V$, $V_{STBYb}=V_{SHDNb}=3.7V$, $R_T=100k\Omega$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
UVLO Release Voltage	V_{RUVLO_HB}		5.6	6.2	6.8	V
UVLO Operate Voltage	V_{DUVLO_HB}		5.0	5.6	6.2	V
UVLO Hysteresis Voltage	ΔV_{UVLO_HB}	$V_{RUVLO_HB} - V_{DUVLO_HB}$	–	0.6	–	V

Enable Control Block

High Side SW ON Resistance	R_{DSSH}	$I_{OSOURCE}=20mA$	–	6.0	8.0	Ω	
Low Side SW ON Resistance	R_{DSL}	$I_{OSINK}=20mA$	–	7.0	9.0	Ω	
Output Current Limit Circuit	Over Current Detection Current	I_{DCTH}	High-Side	230	280	330	mA
		I_{DCTL}	Low-Side	200	250	300	mA
	Over Current Release Current	I_{RCVH}	High-Side	2.5	5	10	mA
		I_{RCVL}	Low-Side	5	10	20	mA
	Output Short Current	I_{SHTH}	$V_{OUT1}=V_{OUT2}=0V$	10	25	50	mA
I_{SHTL}		$V_{OUT1}=V_{OUT2}=V_{DD_HB}$	10	25	50	mA	
Output Rise Time	t_r	$V_{IN}=0$ to 3.3V	–	400	–	ns	
Output Fall Time	t_f	$V_{IN}=0$ to 3.3V	–	400	–	ns	
Rise Dead Time	D_{tr}	$V_{IN}=0$ to 3.3V	–	150	–	ns	
Fall Dead Time	D_{tf}	$V_{IN}=0$ to 3.3V	–	150	–	ns	
Rise Delay Time	t_{d_ON}	$V_{IN}=0$ to 3.3V	–	250	–	ns	
Fall Delay Time	t_{d_OFF}	$V_{IN}=0$ to 3.3V	–	250	–	ns	
Rise – Fall Delay Time Difference	$t_{d_ON} \pm t_{d_OFF}$	$V_{IN}=0$ to 3.3V	–	20	–	ns	
Input Frequency	f_{IN}		–	–	300	kHz	
High Side SW OFF Leak Current	$I_{OLEAKOUTH}$	$V_{SHDNb}=0V$, $V_{DD_HB}=25V$ $V_{OUT1}=V_{OUT2}=0V$	–	–	1	μA	
Low Side SW OFF Leak Current	$I_{OLEAKOUTL}$	$V_{SHDNb}=0V$, $V_{DD_HB}=25V$ $V_{OUT1}=V_{OUT2}=25V$	–	–	1	μA	
OUT pin – VDD pin Potential Difference	V_{PDOV}	$V_{SHDNb}=0V$, $I_{ORH}=20mA$	–	0.7	1.0	V	
GND pin – OUT pin Potential Difference	V_{PDGO}	$V_{SHDNb}=0V$, $I_{ORL}=20mA$	–	0.7	1.0	V	

Shutdown Circuit Block

SHDNb pin High Voltage (Operating Mode)	$V_{IHSHDNb}$		1.6	–	V_{DD_SW}	V
SHDNb pin Low Voltage (Shutdown Mode)	$V_{ILSHDNb}$		0	–	0.6	V
SHDNb pin Pull Down Resistance	R_{PDSDNB}	$V_{SHDNb}=3.3V$	210	300	390	$k\Omega$

Input Circuit Block

IN1, IN2 pin High Voltage	V_{IHIN1} , V_{IHIN2}		1.6	–	V_{DD_SW}	V
IN1, IN2 pin Low Voltage	V_{ILIN1} , V_{ILIN2}		0	–	0.6	V
IN1, IN2 pin Input Current	I_{IIN1} , I_{IIN2}	$V_{IN}=3.3V$	–	–	1	μA

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■ ELECTRICAL CHARACTERISTICS

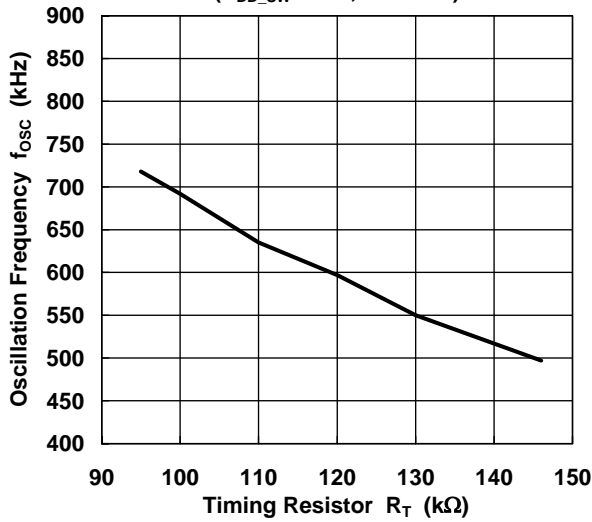
General Characteristics

(Unless otherwise noted, $V_{DD_SW}=3.7V$, $V_{DD_HB}=25V$, $V_{STBYb}=V_{SHDNb}=3.7V$, $R_T=100k\Omega$, $T_a=25^\circ C$)

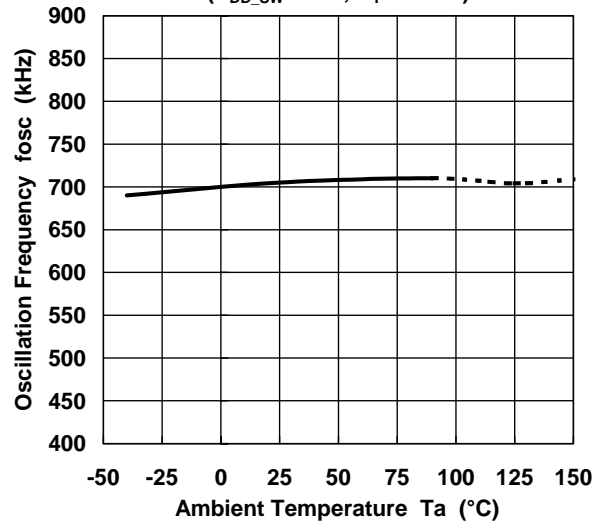
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
STBYb pin High Voltage (Operating Mode)	$V_{IHSTBYb}$		1.6	–	V_{DD_SW}	V
STBYb pin Low Voltage (Standby Mode)	$V_{ILSTBYb}$		0	–	0.6	V
STBYb pin Pull Down Resistance	$R_{PDSTBYb}$	$V_{STBYb}=3.3V$	210	300	390	$k\Omega$
FLT pin Low Level Output Voltage	V_{LFLT}	$I_{FLT}=500\mu A$	–	0.25	0.5	V
FLT pin OFF Leak Current	$I_{OLEAKFLT}$	$V_{FLT}=5.5V$	–	–	1	μA
Quiescent Current (Switching Regulator Block)	I_{QSW}	$R_T=100k\Omega$, No Load	–	1.9	2.8	mA
Quiescent Current (Half Bridge Driver Block)	I_{QHB}	$f_{IN1}=f_{IN2}=10kHz$ antiphase 50% Duty Cycle	–	0.7	1.0	mA
Quiescent Current (Standby)	I_{QSTBY}	$V_{DD_HB}=0V$, $V_{STBYb}=V_{SHDNb}=0V$	–	0.9	1.8	μA

■ TYPICAL CHARACTERISTICS (Boost Converter Block)

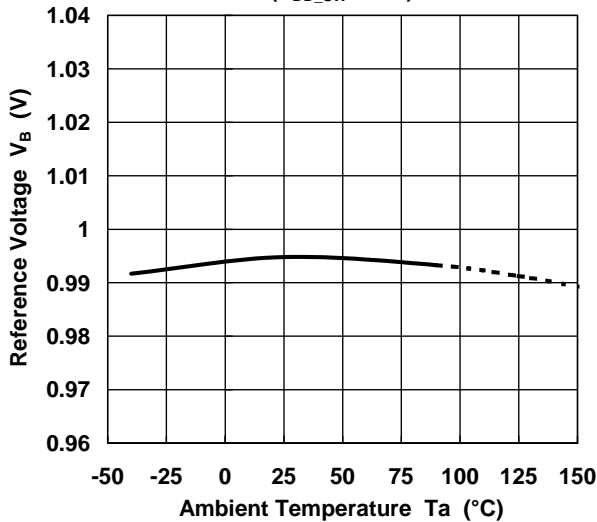
Timing Resistor vs. Oscillation Frequency
($V_{DD_SW}=3.7V$, $T_a=25^\circ C$)



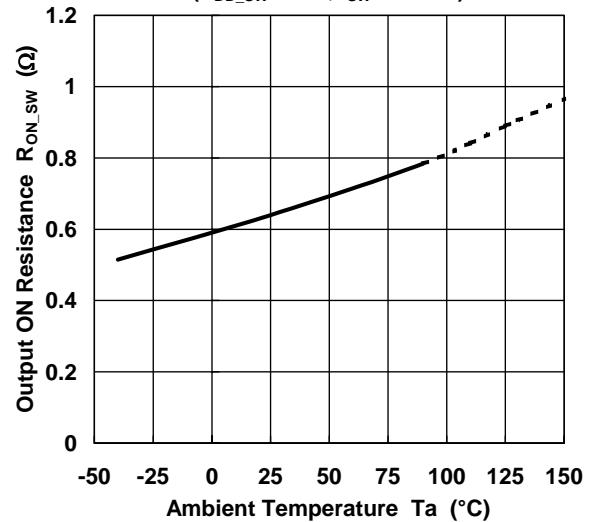
Oscillation Frequency vs. Temperature
($V_{DD_SW}=3.7V$, $R_T=100k\Omega$)



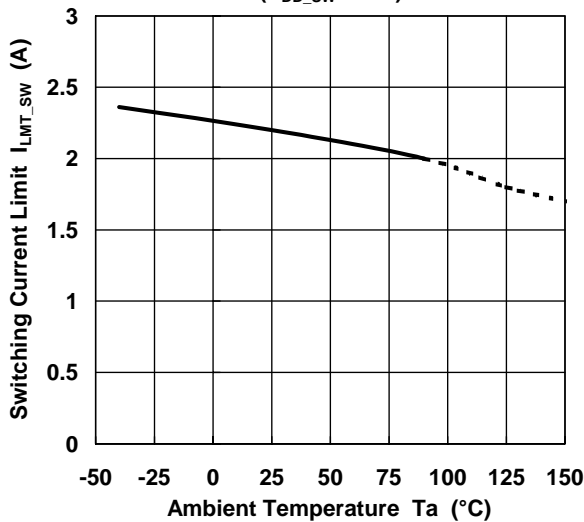
Reference Voltage vs. Temperature
($V_{DD_SW}=3.7V$)



Output ON Resistance vs. Temperature
($V_{DD_SW}=3.7V$, $I_{SW}=100mA$)

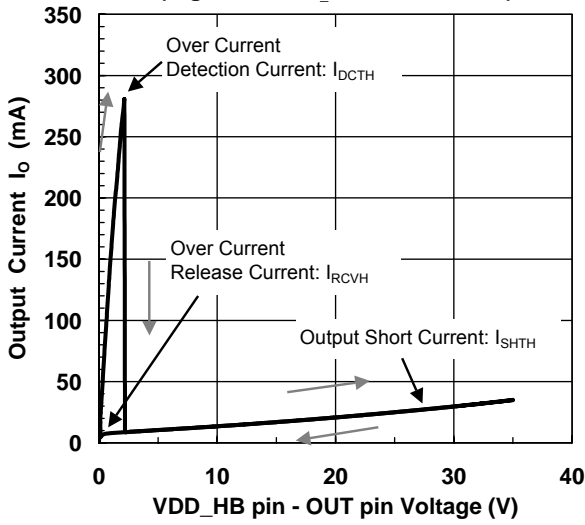


Switching Current Limit vs. Temperature
($V_{DD_SW}=3.7V$)

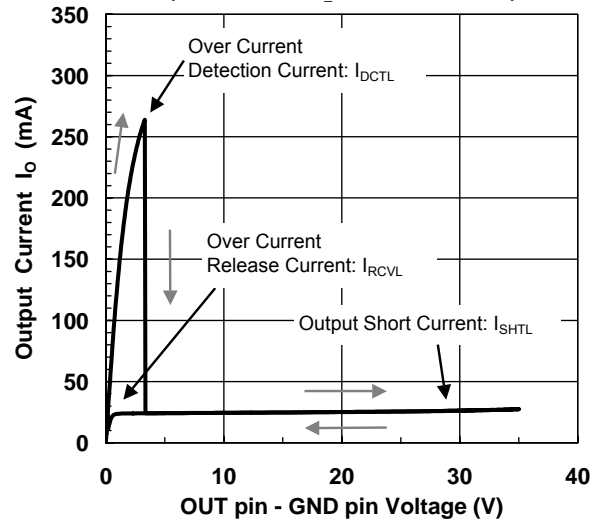


■ TYPICAL CHARACTERISTICS (Half Bridge Driver Block)

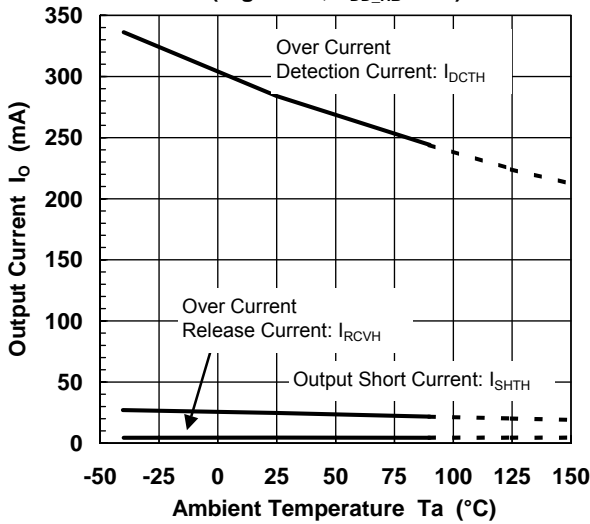
Output Current Limit Characteristics (High Side, $V_{DD_HB}=35V$, $T_a=25^\circ C$)



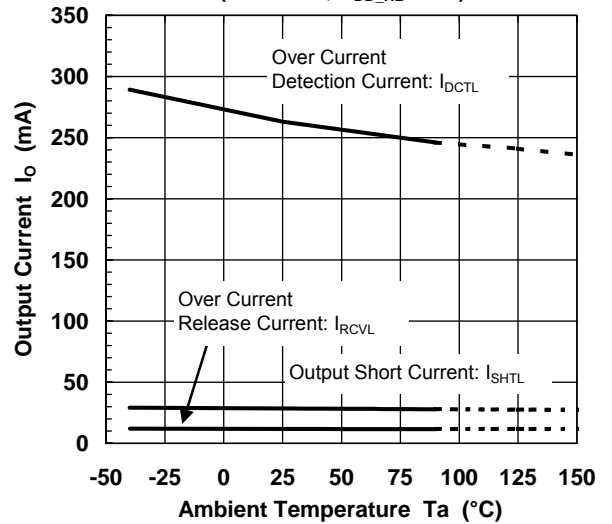
Output Current Limit Characteristics (Low Side, $V_{DD_HB}=35V$, $T_a=25^\circ C$)



Output Current Limit vs. Temperature (High Side, $V_{DD_HB}=35V$)

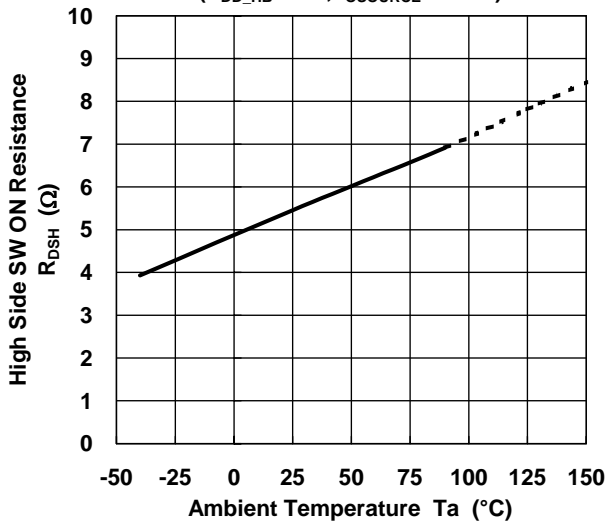


Output Current Limit vs. Temperature (Low Side, $V_{DD_HB}=35V$)

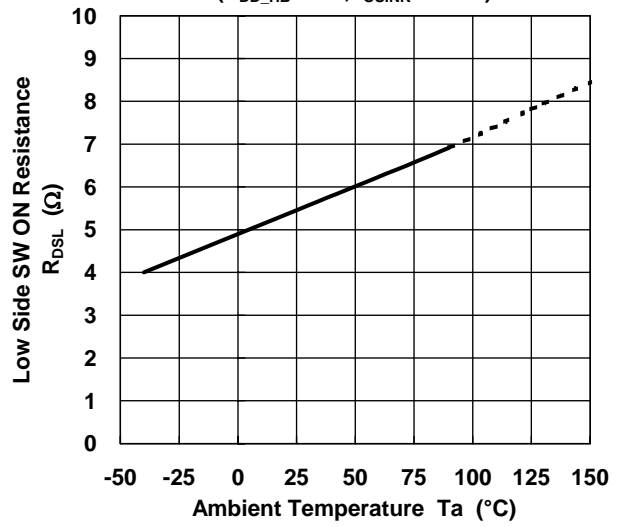


■ TYPICAL CHARACTERISTICS (Half Bridge Driver Block)

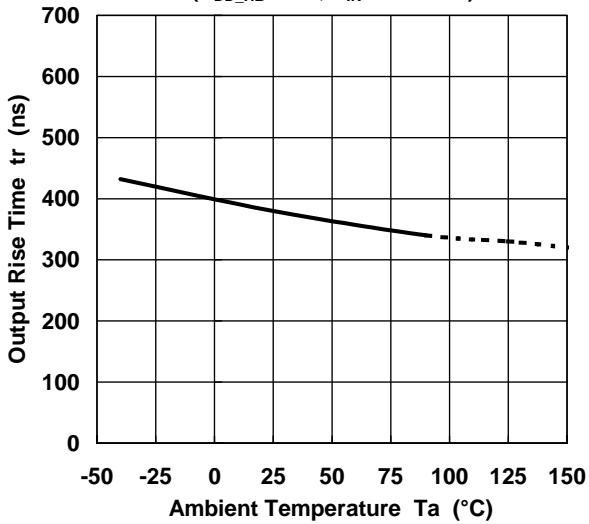
High Side SW ON Resistance vs. Temperature
($V_{DD_HB}=25V$, $I_{OSOURCE}=20mA$)



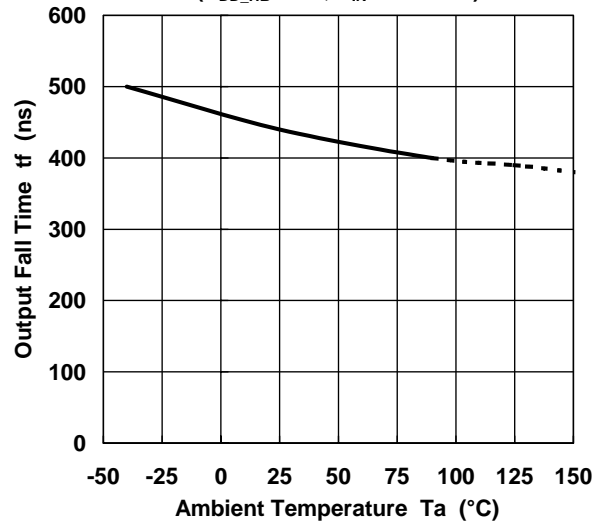
Low Side SW ON Resistance vs. Temperature
($V_{DD_HB}=25V$, $I_{OSINK}=20mA$)



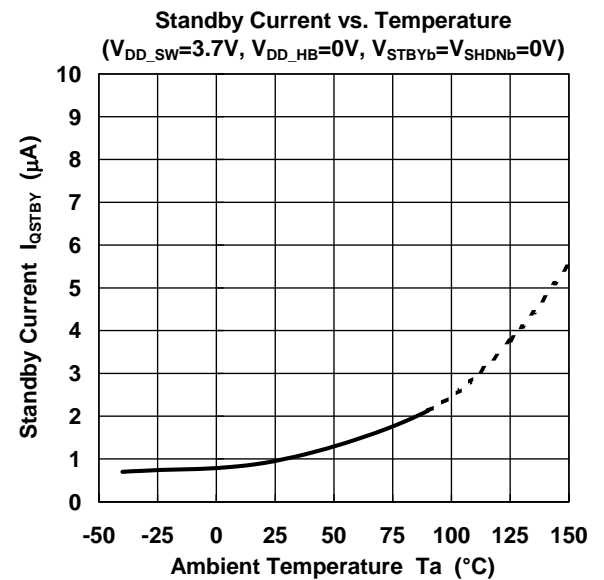
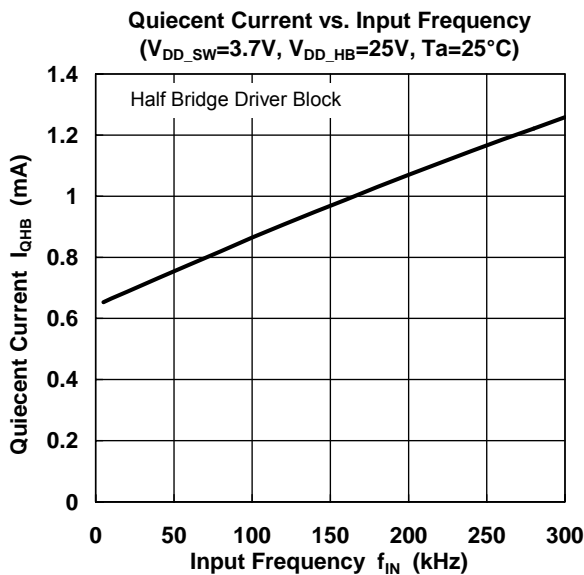
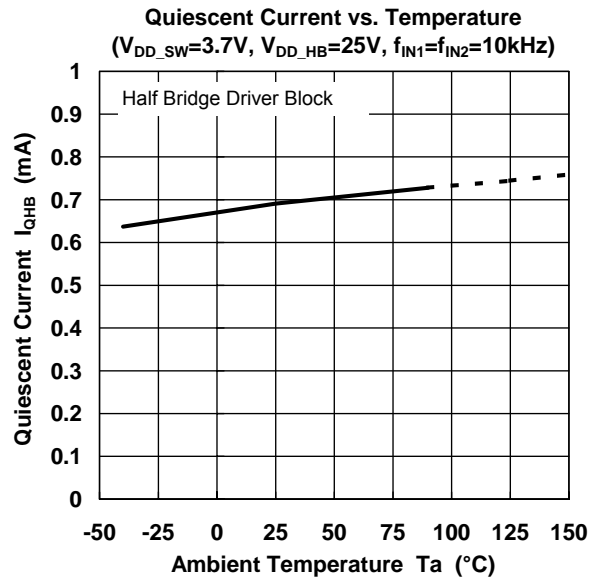
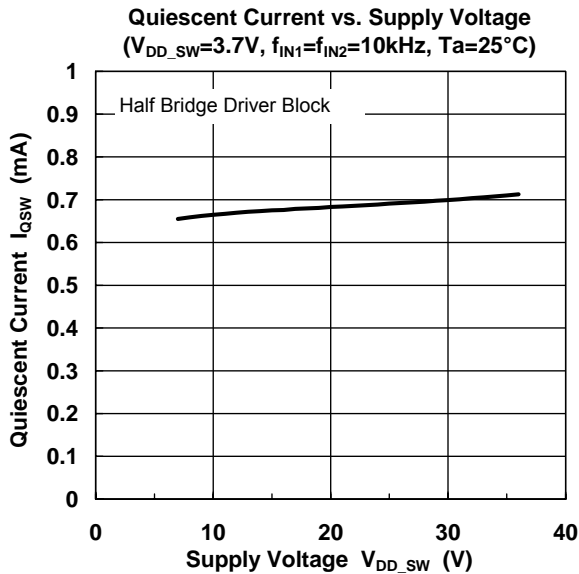
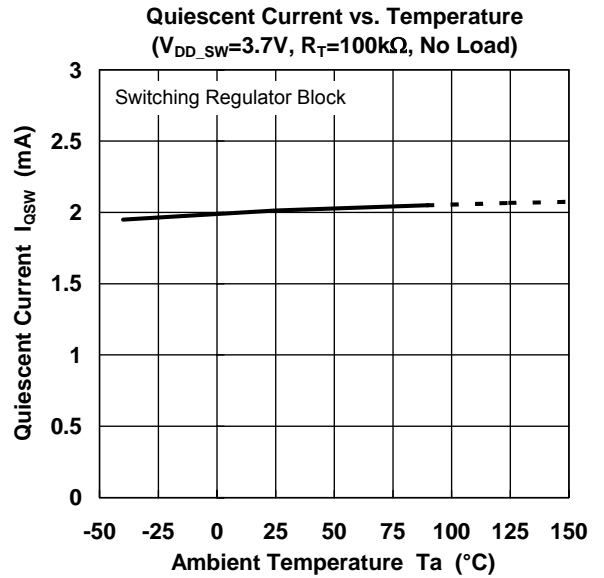
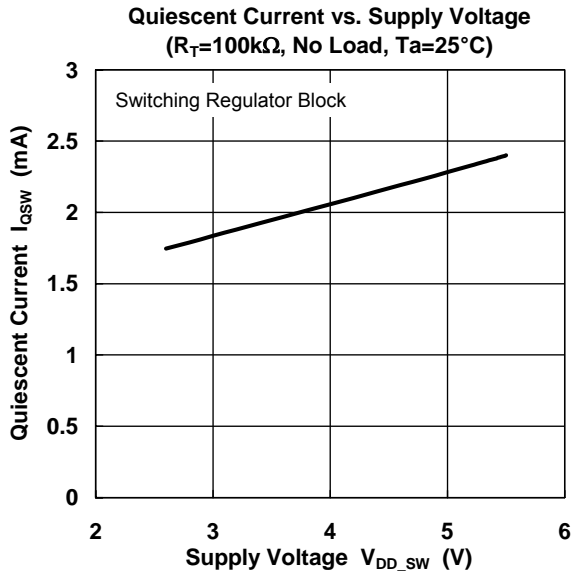
Output Rise Time vs. Temperature
($V_{DD_HB}=25V$, $V_{IN}=0$ to 3.3V)



Output Fall Time vs. Temperature
($V_{DD_HB}=25V$, $V_{IN}=0$ to 3.3V)



■ TYPICAL CHARACTERISTICS (General Characteristics)



■ Switching Regulator Block Pin Operation Table

INPUT		OUTPUT			Mode
STBYb	VDD_SW	FLT	Feed back Switch	Power MOS FET	
L	–	Hi-Z	OFF	OFF	Stand-by
H	$< V_{DUVLO_SW}$	L	OFF	OFF	UVLO
H	$\geq V_{RUVLO_SW}$	Hi-Z	ON	ON	Active

INPUT		OUTPUT			Mode
Tj	I _{sw}	FLT	Feed back Switch	Power MOS FET	
$>165^{\circ}\text{C}$	–	L	OFF	OFF	TSD (*4)
–	$\geq I_{LMTSW}$	L	OFF	OFF	OCP (*5)

(*4) After the TSD function operates, it returns by $T_j < 125^{\circ}\text{C}$.

(*5) Power MOSFET is controlled by a pulse-by-pulse after an OCP function.

■ Switching Regulator Block Pin Operation Table

INPUT		OUTPUT	
IN1	IN2	OUT1	OUT2
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

INPUT				OUTPUT			Mode	
IN1, IN2	STBYb	SHDNb	VDD_HB	FLT	OUT1	OUT2	SW.REG	Half Bridge Driver
L or H	L	L	–	Hi-Z	Hi-Z	Hi-Z	Stand-by	
L or H	L	H	–	Hi-Z	Hi-Z	Hi-Z	Stand-by	
L or H	H	L	$< V_{DUVLO_HB}$	L	Hi-Z	Hi-Z	Active	UVLO
L or H	H	L	$\geq V_{RUVLO_HB}$	Hi-Z	Hi-Z	Hi-Z	Active	Shutdown
L or H	H	H	$< V_{DUVLO_HB}$	L	Hi-Z	Hi-Z	Active	UVLO
L or H	H	H	$\geq V_{RUVLO_HB}$	Hi-Z	L or H	L or H	Active	

INPUT			OUTPUT			Mode
Tj	I _{OUT1}	I _{OUT2}	FLT	OUT1	OUT2	
$>165^{\circ}\text{C}$	–	–	L	Hi-Z	Hi-Z	TSD (*4)
–	$\geq I_{DCTH1}, I_{DCTL1}$	–	Hi-Z	I _{SHTH1} , I _{SHTL1}	L or H	CC (*6)
–	–	$\geq I_{DCTH2}, I_{DCTL2}$	Hi-Z	L or H	I _{SHTH2} , I _{SHTL2}	CC (*6)

(*6) After CC(Constant Current) function, an output is controlled by constant current.

■ Timing Chart

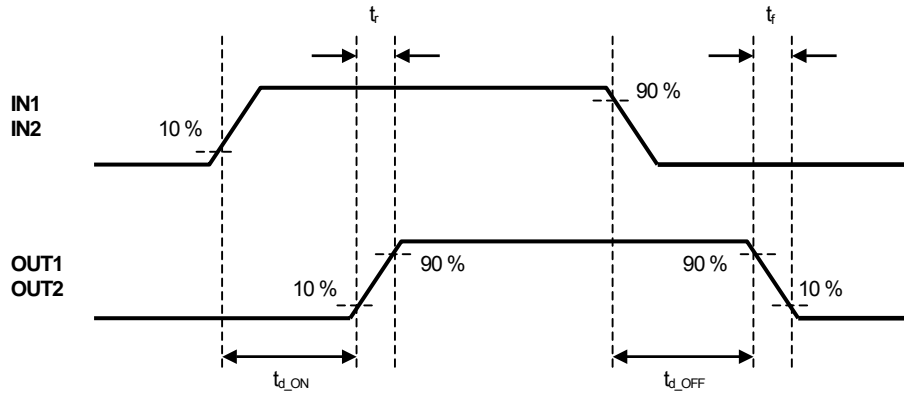
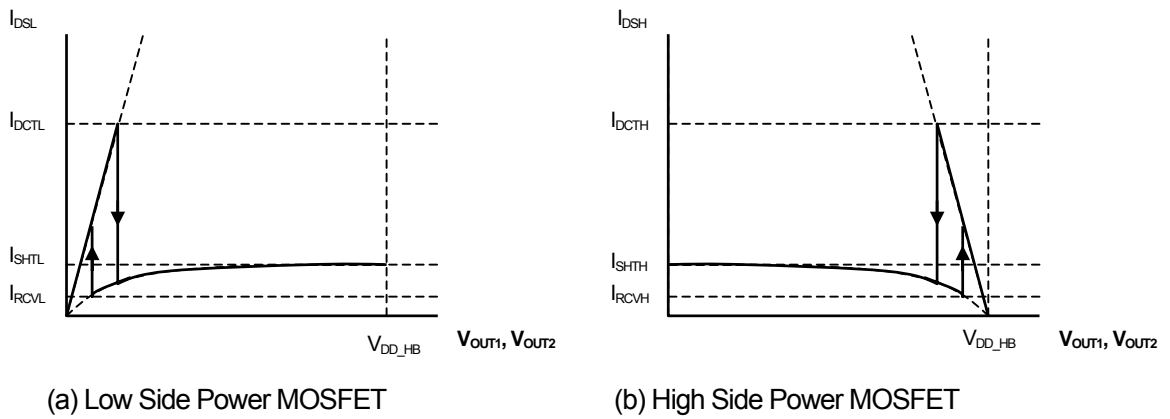


Fig. 1. Output Rise/Fall Time, Rise/Fall Delay Time

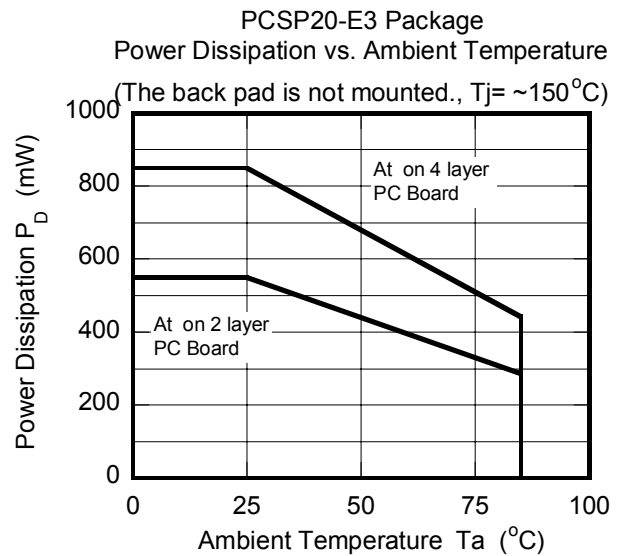
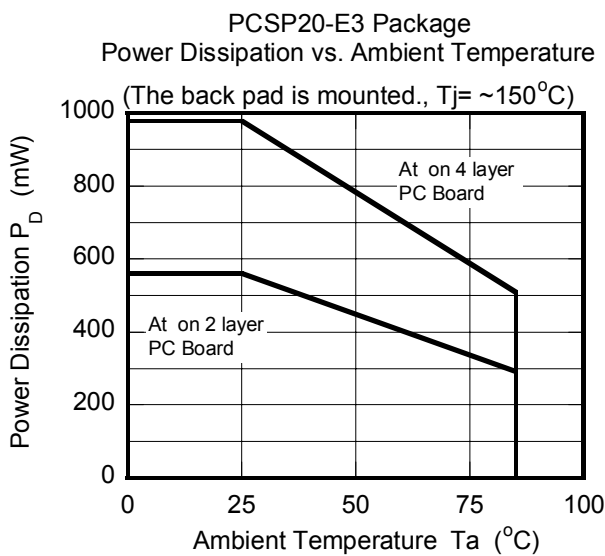


(a) Low Side Power MOSFET

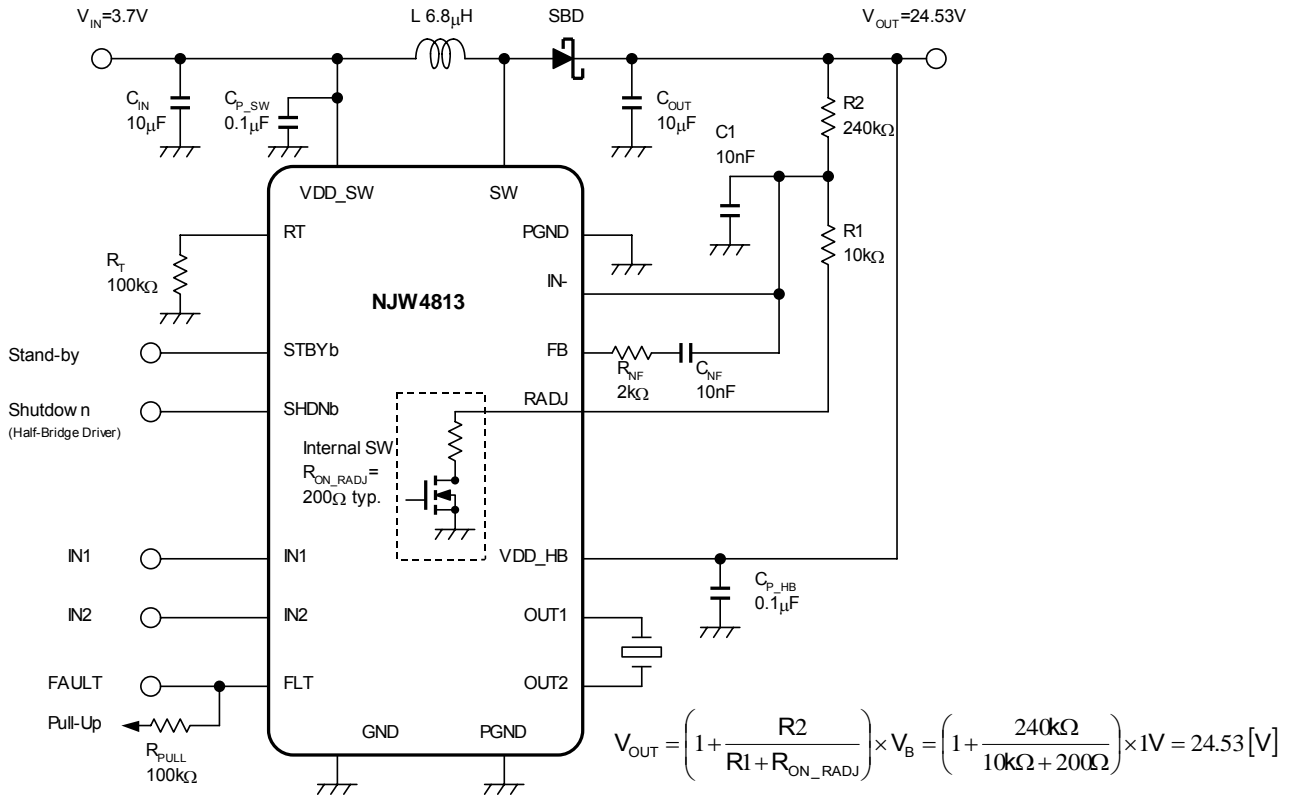
(b) High Side Power MOSFET

Fig. 2. Output Current Limit Circuit

■ Power Dissipation vs. Ambient Temperature



APPLICATION EXAMPLE



MEMO

[CAUTION]

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