

Low-Voltage Dual-SPDT (0.5Ω) Analog Switch with Negative Swing Audio Capability

Features

- Negative Signal Handling Capability at all Ports
- Low On-Resistance: 0.5Ω at 3.0V Supply
- 0.25Ω Maximum R_{ON} Flatness for 3.0V Supply
- -3dB Bandwidth: 85MHz
- Low-ICCT Current Over an Expanded Control Input Range
- Wide VDD Range: 1.65V to 4.3V
- Power-off Protection on Common Ports
- Rail-to-Rail Signal Range
- High Off Isolation: -80dB @ 100kHz
- Crosstalk Rejection Reduces Signal Distortion: -80dB @ 100kHz
- Extended Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
-10-contact UQFN (ZM10)

Description

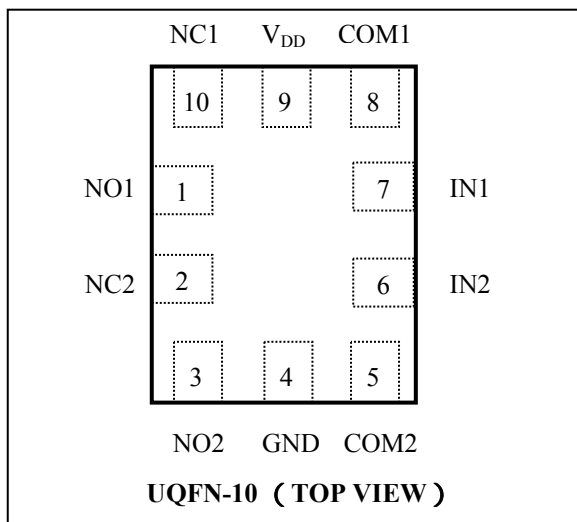
PI3A268C is a dual, fast single-pole double throw (SPDT) CMOS switch with negative signal handling capability at all ports. It can be used as an analog switch or as a low-delay bus switch. Operating over a wide power supply voltage ranges from 1.65V to 4.3V, PI3A268C processes a low on-resistance and distortion. Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

PI3A268C dissipates a very low supply current even when the control voltage is lower than supply. This feature suits mobile handset applications by allowing direct interface with the general-purpose I/Os of baseband processors with minimal battery consumption.

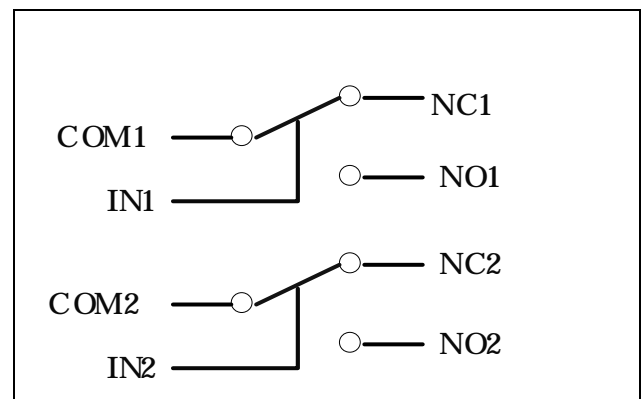
Application

- Cell Phones, PDAs, MP3 Players
- Portable Instrumentation
- Computer Peripherals
- Speaker Headset Switching
- Power Routing
- Relay Replacement
- Audio and Video Signal Routing
- PCMCIA Cards
- Modems

Pin Assignment



Functional Block Diagram



Maximum Ratings

Storage Temperature.....	-65 to +150
Ambient Temperature with Power Applied.....	-40 to +85
Supply Voltage V_{DD}	-0.5V to +4.6V
Control Input Voltage V_{INx}	-0.5V to +4.6V
DC Input Voltage V_{INPUT}	$V_{DD} - 4.6V$ to $V_{DD} + 0.3V$
Continuous Current NO_NC_COM_.....	±350mA
Peak Current NO_NC_COM_ (pulsed at 1ms 50% duty cycle)	±400mA
Peak Current NO_NC_COM_ (pulsed at 1ms 10% duty cycle)	±500mA

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Control input must be held HIGH or LOW; it must not float.

Pin Description

Pin	Name	Description
1, 3	NO _x	Data Ports (Normally open)
4	GND	Ground
2, 10	NC _x	Data Ports (Normally closed)
5, 8	COM _x	Common Output / Data Ports
9	V_{DD}	Positive Power Supply
6, 7	IN _x	Logic Control Pins

Logic Function Table

Logic Input (IN _x)	Function
0	NC _x Connected to COM _x
1	NO _x Connected to COM _x

Note: x = 1 or 2

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	1.65	-	4.3	V
V_{IN}	Control Input Voltage	-	0	-	4.3	V
V_{INPUT}	Switch Input Voltage	-	$V_{DD} - 4.6V$	-	V_{DD}	V
T_A	Operating Temperature	-	-40	25	85	°C
t_r, t_f	Input Rise and Fall Time	-	0	-	10	ns/V

Electrical Characteristics

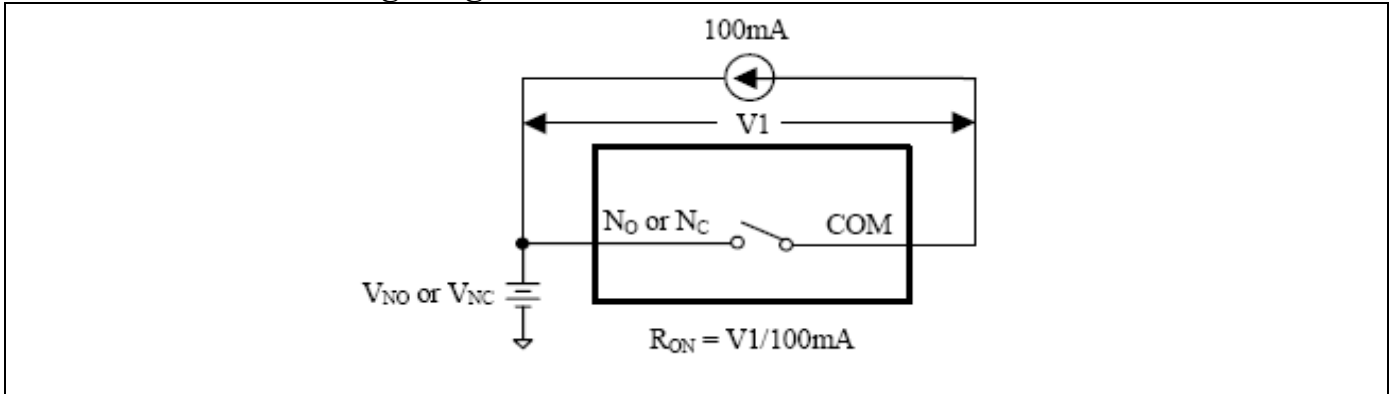
(T_A = -40°C to 85°C, unless otherwise noted. Typical values are at V_{DD}=3.0V and +25°C.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ANALOG SWITCH						
Analog Signal Range	V _{NO} , V _{NC} , V _{COM}		0	-	V _{DD}	V
On-Resistance	R _{ON}	V _{DD} = 4.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = -0.3V/0V/0.7V/3.6V/4.3V <i>Test Circuit Figure 1</i>	-	0.40	-	Ω
		V _{DD} = 3.0V, I _{COM} = 100mA, V _{NO} or V _{NC} = -1.6V/0V/0.7V/2.3V/3.0V <i>Test Circuit Figure 1</i>	-	0.50	0.8	
		V _{DD} = 2.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = -2.3V/0V/0.7V/1.6V/2.3V <i>Test Circuit Figure 1</i>	-	0.60	-	
		V _{DD} = 1.65V, I _{COM} = 100mA, V _{NO} or V _{NC} = -2.95V/0V/1.65V <i>Test Circuit Figure 1</i>	-	1.00	-	
On-Resistance Match Between Channels	ΔR _{ON}	V _{DD} = 4.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = 0.7V, <i>Test Circuit Figure 1</i>	-	0.04	0.13	Ω
		V _{DD} = 3.0V, I _{COM} = 100mA, V _{NO} or V _{NC} = 0.7V, <i>Test Circuit Figure 1</i>	-	0.06	0.13	
		V _{DD} = 2.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = 0.7V, <i>Test Circuit Figure 1</i>	-	-	0.12	
		V _{DD} = 1.65V, I _{COM} = 100mA, V _{NO} or V _{NC} = 0.7V, <i>Test Circuit Figure 1</i>	-	-	1.0	
On-Resistance Flatness	R _{ONF}	V _{DD} = 4.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = -0.3V, 0V, 4.3V, <i>Test Circuit Figure 1</i>	-	-	0.25	Ω
		V _{DD} = 3.0V, I _{COM} = 100mA, V _{NO} or V _{NC} = -1.6V, 0V, 3.0V, <i>Test Circuit Figure 1</i>	-	-	0.25	
		V _{DD} = 2.3V, I _{COM} = 100mA, V _{NO} or V _{NC} = -2.3V, 0V, 2.3V, <i>Test Circuit Figure 1</i>	-	0.5	-	
		V _{DD} = 1.65V, I _{COM} = 100mA, V _{NO} or V _{NC} = -2.95V, 0V, 1.65V, <i>Test Circuit Figure 1</i>	-	0.6	-	
Power-Off Leakage Current (Common Port)	I _{OFF}	Common Port (COM1, COM2), V _{IN} =0 to 4.3V, V _{DD} =0V, NC, NO floating	-1	-	1	μA
Source-Off Leakage Current	I _{OFF (NO)} or I _{OFF (NC)}	V _{DD} =3.0V, V _{NO} or V _{NC} = -1.6V and 3.0V	-0.25	-	0.25	μA
Channel On Leakage Current	I _{NC(ON)} , I _{NO(ON)} , I _{COM(ON)}	V _{DD} =3.0V, V _{NO} or V _{NC} = -1.6V and 3.0V	-0.15	-	0.15	
Supply Current	I _{CC}	V _{DD} =4.3V, V _{IN} =0 or V _{DD}	-0.5	-	0.5	μA
Increase in I _{CC} per Input	I _{CCT}	V _{DD} =4.3V, Input at 2.6V	-	3	10.0	
		V _{DD} =4.3V, Input at 1.8V	-	7	15.0	
DIGITAL INPUTS						
Input Logic High	V _{IH}	V _{DD} =3.60V to 4.3V	1.70	-	-	V
		V _{DD} =3.00V to 3.60V	1.50	-	-	
		V _{DD} =2.70V to 3.00V	1.35	-	-	
		V _{DD} =2.30V to 2.70V	1.30	-	-	
		V _{DD} =1.65V to 2.30V	0.90	-	-	
Input Logic Low	V _{IL}	V _{DD} =3.60V to 4.30V	-	-	0.6	
		V _{DD} =2.70V to 3.60V	-	-	0.5	
		V _{DD} =2.30V to 2.70V	-	-	0.4	
		V _{DD} =1.65V to 2.30V	-	-	0.4	
IN Input Leakage Current	I _{IN}	V _{IN} =0 or V _{DD}	-0.5	-	0.5	μA
To be continued.						

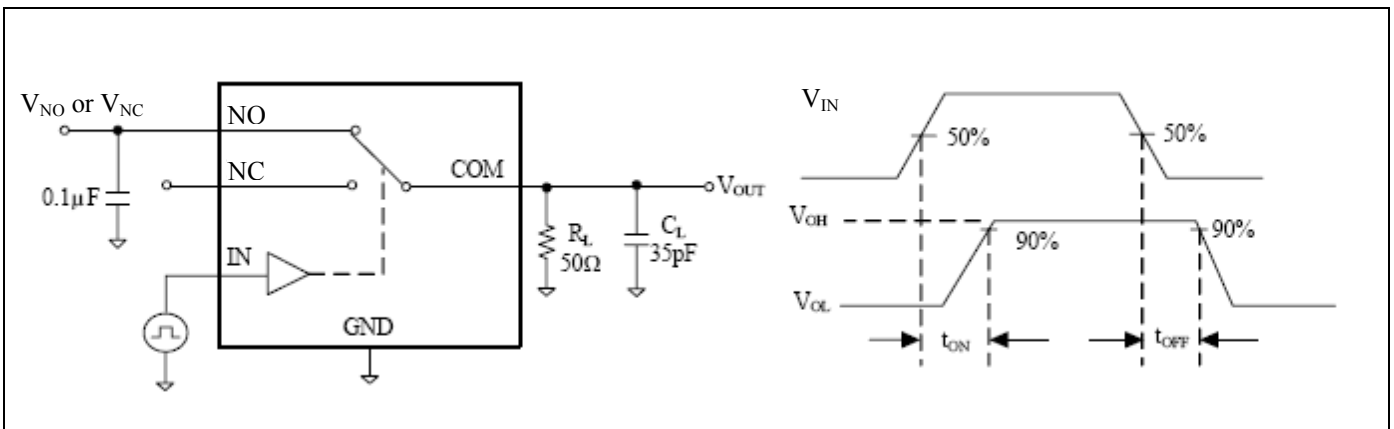
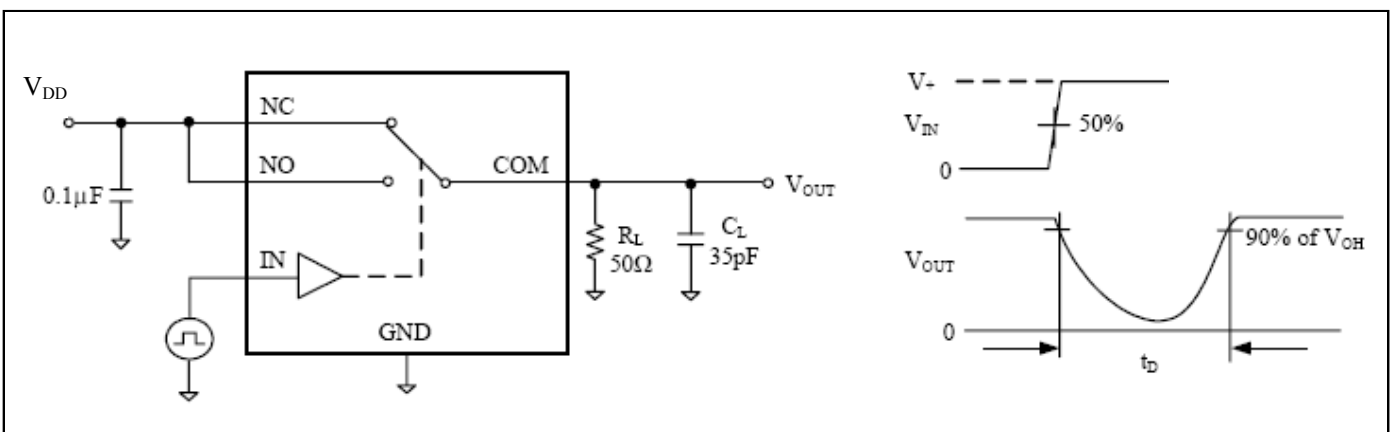
Continuously.							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{DD}=3.60V$ to $4.30V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	50	ns	
		$V_{DD}=2.70V$ to $3.60V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	50		
		$V_{DD}=2.30V$ to $2.70V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	50		
		$V_{DD}=1.65V$ to $2.30V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	40	-		
Turn-Off Time	t_{OFF}	$V_{DD}=3.60V$ to $4.30V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	50	ns	
		$V_{DD}=2.70V$ to $3.60V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	55		
		$V_{DD}=2.30V$ to $2.70V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	-	60		
		$V_{DD}=1.65V$ to $2.30V$, $V_{IH}=1.5V$, $V_{IL}=0V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 2.	-	60	-		
Break-Before-Make Delay	t_{BBM}	$V_{DD}=3.60V$ to $4.30V$, $V_{IH}=1.5V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 3.	-	6	-	ns	
		$V_{DD}=2.70V$ to $3.60V$, $V_{IH}=1.5V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 3.	-	7	-		
		$V_{DD}=2.30V$ to $2.70V$, $V_{IH}=1.5V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 3.	-	10	-		
		$V_{DD}=1.65V$ to $2.30V$, $V_{IH}=1.5V$, $R_L=50\Omega$, $C_L=35pF$. See Test Circuit Figure 3.	-	21	-		
NC-NO and COM-NC/NO Off-Isolation	O_{ISO}	$V_{DD}=1.65V$ to $4.3V$, $V_{BIAS}=1.5V$, $V_{IN}=0dBm$, $V_{IH}=1.5V$, $V_{IL}=0V$. See Test Circuit Figure 4 and Figure 5	100kHz	-	-80	-	dB
Channel-to-Channel Crosstalk	X_{TALKD}	$V_{DD}=1.65V$ to $4.3V$, $V_{BIAS}=1.5V$, $V_{IN}=0dBm$, $V_{IH}=1.5V$, $V_{IL}=0V$. See Test Circuit Figure 6	100kHz	-	-80	-	dB
3dB Bandwidth	f_{3dB}	$V_{DD}=1.65V$ to $4.3V$, $V_{IN}=0dBm$, $V_{IH}=1.5V$, $V_{IL}=0V$. See Test Circuit Figure 7.	-	85	-	MHz	
Charge Injection Select Input to Common I/O	Q	$V_{DD}=1.65V$ to $4.30V$, $V_{IN} = GND$, $R_S = 0$, $C_L = 1nF$, $V_{IH}=1.5V$, $V_{IL}=0V$ See Test Circuit Figure 8.	-	52	-	pC	
Total Harmonic Distortion	THD	$V_{DD}=1.65V$ to $4.30V$, $f=20Hz$ to $20kHz$, $R_L=32\Omega$, $V_{IN}=2V_{PP}$, $V_{BIAS}=0V$	-	0.06	-	%	

Capacitance

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Control Pin Input Capacitance	C_{IN}	$V_{DD}=0V$, $f=1MHz$,	-	6	-	pF
NC Off Capacitance	$C_{NC(OFF)}$	$V_{DD}=3.3V$, $f=1MHz$, See Test Circuit Figure 9.	-	21	-	
NO Off Capacitance	$C_{NO(OFF)}$	$V_{DD}=3.3V$, $f=1MHz$, See Test Circuit Figure 9.	-	21	-	
NC On Capacitance	$C_{NC(ON)}$	$V_{DD}=3.3V$, $f=1MHz$, See Test Circuit Figure 10.	-	65	-	
NO On Capacitance	$C_{NO(ON)}$	$V_{DD}=3.3V$, $f=1MHz$, See Test Circuit Figure 10.	-	65	-	

Test Circuits and Timing Diagrams

Figure 1. On Resistance
Notes:

1. Unused input (NC or NO) must be grounded.


Figure 2. Switching Times

Figure 3. Break Before Make Interval Timing

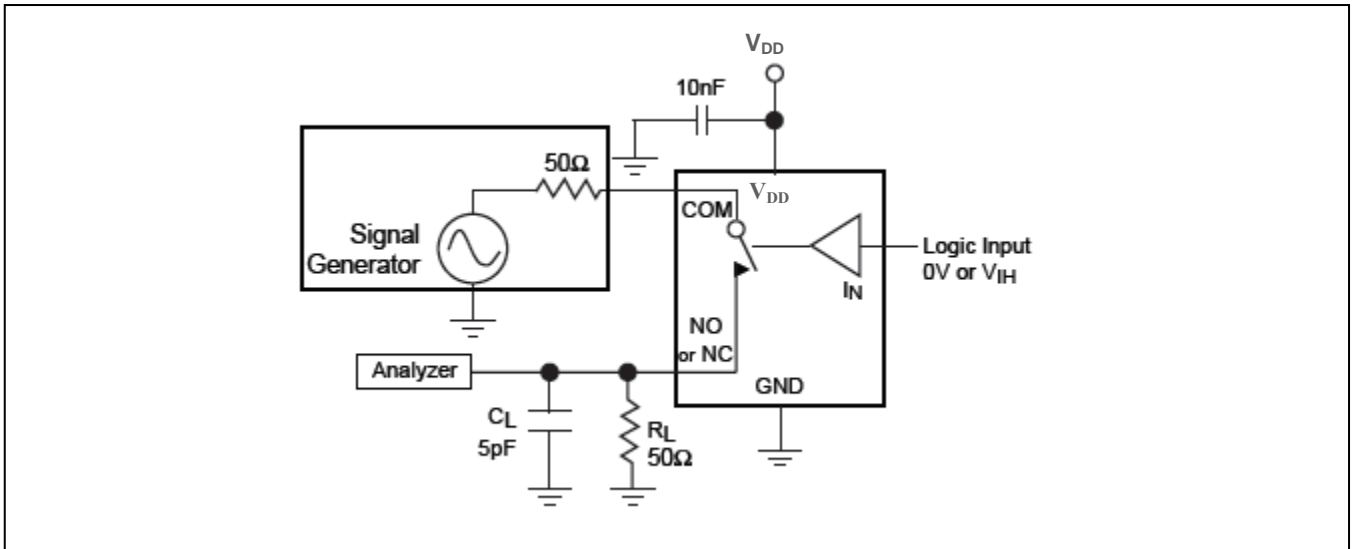


Figure 4. COM-NC/NO Isolation

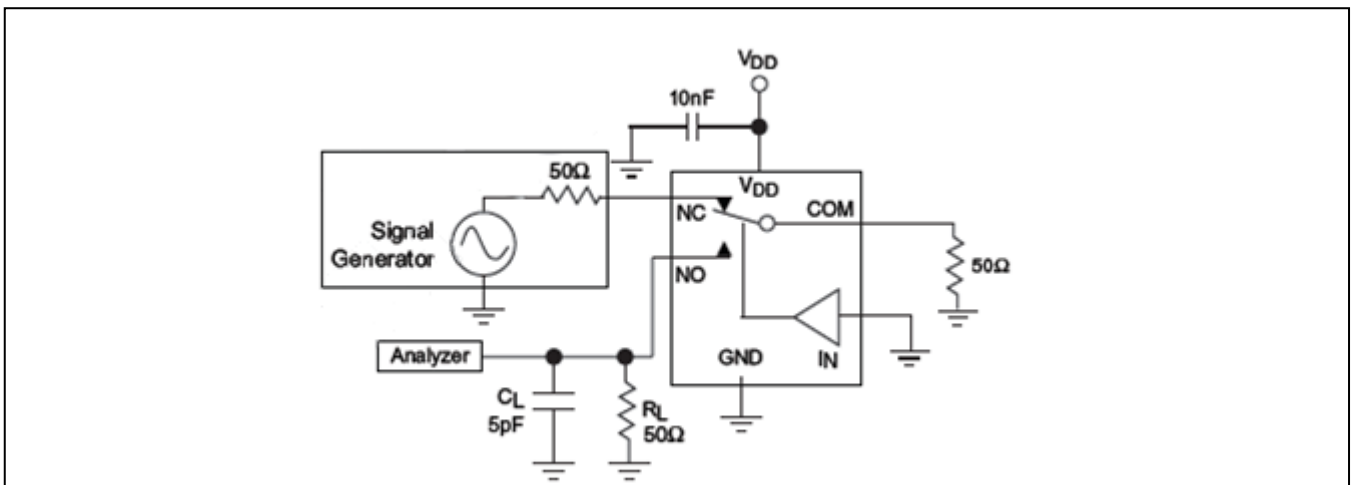


Figure 5. NC-NO Isolation

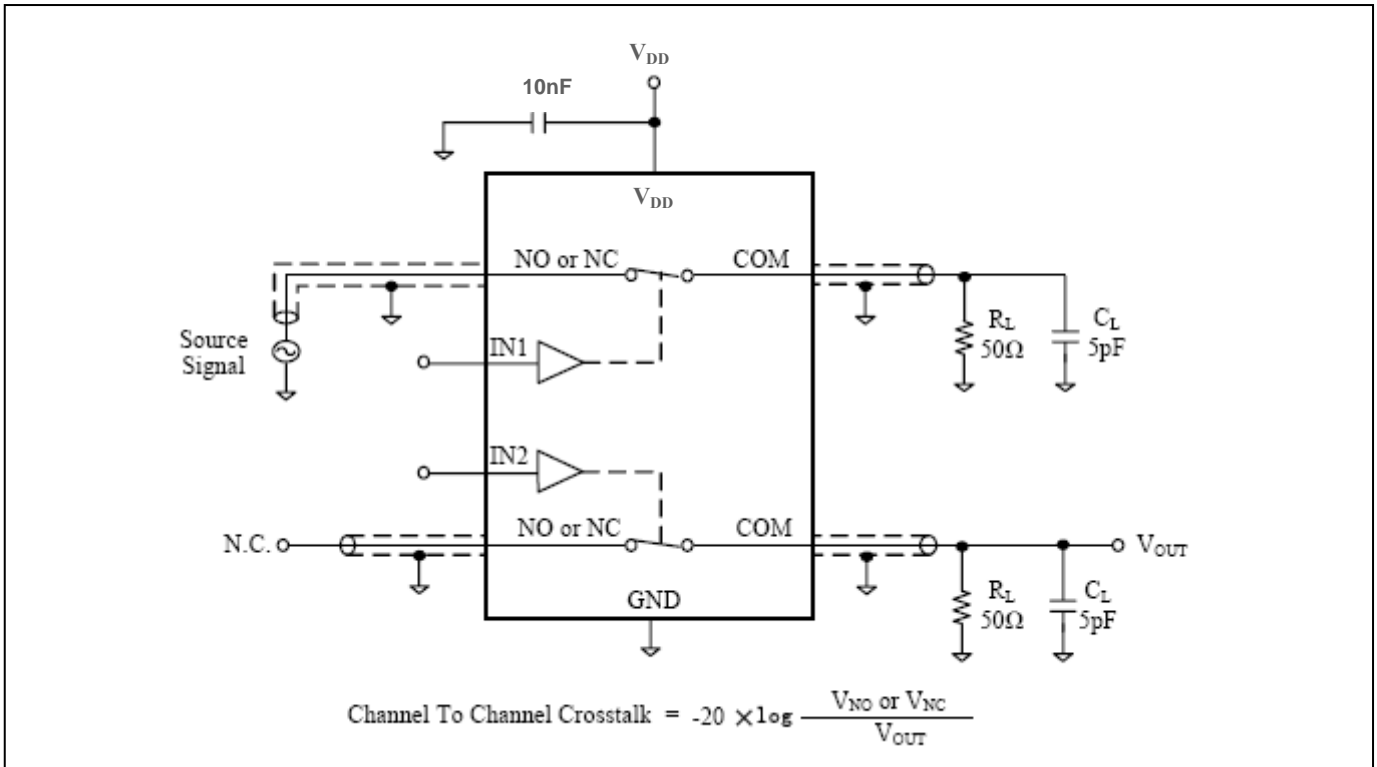


Figure 6. Channel-to-Channel Crosstalk

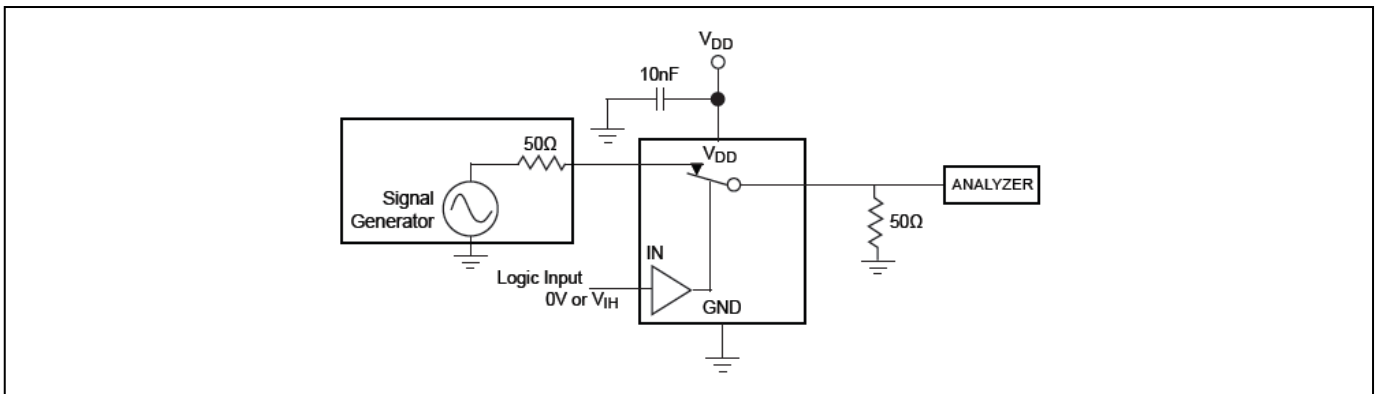


Figure 7. Bandwidth

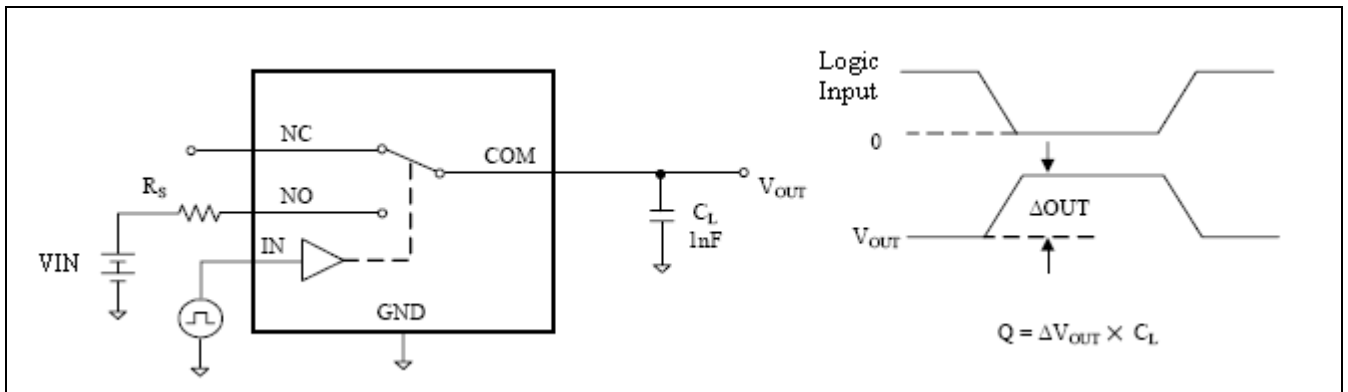


Figure 8. Charge Injection

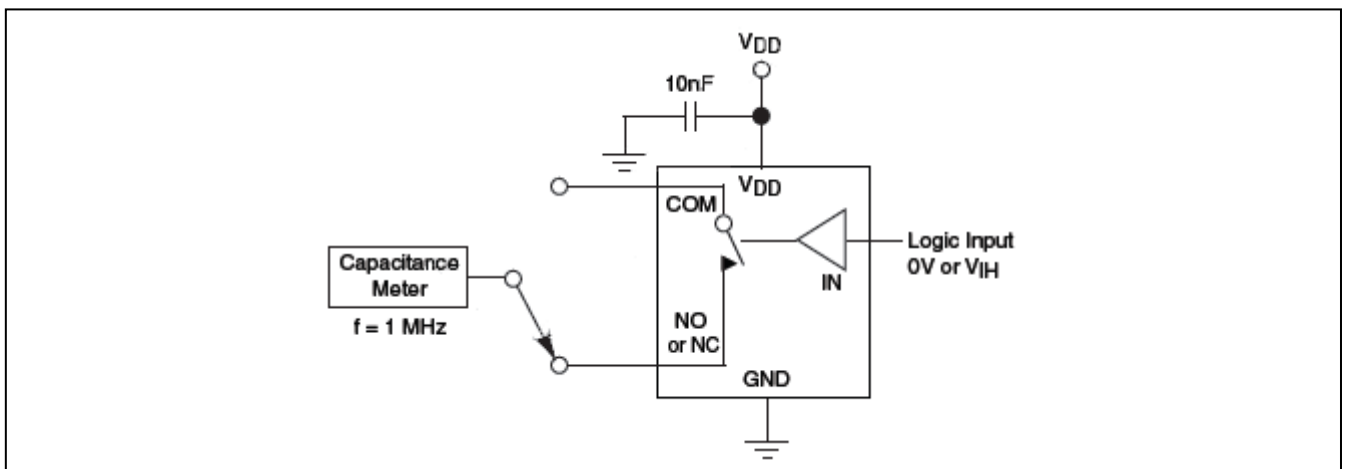


Figure 9. Channel Off Capacitance

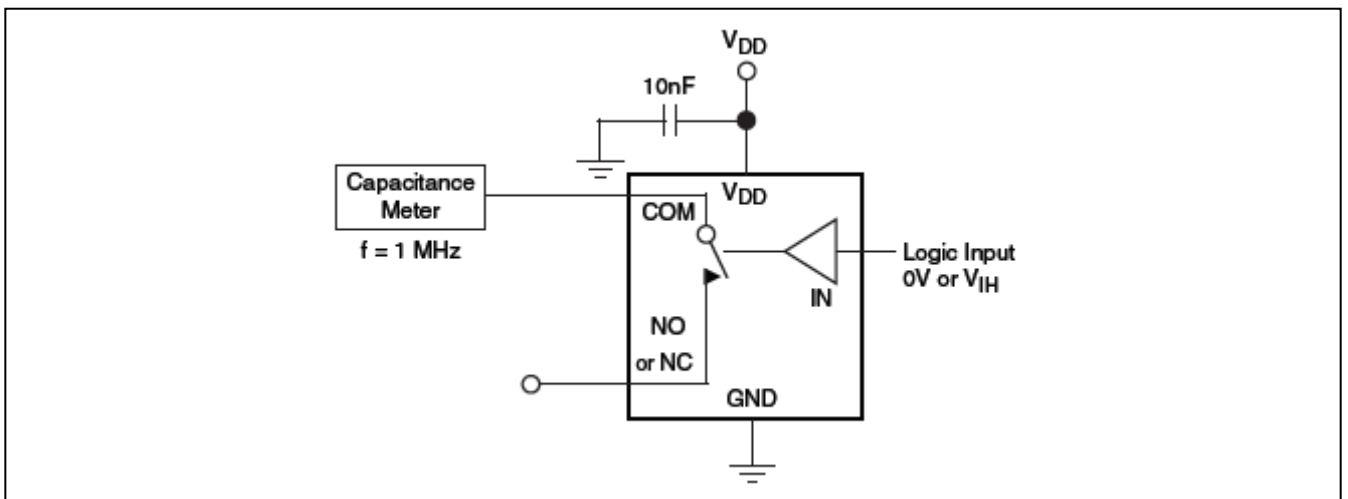
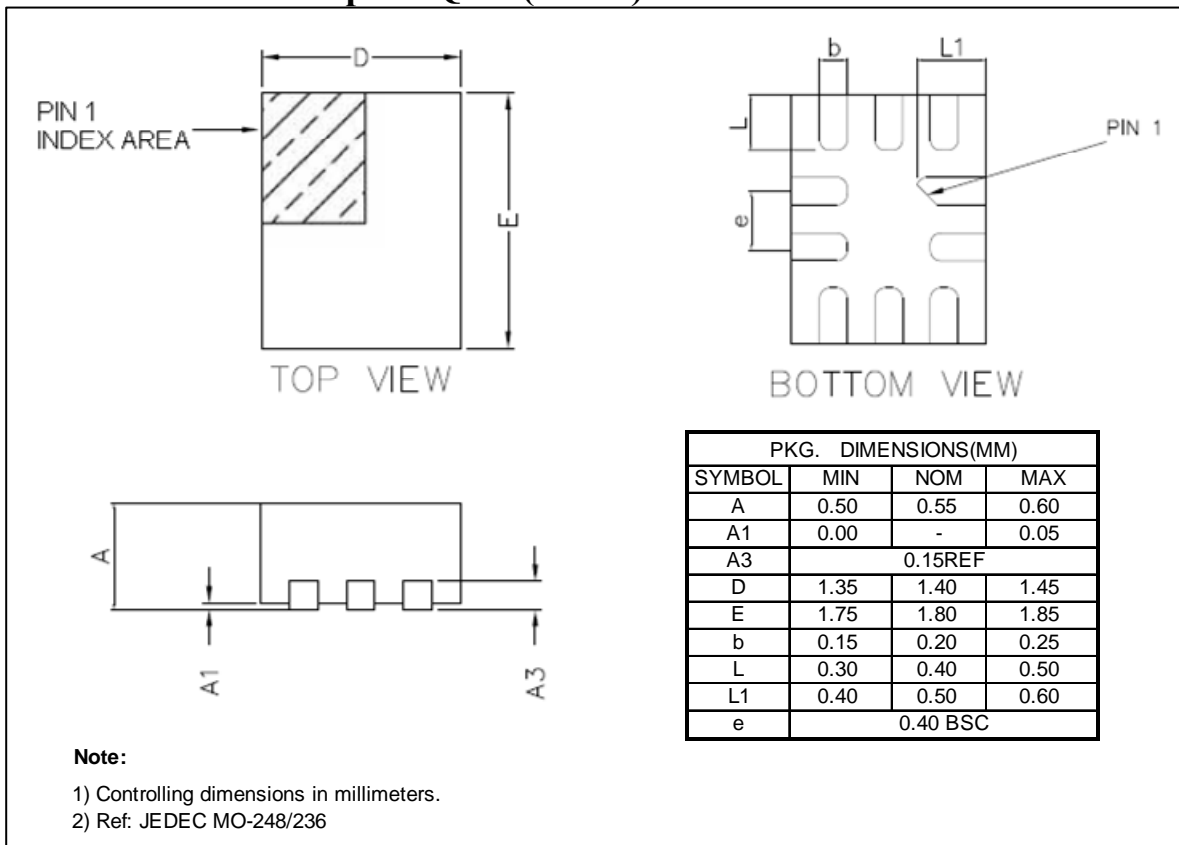
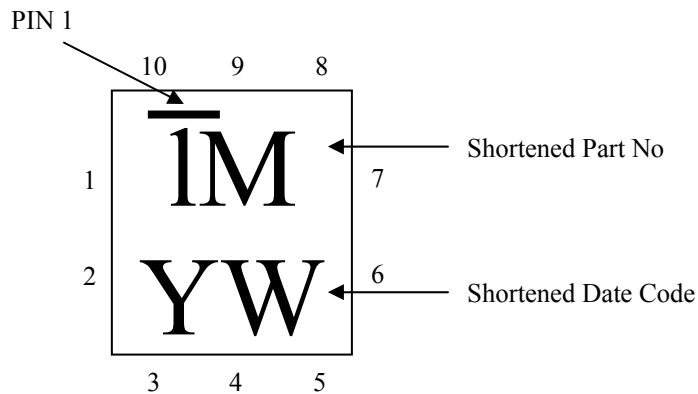


Figure 10. Channel On Capacitance

Mechanical Information 10-pin UQFN (ZM10)



Marking Description



Ordering Information

Part Number	Package Code	Package
PI3A268CZME	ZM	Lead Free and Green UQFN-10 (ZM10)

Notes:

- E = Pb-free and Green
- X Suffix= Tape and reel