Constant Voltage High Power Factor PWM Boost Driver Controller for MR16 Application

General Description

The RT8465 is a constant output voltage, active high power factor, PWM Boost driver controller. It can be used as the first Boost stage followed by a constant current Buck converter with input from AC/electronic transformer in MR16/AR111 application. To achieve high power factor, the AC input voltage from AC/electronic transformer is sensed via the SIN pin. An internal power factor correction circuit follows the sensed sine waveform and modulates the external MOSFET duty cycle-by-cycle to achieve constant output voltage.

The output voltage is adjustable via an output resistive divider. By operating at 220kHz, the filter component size can be small to fit in tight MR16 space. To drive industrial grade MOSFET switches, the RT8465 gate driver can deliver up to 0.8A output current with 9V gate output voltage.

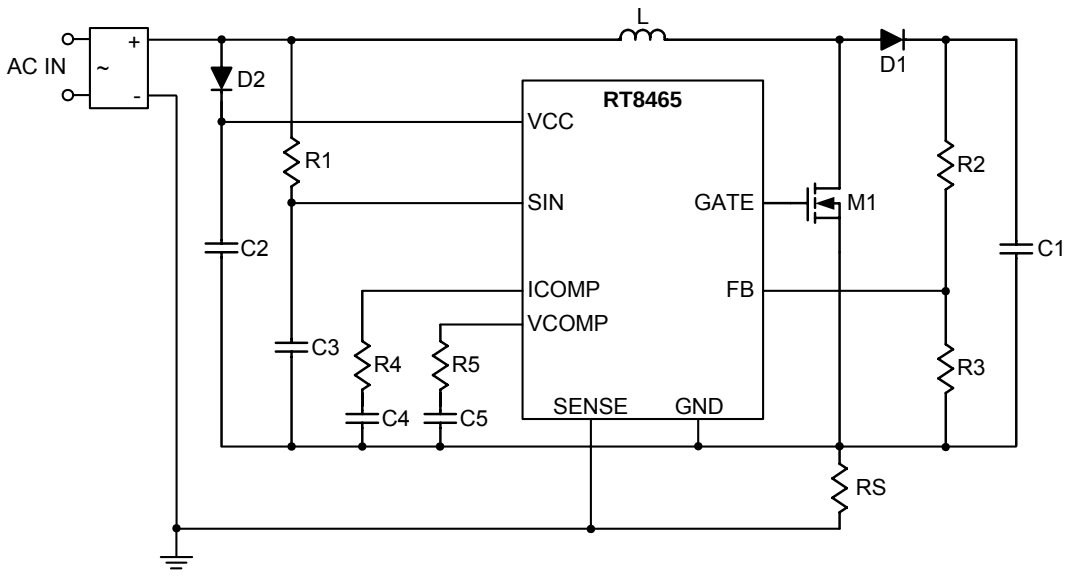
Features

- **Wide Input Voltage Range : 8V to 32V**
- **High Power Factor Correction with Simple System Circuits**
- **Adjustable Constant Output Voltage**
- **Built-in High Power Factor Correction Circuit**
- **Typical 250μA Start-Up Supply Current**
- **Low Quiescent Current : 0.1μA**
- **SOP-8 Package**
- **RoHS Compliant and Halogen Free**

Applications

- MR16, AR111 Lamps
- PFC Controller

Simplified Application Circuit



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Ordering Information

RT8465 □□

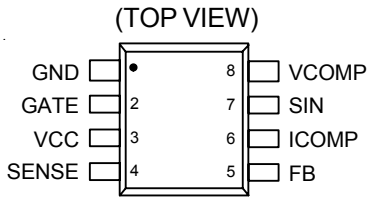
- Package Type
  S : SOP-8
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

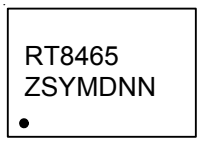
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations



SOP-8

Marking Information



RT8465ZS : Product Number

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground.
2	GATE	Gate Driver for External MOSFET Switch.
3	VCC	Power Supply. For good bypass, place a ceramic capacitor near the VCC pin.
4	SENSE	Inductor Current Sense Input. The inductor current is sensed by a resistor between GND and SENSE pins. The sense pin signal is used as the saw tooth signal to the PWM comparator. The comparator output will modulate the GATE turn-on duty to achieve the output voltage regulation.
5	FB	Output Voltage Sense Input. The Output voltage is sensed through an external resistive divider. The sensed voltage (which is tied to amplifier negative input) is compared to an internal reference threshold at 1.2V (which is tied to amplifier positive input).
6	ICOMP	Output of the Multiplier. To achieve high power factor, the voltage loop amplifier output signal is modulated with the sensed input voltage through the SIN pin by an internal multiplier. A compensation network between ICOMP and GND is needed.
7	SIN	Input Power Voltage Sensing for PFC Function. An external resistor for input voltage sensing is connected to the power input.
8	VCOMP	Output of the Internal Voltage Loop GM Amplifier. A compensation network between VCOMP and GND is needed.

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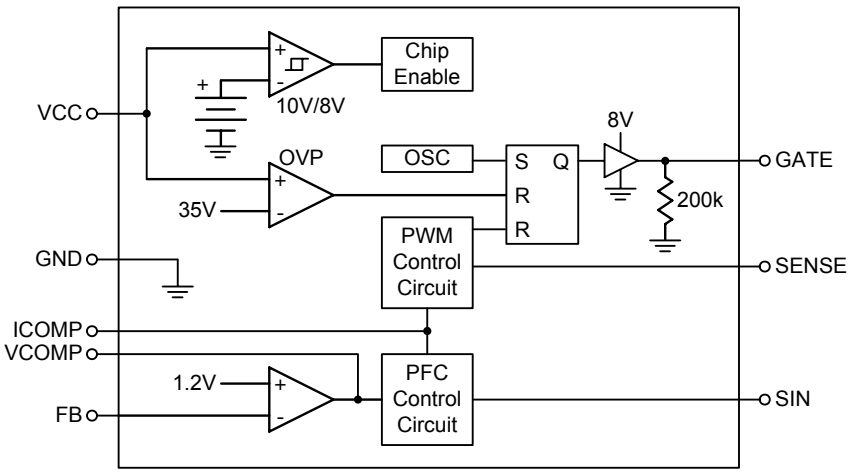
Function Block Diagram



Operation

The RT8465 is a floating-GND Boost PWM current mode controller with an integrated low side floating gate driver. The start up voltage of RT8465 is around 10V. Once VCC is above 10V, the RT8465 will maintain operation until VCC drops below 8V.

The RT8465's main control loop consists of a 220kHz fixed frequency oscillator, an internal 1.2V feedback (FB) voltage sense threshold, and the PFC control circuit with a PWM comparator. In normal operation, the GATE turns high when the gate driver is set by the oscillator (OSC). When the feedback (FB) voltage is below the reference 1.2V threshold, the VCOMP pin voltage will go high. The ICOMP signal is the result of VCOMP signal multiplied with SIN signal. Higher ICOMP voltage means longer GATE turn-on period. The GATE does not always turn off in each cycle. The GATE will be turned on again by OSC for the next switching cycle.

The RT8465 provides several protections, including input voltage Under Voltage Lockout (UVLO), Over Current Protection (OCP) and VCC Over Voltage Protection (OVP). Additionally, to ensure the system reliability, the RT8465 is built with internal thermal protection function.

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Absolute Maximum Ratings (Note 1)

- VCC, SIN to GND ---------- –0.3V to 40V
- GATE to GND (Note 6) ---------- –0.3V to 16V
- VCOMP, ICMOP to GND ---------- –0.3V to 4V
- FB to GND ---------- –0.3V to 2V
- SENSE to GND ---------- –1V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.53W
- Package Thermal Resistance (Note 2)
  SOP-8, θ_{JA} ---------- 188°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC ---------- 8V to 32V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 24V_{DC}, C_{LOAD} = 1nF, R_{LOAD} = 2.2Ω in series, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Start-Up Voltage	V_{ST}		--	10	11	V
Under Voltage Lockout Threshold	V_{UVLO}		7	8	--	V
Under Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	2	--	V
Input Supply Current	I_{CC}	After Start-Up, V_{CC} = 24V	--	2	5	mA
Input Quiescent Current	I_{QC}	Before Start-Up, V_{CC} = 7V	--	0.1	--	μA
Oscillator						
Switching Frequency	f_{SW}	V_{SIN} = 14V	190	220	250	kHz
Maximum Duty in Transient Operation	$D_{MAX(TR)}$	VC = 3V	--	--	100	%
Maximum Duty in Steady State Operation	D_{MAX}		--	97	--	%
Blanking Time	t_{BLANK}		200	--	--	ns
Minimum Turn-Off Time		(Note 5)	--	650	--	ns
Current Sense Amplifier						
Current Sense Voltage	V_{SENSE}	V_{COMP} = 1V, S_{IN} = 15V	--	–100	--	mV
Sense Input Current	I_{SENSE}	Sense = 100mV (Note 5)	--	10	--	μA

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Gate Driver Output							
GATE Pin Maximum Voltage		V_{GATE}	No Load at GATE Pin	--	9.5	16	V
GATE Voltage	High	V_{GATE_H}	I_{GATE} = –20mA	--	9.1	--	V
			I_{GATE} = –100μA	--	9.4	--	
	Low	V_{GATE_L}	I_{GATE} = 20mA	--	0.75	--	V
			I_{GATE} = 100μA	--	0.5	--	
GATE Drive Rise and Fall Time			1nF Load at GATE	--	70	100	ns
GATE Drive Source and Sink Peak Current			1nF Load at GATE (Note 4)	--	0.5	0.8	A
Multiplier							
SIN Pin Input Current			V_{SIN} = 14V	50	60	70	μA
			V_{SIN} = 28V	80	100	120	
ICOMP Threshold for PWM Switch Off		V_{ICOMP}		--	1.2	--	V
VC Output Current		I_{VCOMP}	0.5V ≤ VC ≤ 2.4V (Note 5)	--	16	--	μA
Feedback Voltage		V_{FB}		1.1	1.2	1.3	V
Feedback Input Current		I_{FB}	V_{FB} = 1.2V (Note 5)	--	1	--	μA
OVP and Soft-Start							
Over Voltage Protection		V_{OVP}	VCC Pin	32	35	38	V
Thermal Protection							
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
SIN Pin Input Resistance				--	200	--	kΩ

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design; not subject to production test.

Note 6. The GATE voltage is internally clamped and varies with operating conditions.

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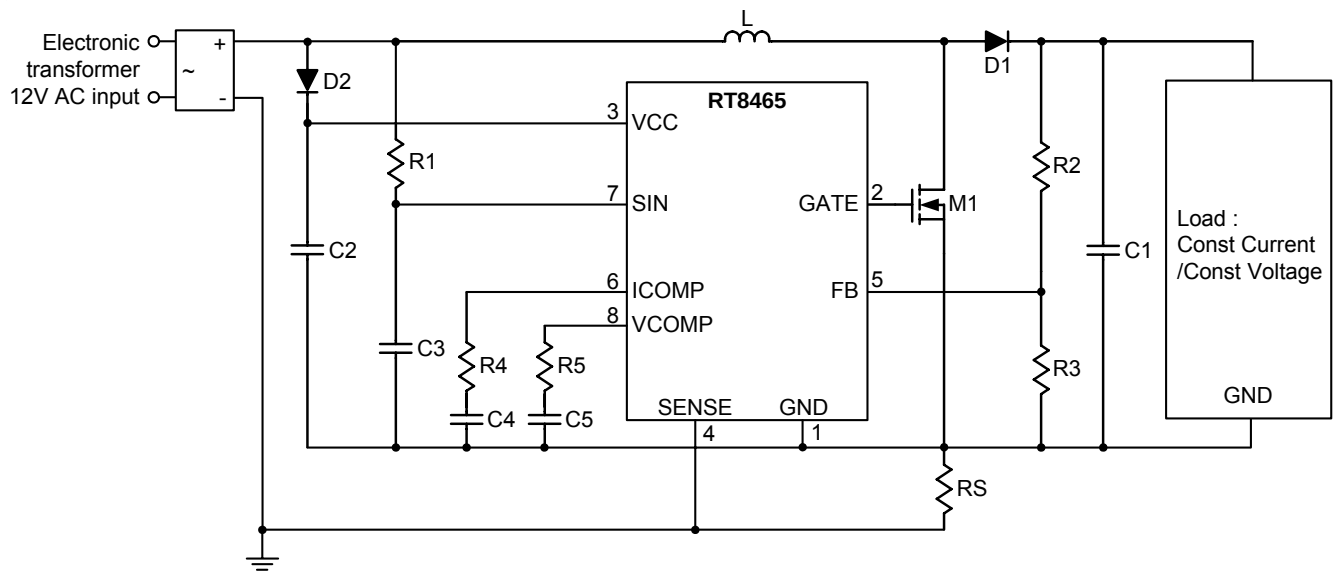
Typical Application Circuit



CC converters : RT8450/RT8471/RT8463

CC drivers : RT8482/RT8458D

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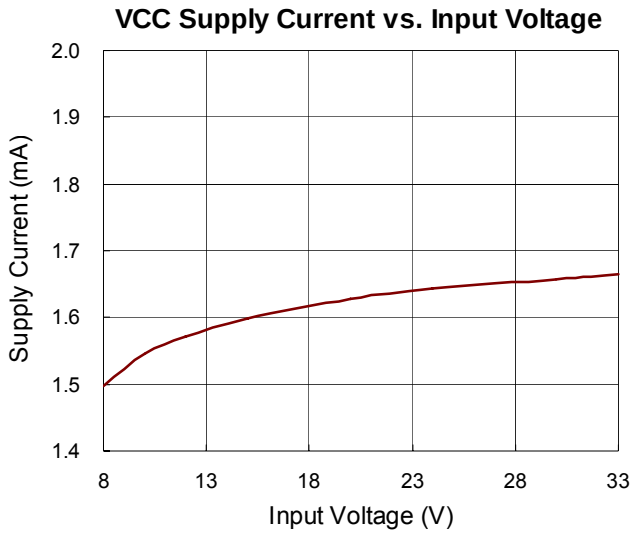
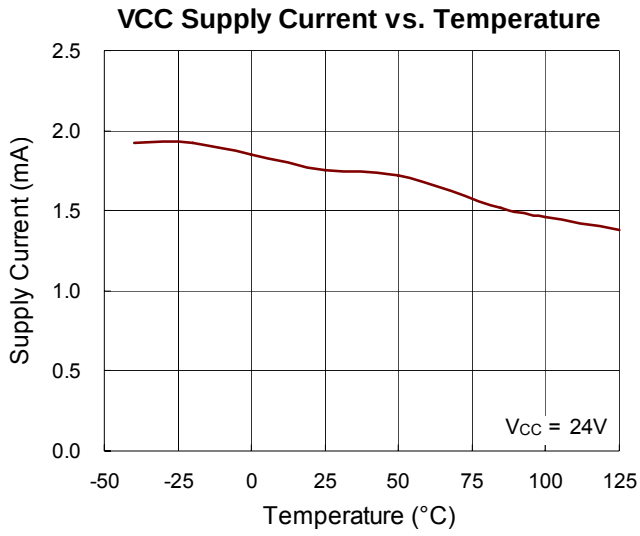
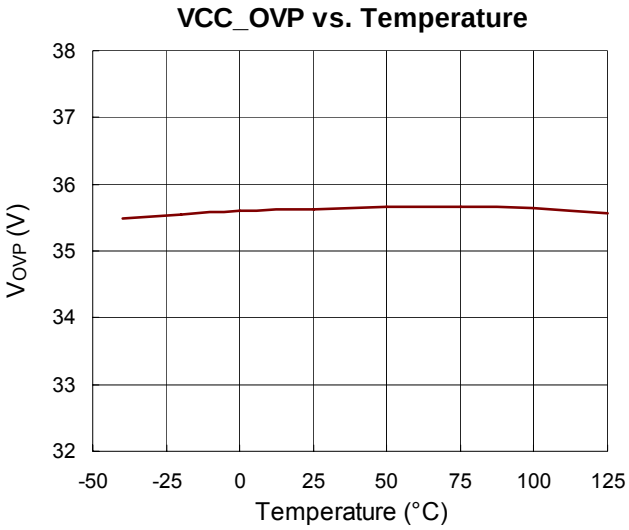
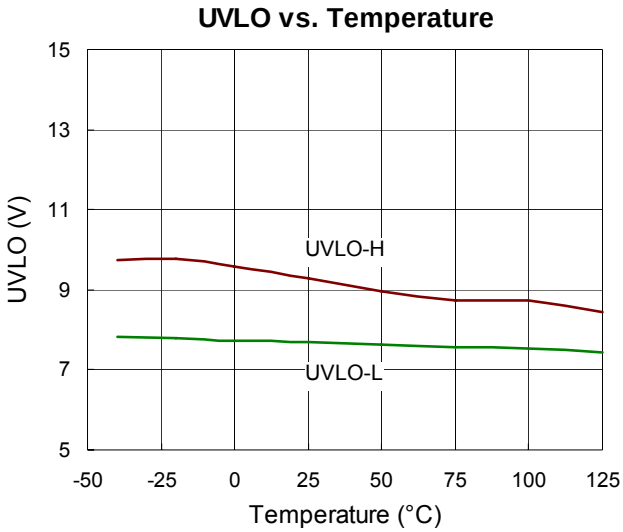
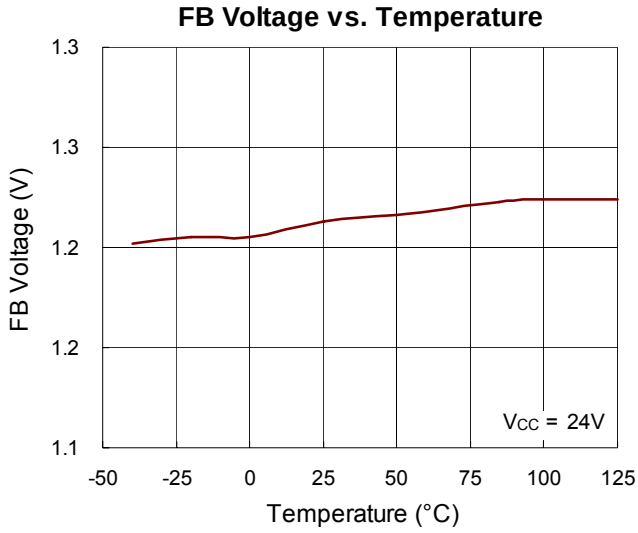
Typical Operating Characteristics

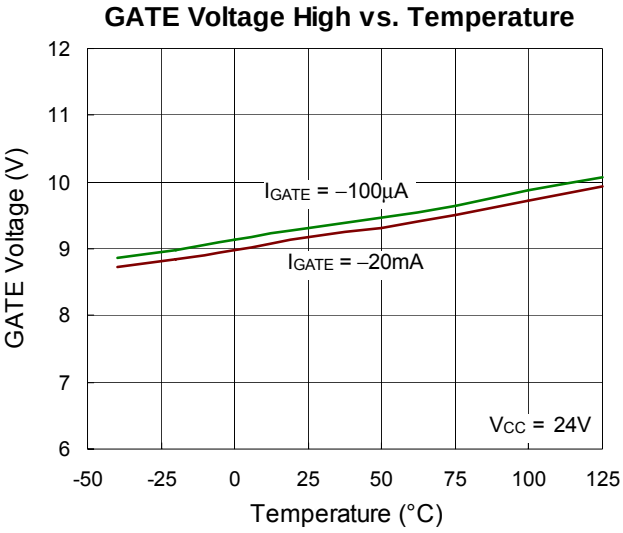












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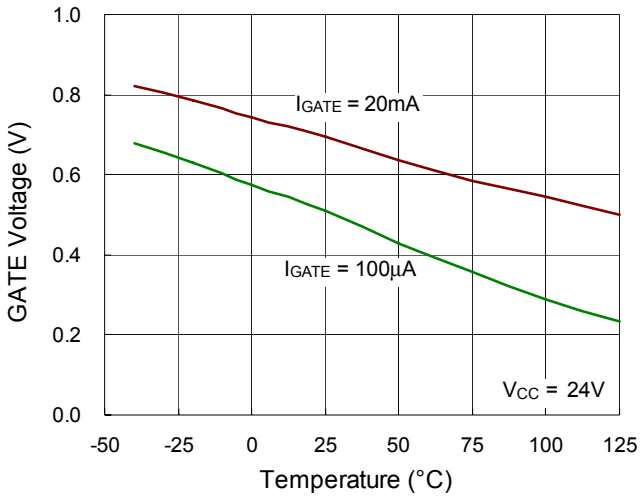
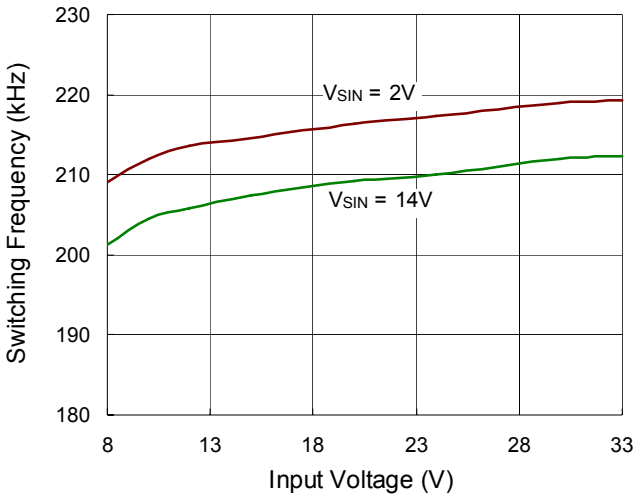
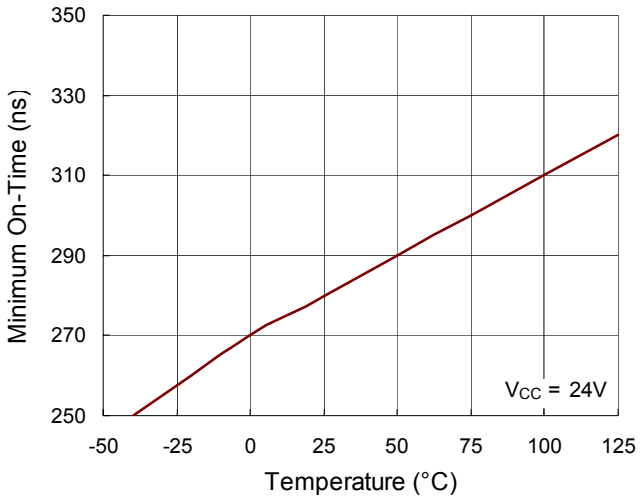
GATE Voltage Low vs. Temperature



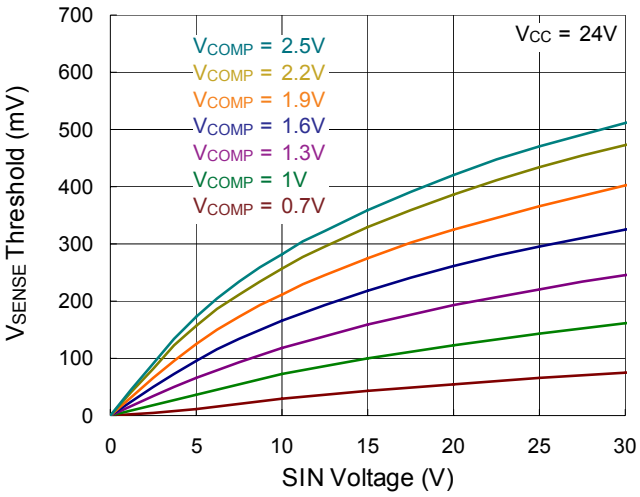
Switching Frequency vs. Input Voltage



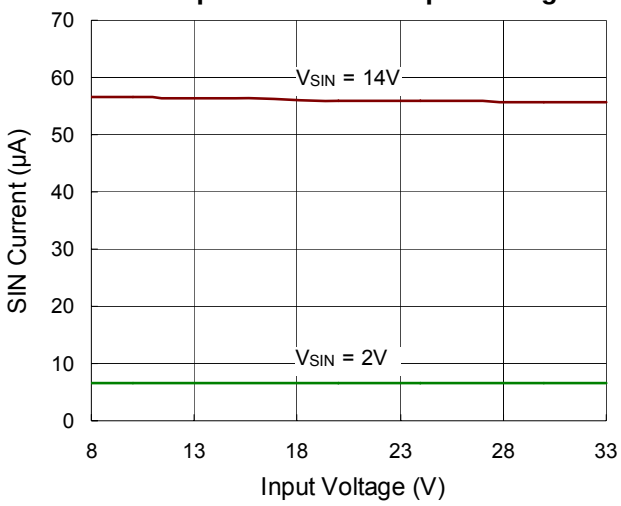
Minimum On-Time vs. Temperature



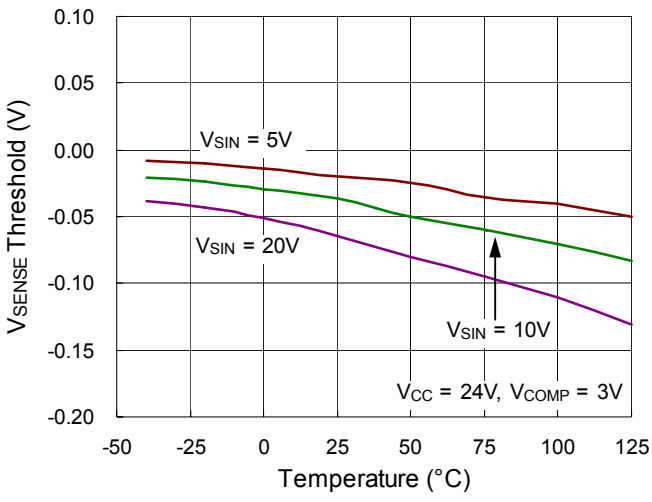
SIN Voltage vs. V_{SENSE} Threshold



SIN Input Current vs. Input Voltage



V_{SENSE} Threshold vs. Temperature



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Application Information

The RT8465 provides active power factor correction for power systems with fewer external components.

The RT8465 can operate in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) by fixed frequency PWM control. The fixed switching frequency is internally set at 220kHz.

The IC operates with a dual control topology; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter DCM. In DCM, the average current waveform will be distorted but the resultant harmonics are still low enough to meet the standard of IEC61000-3-2.

The RT8465 employs average current control to achieve a better input current waveform.

In Figure 1, the inductor current is sensed and filtered by a current error amplifier of which output drives a PWM modulator. In this way, the inner current loop tends to minimize the error between the average input current I_{IN} and its reference. The converter works in CCM, so the same considerations done with regard to the peak current control can be applied.

Multiplier

The multiplier has two inputs. The SIN pin is the divided sinusoidal voltage which makes the current sense comparator threshold voltage vary from zero to peak value. The other input is the output of error amplifier at VCOMP pin. In this way, the input average current wave will be sinusoidal as well as reflects the load status. In order to achieve high power factor and good THD achieved, the multiplier transfer character is designed to be linear over a wide dynamic range, namely, 1V to 20V for SIN and 0.8V to 1.2V for FB. The relationship between the multiplier output and inputs is described as the below equation :

$$V_{ICOMP} = k \times (V_{COMP} - 0.7) \times V_{SIN}$$

where V_{ICOMP} is the reference for the current sense, k is the multiplier gain, VCOMP is the error amplifier output voltage and V_{SIN} is the sinusoidal reference voltage on pin 7.

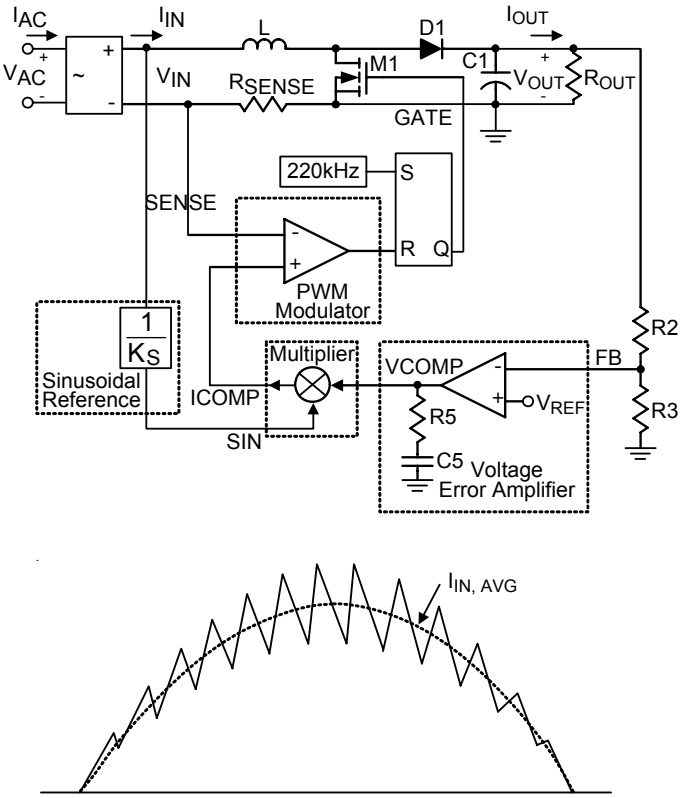

Figure 1. Functional Block with PFC CCM Control

Pulse Width Modulator

The IC employs an average current control scheme in CCM to achieve the power factor correction. If the voltage loop is working and output voltage is kept constant, the duty cycle, D_{OFF}, for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to VIN. The objective of the current loop is to regulate the average inductor current such that it is proportional to the duty cycle, D_{OFF}, and the input voltage, V_{IN}. Figure 2 shows the waveform for the control scheme.

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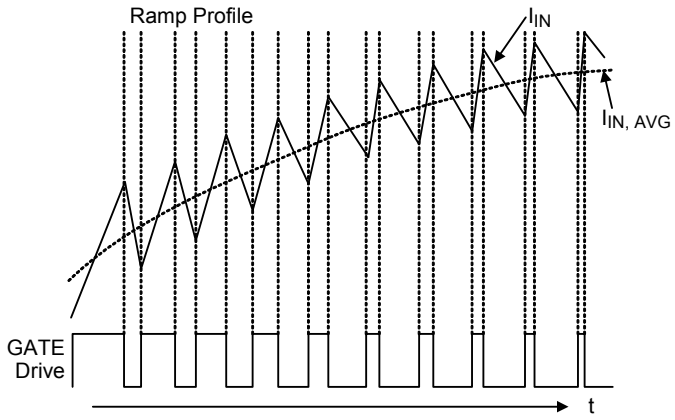

Figure 2. Average Current Controls in CCM

The PWM is performed by the intersection of a ramp signal with the current error amplifier output. The PWM cycle starts with the GATE turn on for a minimum duration about 300ns typical. In case of the inductor current reaches the peak current limitation, the GATE will be turned off immediately when V_{SENSE} is triggered.

Error Amplifier

The outer voltage loop of the cascaded control scheme regulates the PFC output bus voltage V_{OUT}. The internal reference on the non-inverting input of the error amplifier is 1.2V. The error amplifier's inverting feedback FB is connected to an external resistor divider which senses the output voltage.

The output of the error amplifier is one of the two inputs of the multiplier. A compensation loop is connected outside between the error amplifier output at the VCOMP pin, and ground of the GND pin. Normally, the compensation loop bandwidth is very low to realize high power factor for PFC converter. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

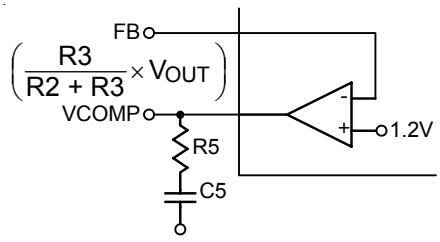

Figure 3. Voltage Loop Amplifier

Current Sense/Current Sense Comparator

The PFC switch's turn-on current is sensed through an external resistor in series with the switch. When the sensed voltage exceeds the threshold voltage (the multiplier output), the current sense comparator will become low and the external MOSFET will be turned off. This ensures a cycle-by-cycle current mode control operation. The maximum current sense reference is 1.8V. The max value usually occurs in start-up process or abnormal conditions such as short load.

Under Voltage Lockout (UVLO)

The RT8465 internal UVLO block monitors the VCC power supply with 2V hysteresis. The hysteresis behavior guarantees a one-short startup resistor and hold-up capacitor. The IC will then be consuming typically 150μA when start-up and the power dissipation on resistor would be less than 0.1W. After start-up, the operating current is typically 1.5mA to get a better efficiency.

Over Voltage Protection (OVP)

Whenever V_{OUT} exceeds the rated value by 5%, the over voltage protection is activated. This is implemented by sensing the voltage at FB pin with respect to a reference voltage of 1.2V. This results in a lower input power to reduce the output voltage V_{OUT}.

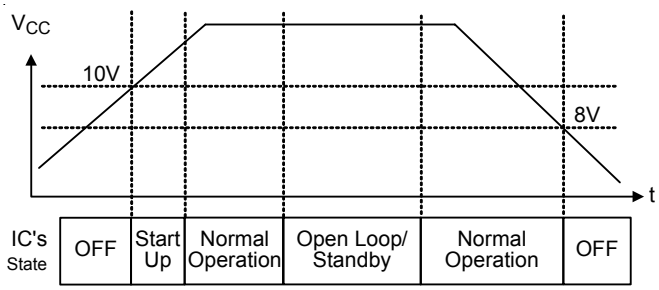

Figure 4. State of Power V_{CC} Operation

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Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 188°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (188°C/W) = 0.53W for SOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

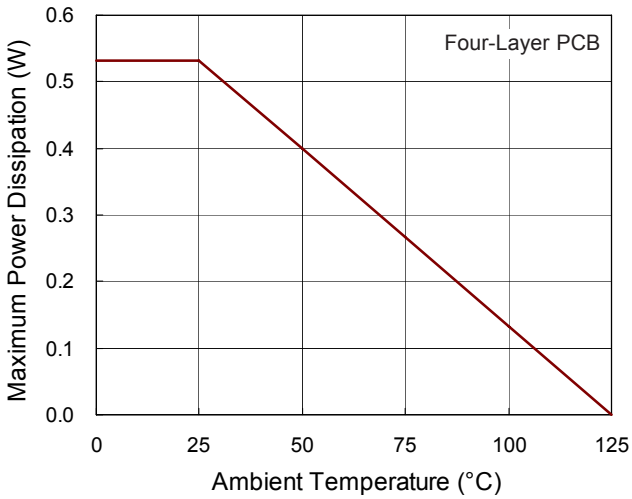

Figure 5. Derating Curve of Maximum Power Dissipation

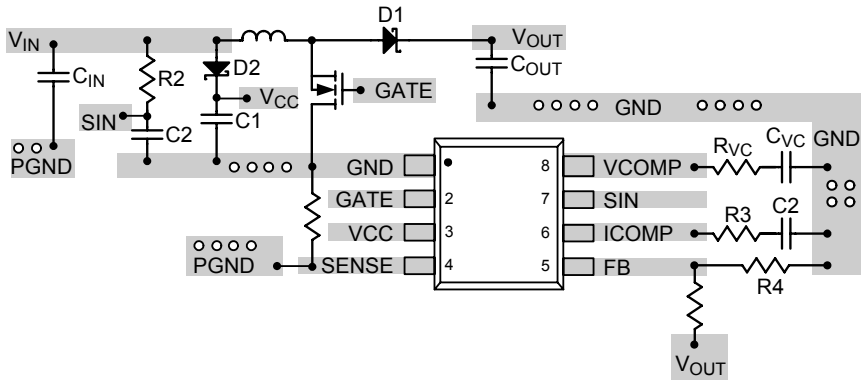

Figure 6. PCB Layout Guide

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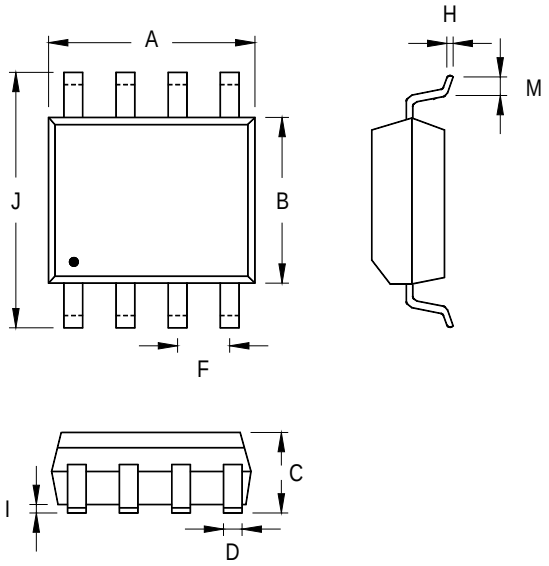
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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