



# STL65DN3LLH5

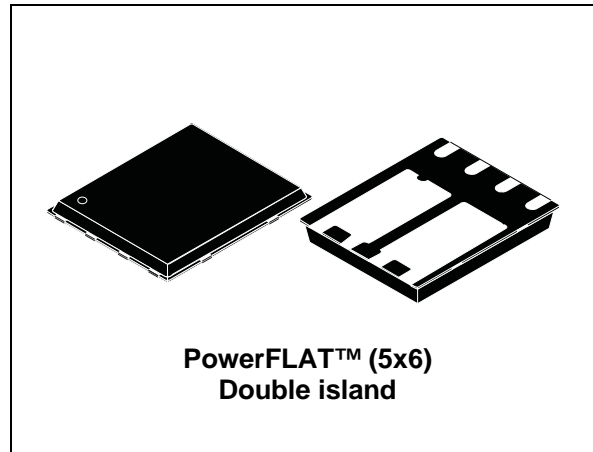
Dual N-channel 30 V, 0.0059  $\Omega$ , 19 A  
PowerFLAT™(5x6) double island, STripFET™ V Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STL65DN3LLH5	30 V	<0.0065 $\Omega$	19 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



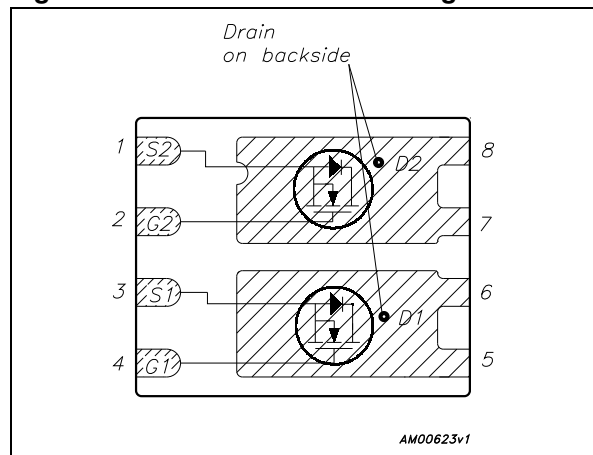
## Application

Switching applications

## Description

This product utilizes the 5<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology. The lowest available R<sub>DS(on)</sub>\*Q<sub>g</sub>, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL65DN3LLH5	65DN3LLH5	PowerFLAT™(5x6) Double island	Tape and reel

# Contents

- 1      Electrical ratings ..... 3**
- 2      Electrical characteristics ..... 4**
  - 2.1    Electrical characteristics (curves) ..... 6
- 3      Test circuits ..... 8**
- 4      Package mechanical data ..... 9**
- 5      Revision history ..... 11**

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	65	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	41	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	19	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	11.8	A
$I_{DM}^{(3)}$	Drain current (pulsed)	76	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. The value is rated according  $R_{thj-c}$
2. The value is rated according  $R_{thj-pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) (steady state)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	32	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current, (pulse width limited by $T_J$ max)	18.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24$ V)	270	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.5		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 9.5 A$ $V_{GS} = 4.5 V, I_D = 9.5 A$		0.0059 0.0071	0.0065 0.0079	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	1500	-	pF
$C_{oss}$	Output capacitance			230		
$C_{rss}$	Reverse transfer capacitance			23		
$Q_g$	Total gate charge	$V_{DD} = 15 V, I_D = 19 A$	-	12	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5 V$		5		
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 14</a> )		4.4		
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain, Bias=0 test signal level = 20 mV, open drain	-	1.6	-	$\Omega$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=9.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 13</a> )		8.8		ns	
$t_r$	Rise time		-	18	-	ns	
$t_{d(off)}$	Turn-off delay time				26		ns
$t_f$	Fall time				4		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		19	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		76	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 19\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=25\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$		24		ns
$Q_{rr}$	Reverse recovery charge		-	12		nC
$I_{RRM}$	Reverse recovery current				1.8	

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

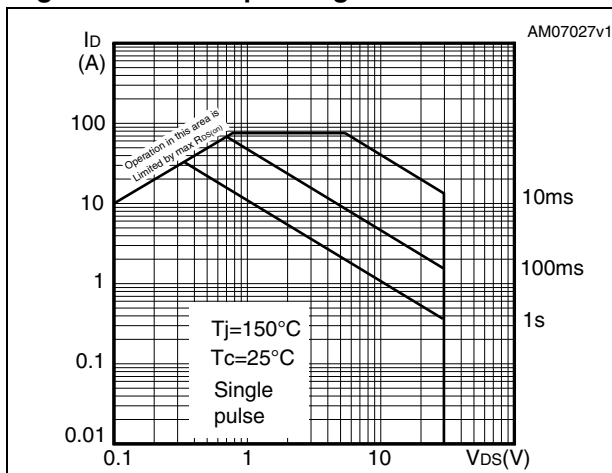


Figure 3. Thermal impedance

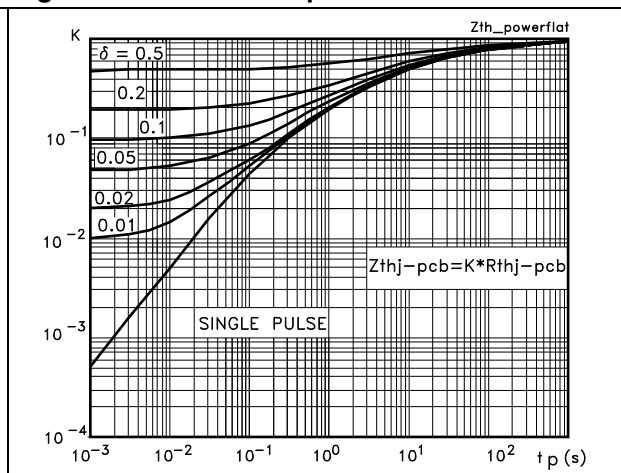


Figure 4. Output characteristics

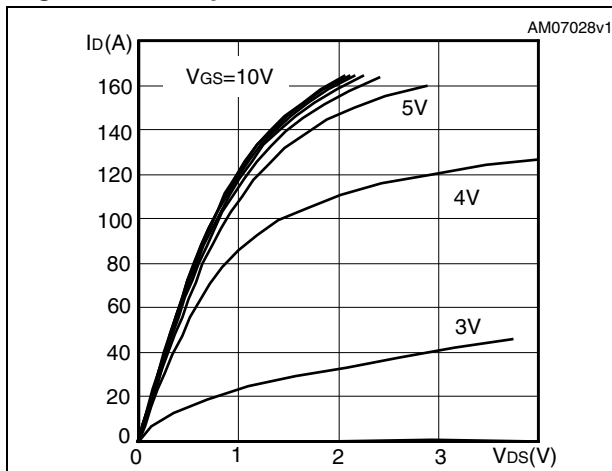


Figure 5. Transfer characteristics

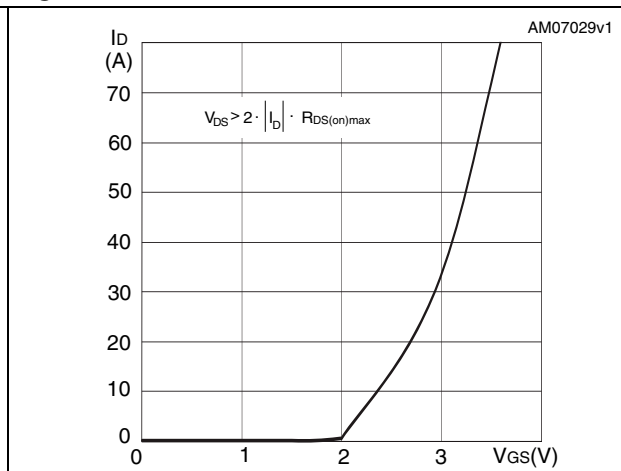


Figure 6. Normalized  $B_{V_{DS}}$  vs temperature

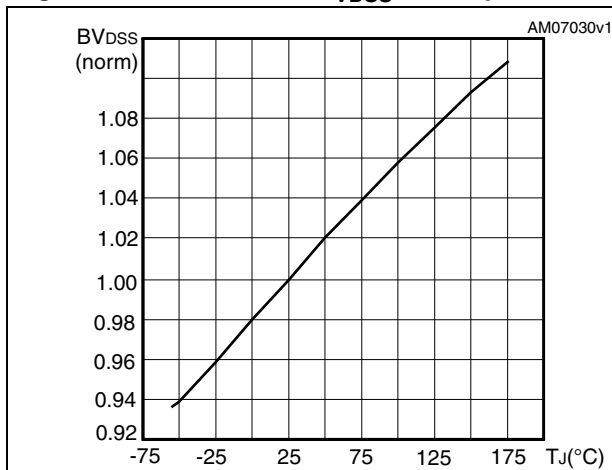


Figure 7. Static drain-source on resistance

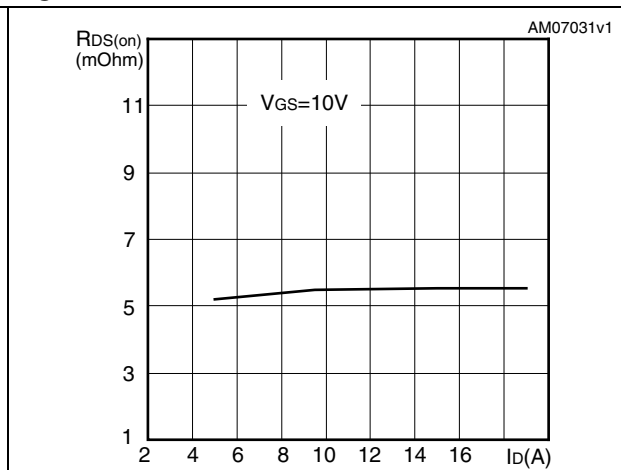


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

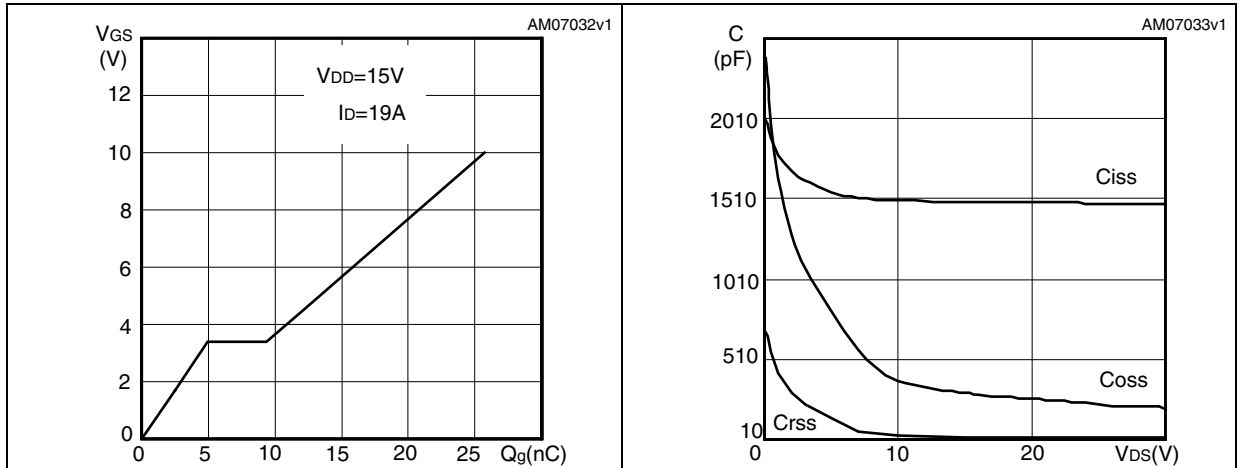


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

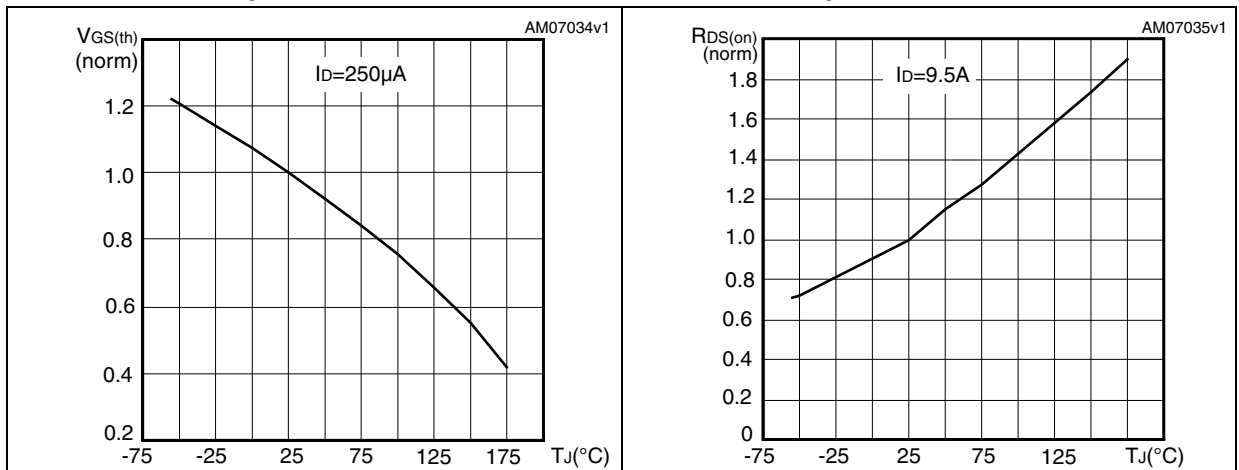
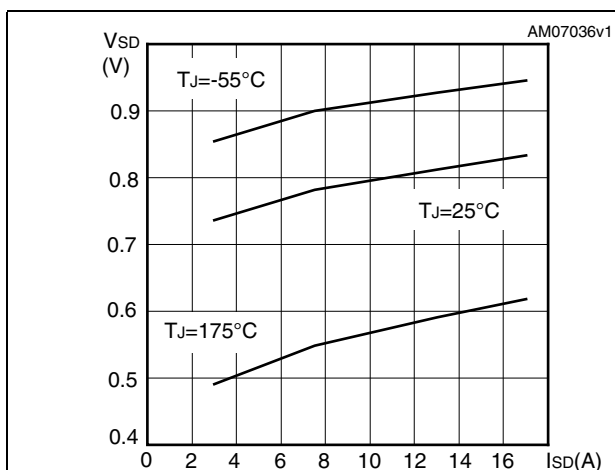


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



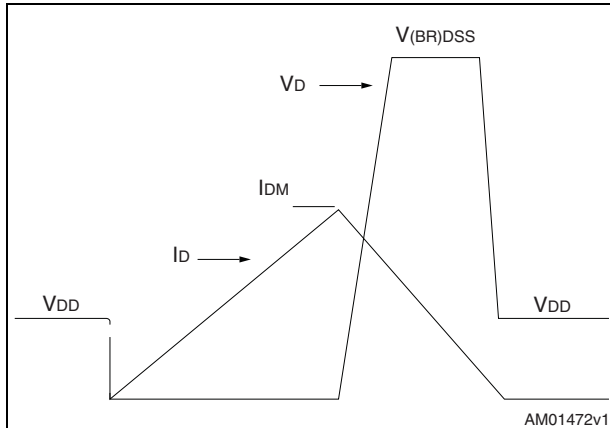
**Figure 15. Test circuit for inductive load switching and diode recovery times**



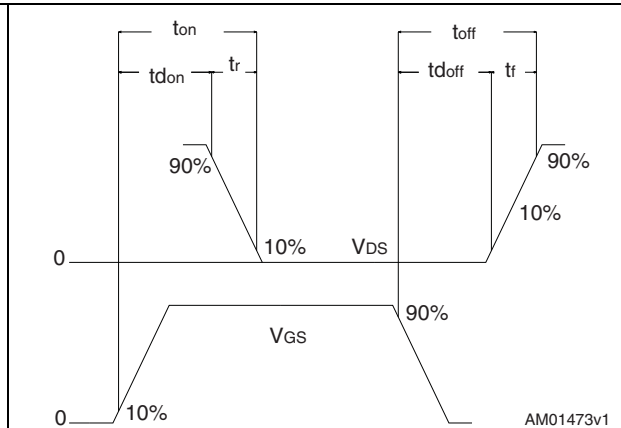
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





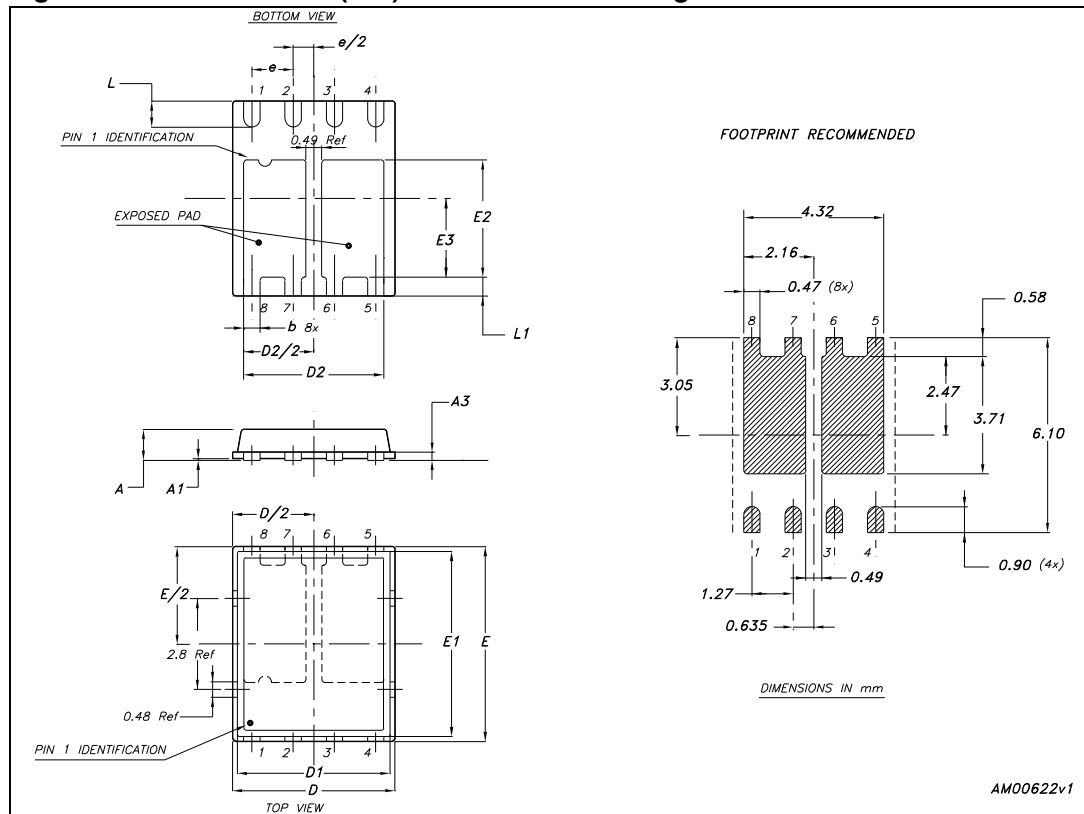
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. PowerFLAT™ (5x6) double island mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.90
A1		0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.11	4.21	4.31
E		6.00	
E1		5.75	
E2	3.51	3.61	3.71
E3	2.32	2.42	2.52
e		1.27	
L	0.70	0.80	0.90
L1	0.48	0.58	0.68

Figure 19. PowerFLAT™ (5x6) double island drawing



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Dec-2010	1	First release

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)