TC514410AP/AJ/ASJ/AZ–70, TC514410AP/AJ/ASJ/AZ–80
TC514410AP/AJ/ASJ/AZ–10

1,048,576 WORD × 4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514410AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514410AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514410AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300 / 350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

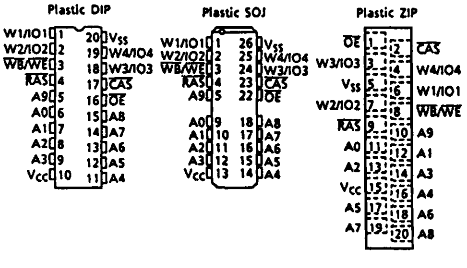
	TC514410AP/AJ/ASJ/ AZ - 70/	- 80/	- 10
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC} Cycle Time	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514410AP/AJ/ASJ/AZ–70)
  - 468mW MAX. Operating (TC514410AP/AJ/ASJ/AZ–80)
  - 413mW MAX. Operating (TC514410AP/AJ/ASJ/AZ–10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write per Bit, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  - TC514410AP : DIP20-P-300C
  - TC514410AJ : SOJ26-P-350
  - TC514410ASJ : SOJ26-P-300A
  - TC514410AZ : ZIP2-P-400A

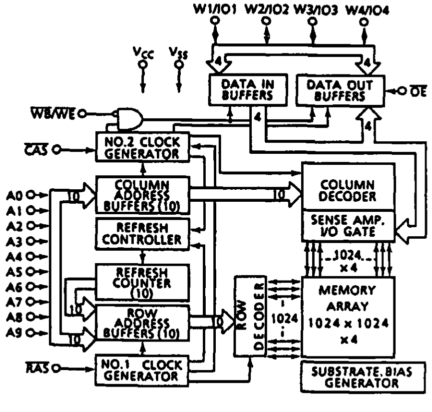
PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~W4/IO4	Write Select/Date Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514410AP/AJ/ASJ/AZ-70	-	100	mA	3, 4 5
		TC514410AP/AJ/ASJ/AZ-80	-	85		
		TC514410AP/AJ/ASJ/AZ-10	-	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	TC514410AP/AJ/ASJ/AZ-70	-	100	mA	3, 5
		TC514410AP/AJ/ASJ/AZ-80	-	85		
		TC514410AP/AJ/ASJ/AZ-10	-	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC}=t_{PC}$ MIN.)	TC514410AP/AJ/ASJ/AZ-70	-	70	mA	3, 4 5
		TC514410AP/AJ/ASJ/AZ-80	-	65		
		TC514410AP/AJ/ASJ/AZ-10	-	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514410AP/AJ/ASJ/AZ-70	-	100	mA	3, 5
		TC514410AP/AJ/ASJ/AZ-80	-	85		
		TC514410AP/AJ/ASJ/AZ-10	-	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)		- 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		- 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = - 5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	125	-	ns	
t_{RAC}	Access Time from $\overline{\text{RAS}}$	-	70	-	80	-	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{\text{CAS}}$	-	20	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	9,15
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	-	40	-	45	-	55	ns	9
t_{CLZ}	$\overline{\text{CAS}}$ to output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_{T}	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	20	-	20	-	25	-	ns	
t_{RHCP}	$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Fast Page Mode)	40	-	45	-	55	-	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	10	-	ns	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{\text{RAS}}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{\text{CAS}}$ Precharge to $\overline{\text{WRITE}}$ Delay Time	75	–	75	–	90	–	ns	13
t_{CSR}	$\overline{\text{CAS}}$ Set-Up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{\text{OE}}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{\text{OE}}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{\text{OE}}$	0	20	0	20	0	20	ns	
t_{OEH}	$\overline{\text{OE}}$ Command Hold Time	20	–	20	–	25	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WTS}	Write Command Set-up Time	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Width	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time	10	-	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	155	-	185	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	-	180	-	215	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	65	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
t_{RAC}	Access Time from $\overline{\text{RAS}}$	-	75	-	85	-	105	ns	9,14, 15
t_{CAC}	Access Time from $\overline{\text{CAS}}$	-	25	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	45	-	55	ns	9,15
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	-	45	-	50	-	60	ns	9
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	75	-	85	-	105	-	ns	
t_{RHCP}	$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	45	-	50	-	60	-	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	40	-	45	-	55	-	ns	
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	55	-	55	-	65	-	ns	13
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	105	-	115	-	140	-	ns	13
t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	70	-	75	-	90	-	ns	13
t_{CPWD}	$\overline{\text{CAS}}$ Precharge to $\overline{\text{WRITE}}$ Delay Time	80	-	80	-	95	-	ns	13
t_{OEA}	$\overline{\text{OE}}$ Access Time	-	25	-	25	-	30	ns	
t_{OEH}	$\overline{\text{OE}}$ Command Hold Time	25	-	25	-	30	-	ns	

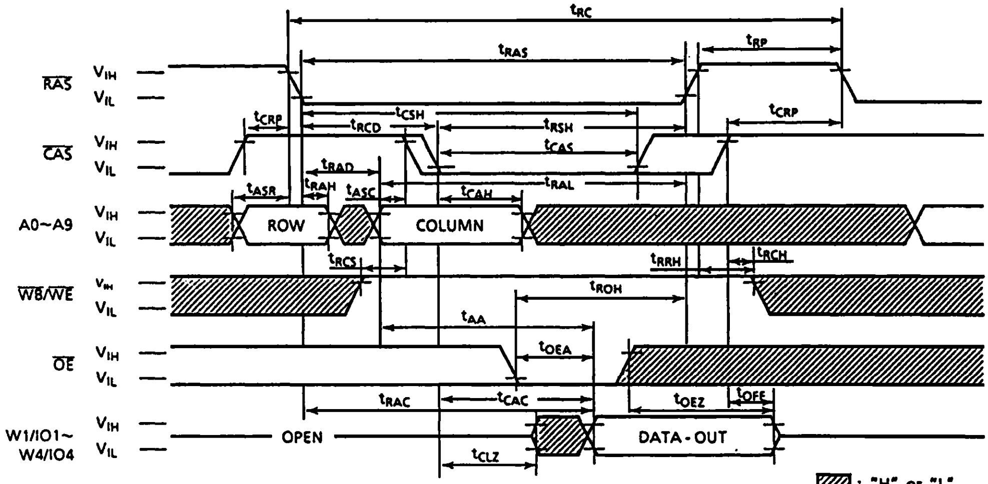
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
C_O	Input/Output Capacitance (I/I01~I/I04)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

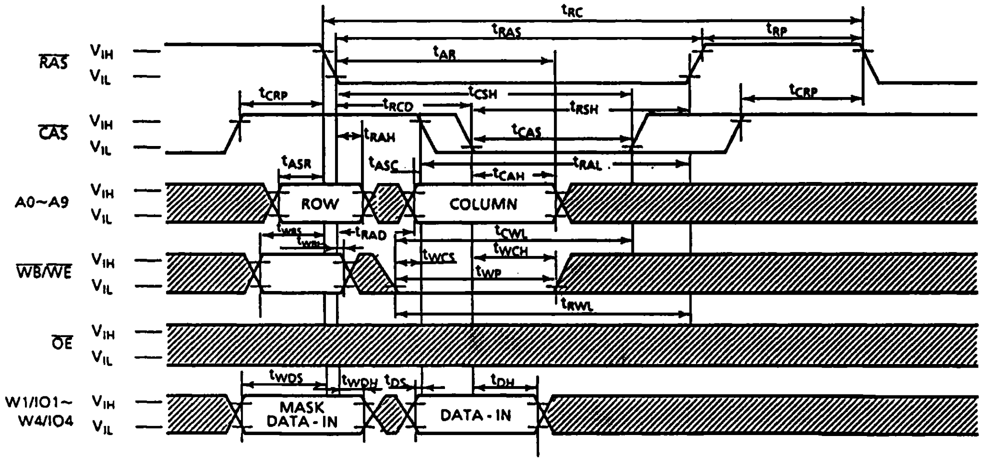
READ CYCLE



▨ : "H" or "L"

Note: DIN="H" or "L"

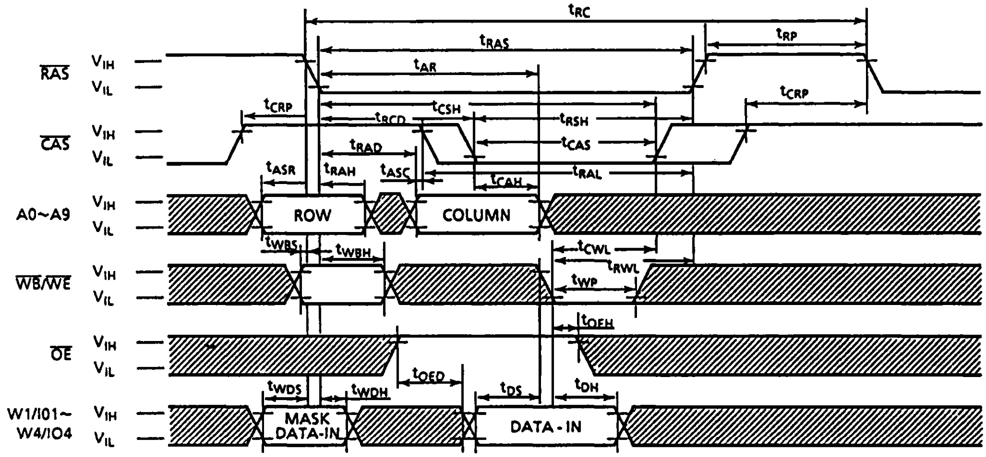
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

Note: DOUT=OPEN

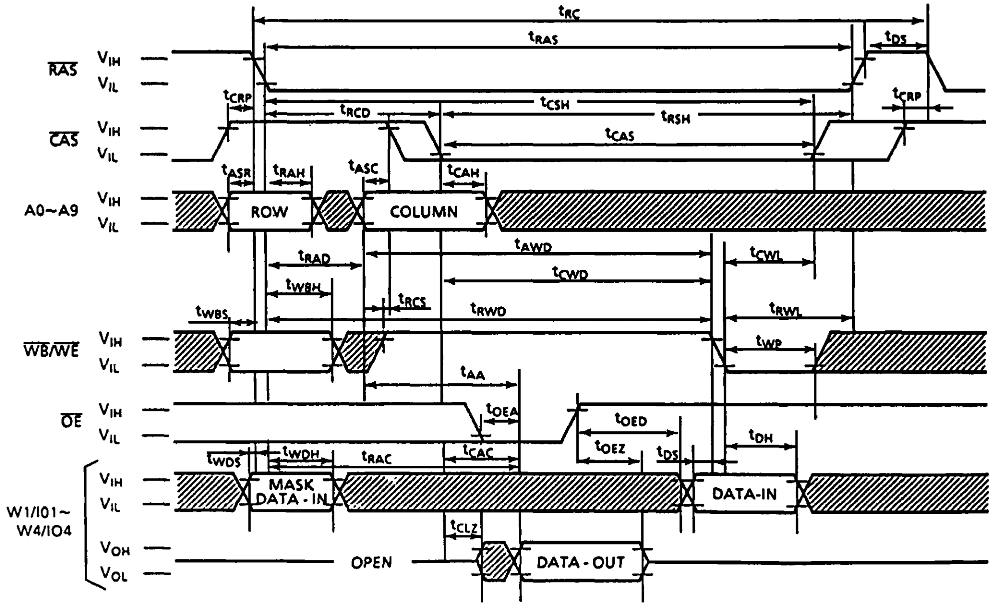
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



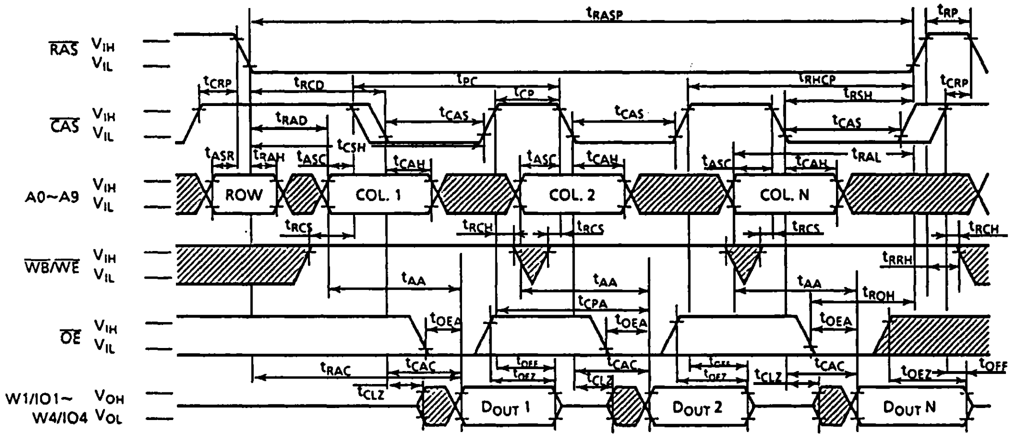
Note: D_{OUT}=OPEN

▨ : "H" or "L"

READ - MODIFY - WRITE CYCLE



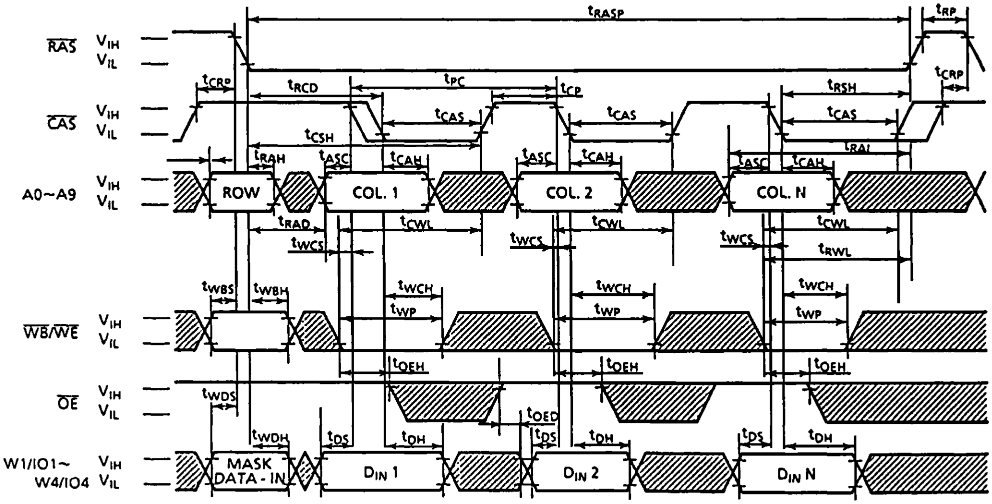
FAST PAGE MODE READ CYCLE



Note: D_{IN}="H"or"L"

▨ : "H" or "L"

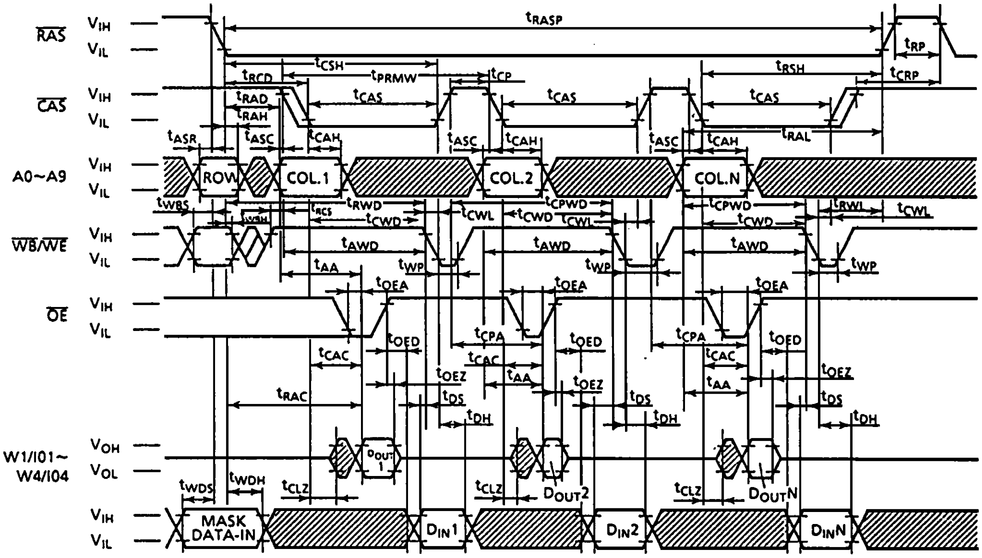
FAST PAGE MODE WRITE CYCLE



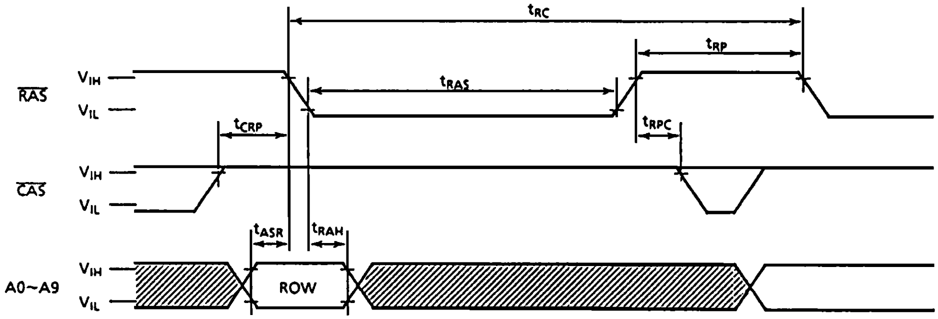
▨ : "H" or "L"

Note: D_{OUT}=OPEN

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



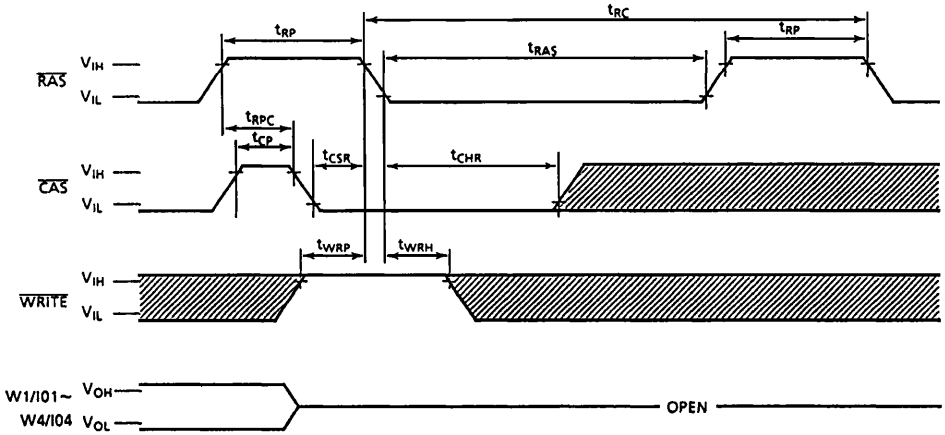
RAS ONLY REFRESH CYCLE



▨ : "H" or "L"

Note: WRITE, OE="H" or "L"

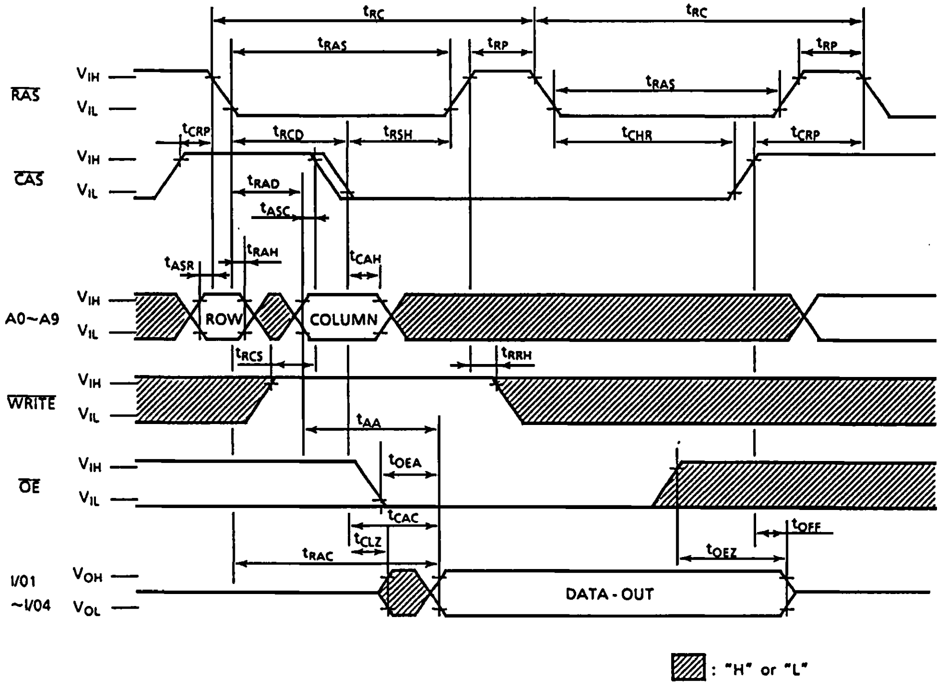
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



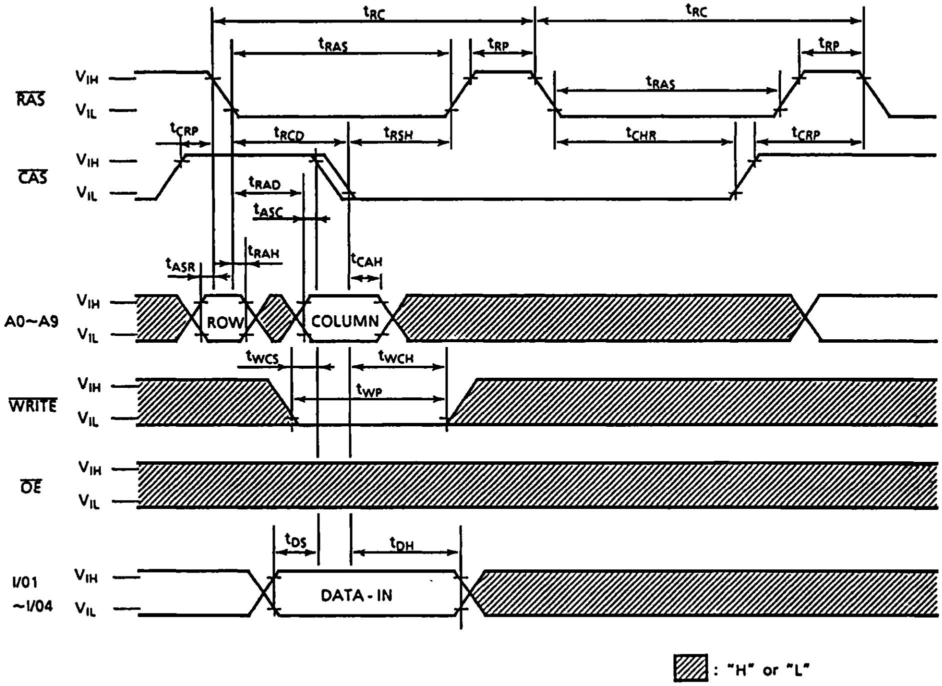
Note : D_{IN}, $\overline{\text{OE}}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

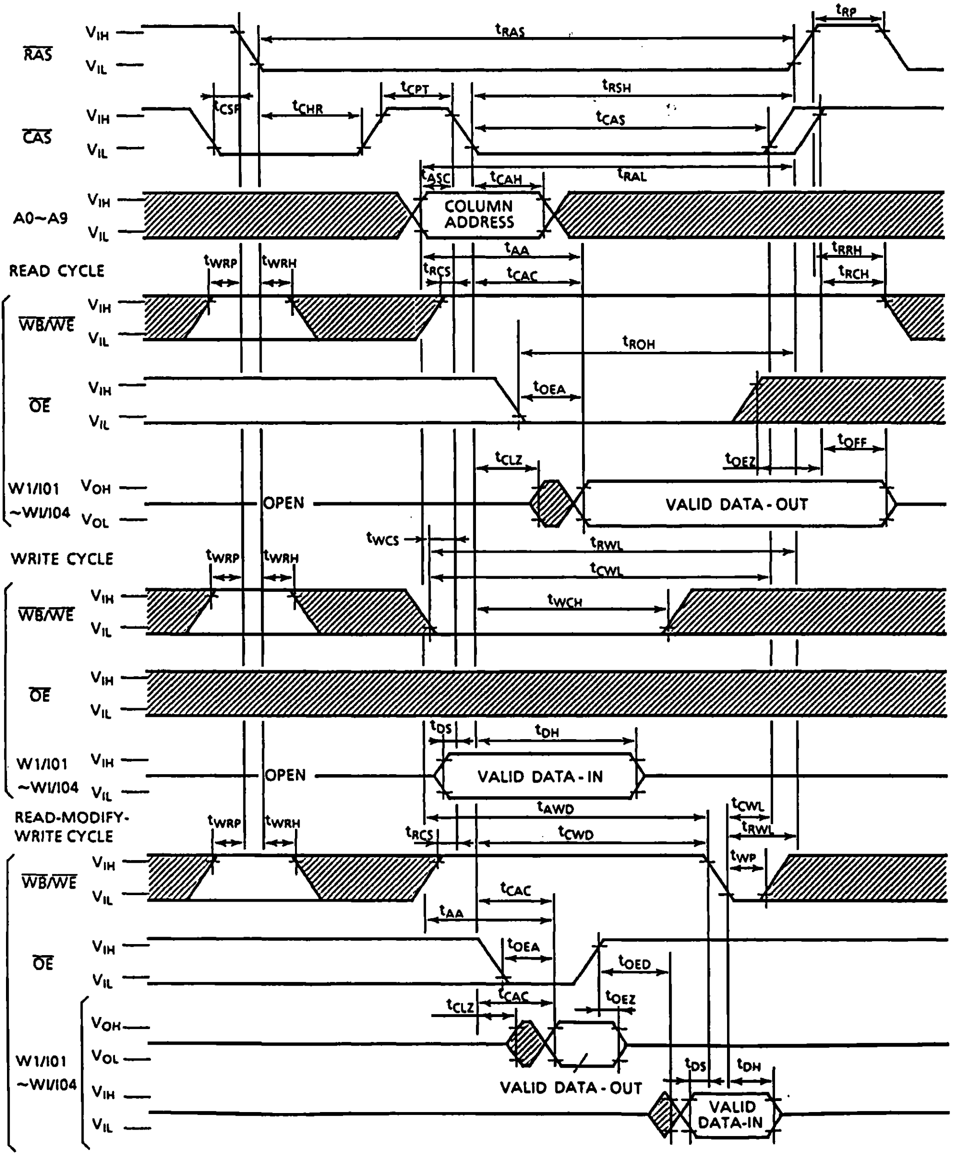
HIDDEN REFRESH CYCLE (READ)



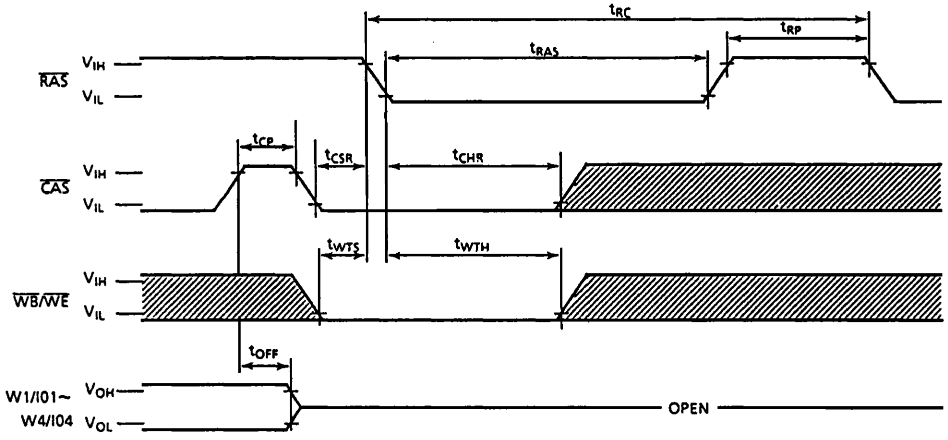
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



$\overline{\text{WE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



Note : D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC51410AP/AJ/ASJ/AZ are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. The "gated $\overline{\text{CAS}}$" feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

A write cycle is performed by bringing ($\overline{\text{WB}}$/) $\overline{\text{WE}}$ low during the $\overline{\text{RAS}}$/$\overline{\text{CAS}}$ operation. The falling edge of $\overline{\text{CAS}}$ or ($\overline{\text{WB}}$/) $\overline{\text{WE}}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{\text{WB}}$(/$\overline{\text{WE}}$) must be low as $\overline{\text{RAS}}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{\text{RAS}}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{\text{RAS}}$ talls the write operation is inhibited on the chip if $\overline{\text{WB}}$(/$\overline{\text{WE}}$) is high as $\overline{\text{RAS}}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valied after the access time has elapsed and remains valied while $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ are low. $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{\text{OE}}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{\text{OE}}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ can control the output. Thus in a read operation, either $\overline{\text{OE}}$ or $\overline{\text{CAS}}$ returning high forces the outputs into the high impedance state.

$\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A9) within each 16 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{\text{RAS}}$-only" cycles.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

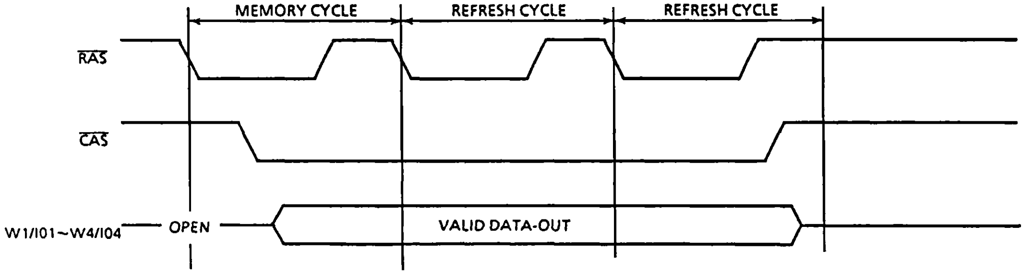
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TC514410AP/AJ/ASJ/AZ offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514410AP/AJ/ASJ/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514410AP/AJ/ASJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514410AP/AJ/ASJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
③ Check "1" out of 512 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.
⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514410AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{00} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514410J/Z. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

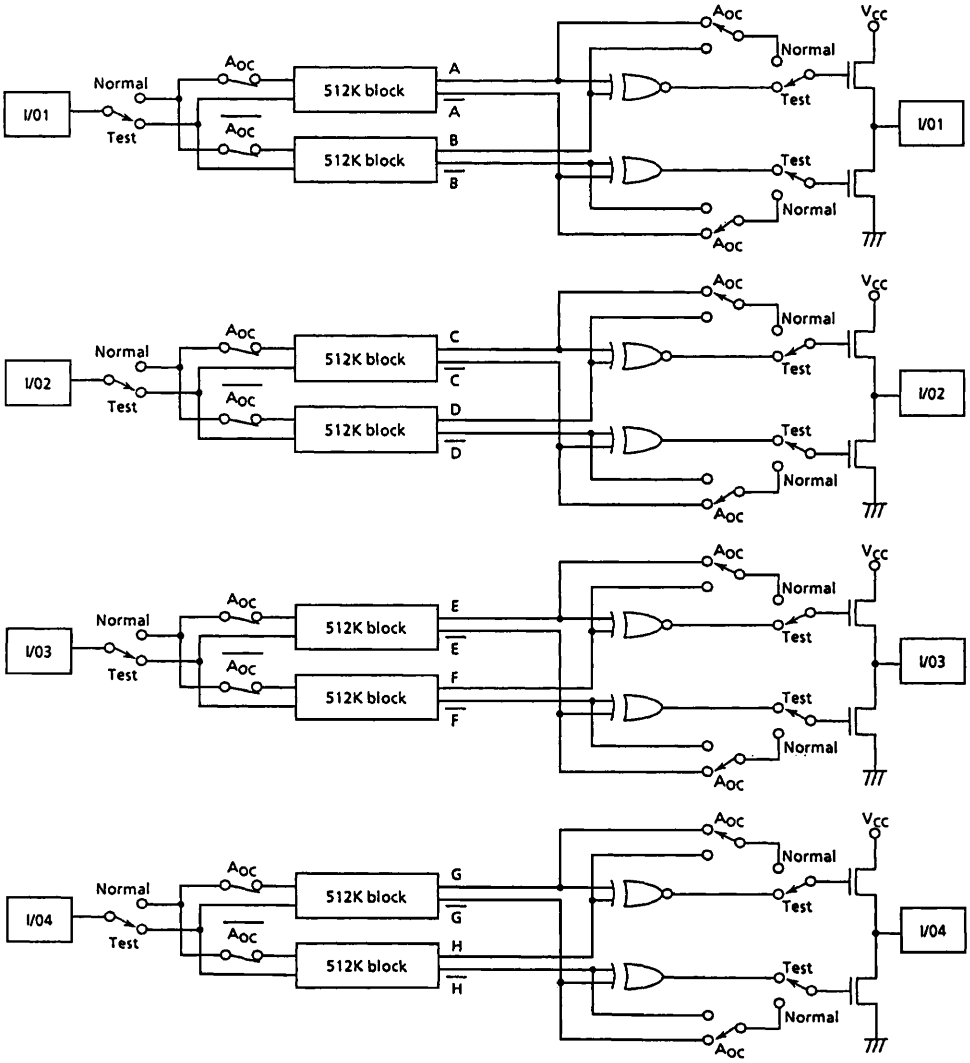


Fig. 1