WINSTAR Display

OLED SPECIFICATION

Model No:

WEG005016ALPP5N00000

OLED Specification

Contents

www.winstar.com.tw

WINSTAR

WINSTAR Display
華凌光電股份有限公司

Technology - Innovation - Value
Eco Friendly - Revolution

SPECIFICATION Version: A

CUSTOMER :
MODULE NO. : **WEG005016ALPP5N00000**

APPROVED BY: (FOR CUSTOMER USE ONLY)	

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2010/11/18		First issue
A	2010.12.20	10	68 series only

1. Module Classification Information

W E G 005016 A L P P 5 N 00000

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

1	Brand：WINSTAR DISPLAY CORPORATION		
2	E：OLED		
3	Display Type：H→Character Type, G→Graphic Type		
4	Number of dots： 50*16 Dots		
5	Serials code		
6	Emitting Color	A：Amber	R：RED
		B：Blue	C：Full color
		G：Green	W：White
		Y：Yellow Green	L：Yellow
7	Polarizer	P：With Polarizer; N: Without Polarizer	
8	Display Mode	P：Passive Matrix ; A: Active Matrix	
9	Driver Voltage	3: 3.0 V; 5: 5.0V	
10	Touch Panel	N：Without touch panel; T: With touch panel	
11	Serial No.	00000: Sales code	

2. General Specification

Item	Dimension	Unit
Number of Characters	50*16 Dots	—
Module dimension	58.0 x 32.0 x 10.0(MAX)	mm
View area	38.0 x 16.0	mm
Active area	29.96 x 11.16	mm
Dot size	0.56 x 0.66	mm
Dot pitch	0.60x 0.70	mm
LCD type	OLED , Yellow	
Duty	1/16	

3. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Notes
Operating Temperature	T_{OP}	-40	+80	℃	
Storage Temperature	T_{ST}	-40	+80	℃	
Input Voltage	V_I	-0.3	VDD	V	
Supply Voltage For Logic	VDD-V_{SS}	-0.3	5.3	V	

4. Electrical Characteristicsical

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD-VSS	—	3.0	5.0	5.3	V
Input High Volt.	VIH	—	0.9 VDD	—	VDD	V
Input Low Volt.	VIL	—	GND	—	0.1VDD	V
Output High Volt.	VOH	IOH=-0.5mA	0.8 VDD	—	VDD	V
Output Low Volt.	VOL	IOL=0.5mA	GND	—	0.2 VDD	V
Supply Current	IDD	VDD=5V	—	16	—	mA
CIEx(Yellow)		x,y(CIE1931)	0.44	0.48	0.52	
CIEy(Yellow)		x,y(CIE1931)	0.46	0.50	0.54	

5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ		160			deg
	(H)φ		160			deg
Contrast Ratio	CR	Dark	2000:1		—	—
Response Time	T rise	—		10		μs
	T fall	—		10		μs
Supply Voltage For Logic 5V 50% CheckBoard Brightness		With polarizer		125		nits
Supply Voltage For Logic 3V 50% CheckBoard Brightness		With polarizer		175		nits

6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	5.0V	Supply Voltage for logic
3	NC	—	
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	NC	—	
16	NC	—	

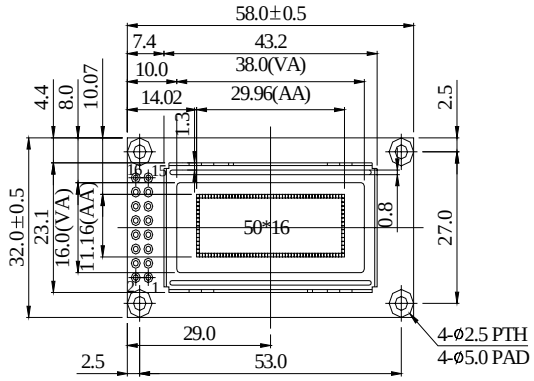
※Brightness Control

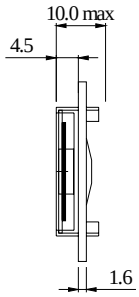
Brightness(nits)	Power consumption(measured with random texts)
125(typical)	80mW(5V*16mA)

Notes: 1.When random texts pattern is running , averagely , at any instance , about 1/2 of pixels will be on.

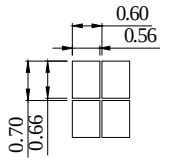
2. You can to use the display off mode to make long life.

7. Counter Drawing & Block Diagram





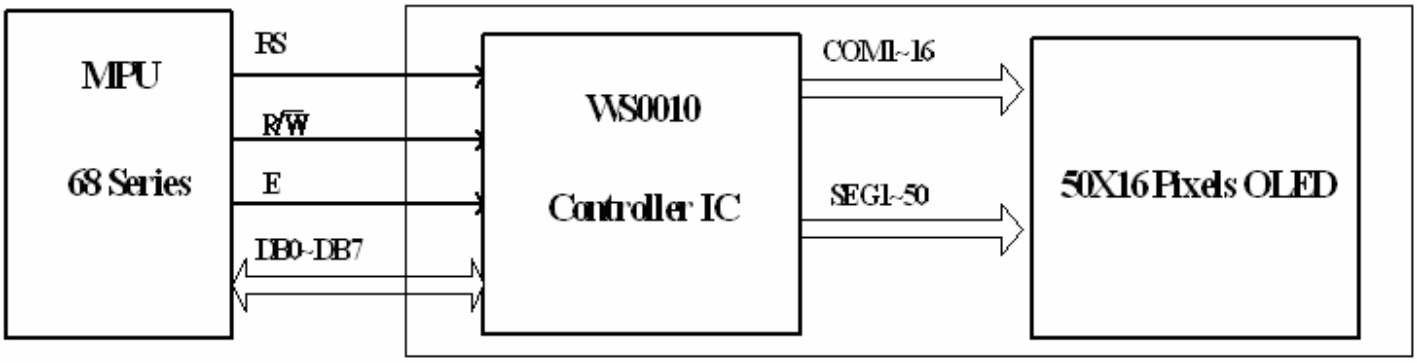
PIN NO.	SYMBOL
1	Vss
2	Vdd
3	NC
4	RS
5	R/$\overline{W}$
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	NC
16	NC



DOT SIZES

SCALE 10/1

The non-specified tolerance of dimension is ±0.3 mm .



Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GXA(Graphic X-axis Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
GYA(Graphic Y-axis Address)	0	1	0	0	0	0	0	CGA0

	1	2	3	4	.....	.....	47	48	49	50
CGA=0	GXA=10000000 GYA=01000000	GXA=10000001 GYA=01000000	GXA=10000010 GYA=01000000	GXA=10000011 GYA=01000000	.....	.....	GXA=10101110 GYA=01000000	GXA=10101111 GYA=01000000	GXA=10110000 GYA=01000000	GXA=10110001 GYA=01000000
CGA=1	GXA=10000000 GYA=01000001	GXA=10000001 GYA=01000001	GXA=10000010 GYA=01000001	GXA=10000011 GYA=01000001	.....	.....	GXA=10101110 GYA=01000001	GXA=10101111 GYA=01000001	GXA=10110000 GYA=01000001	GXA=10110001 GYA=01000001

REGISTERS

IC provides two types of 8-bit registers, namely: Instruction Register (IR) and Data Register (DR). The register is selected using the RS Pin. When the RS pin is set to "0", the Instruction Register Type is selected. When RS pin is set to "1", the Data Register Type is selected. Please refer to the table below.

RS	R/WB	Operation
0	0	Instruction register write as an internal operation.
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation (DDRAM or CGRAM to DR)

INSTRUCTION REGISTER (IR)

The Instruction Register is used to store the instruction code (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address, and the Character Generator RAM (CGRAM) Address. Instruction register can only be written from the MPU.

DATA REGISTER (DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

BUSY FLAG (BF)

The Busy Flag is used to determine whether IC is idle or internally operating. When IC is performing some internal operations, the Busy Flag is set to "1". Under this condition, the no other instruction will not be accepted. When RS Pin is set to "0" and R/WB Pin is set to "1", the Busy Flag will be outputted to the DB7 pin.

When IC is idle or has completed its previous internal operation, the Busy Flag is set to "0". The next instruction can now be processed or executed.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins -- DB0 to DB6.

DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 128 x 8-bits or 128 characters.

The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			**Low Order Bits**			
Address Counter (hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=39 is given below.

DDRAM Address: 39						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
0	1	1	1	0	0	1

1-LINE DISPLAY (N=0)

When the number of characters displayed is less than 128, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position (digit)	**1**	**2**	**3**	**4**	**……**	**126**	**127**	**128**
DDRAM address (hexadecimal)	00	01	02	03	……	7D	7E	7F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	7F	00	01	02	03	04	05	06

2-LINE DISPLAY (N=1*)*

Case 1: The Number of Characters displayed is less than 64 x 2 lines

When the number of characters displayed is less than 64 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 64 x8bits DDRAM space. 1st line is 00 to 3F,second line is 40 to 7F.Please refer the figure below.

Display Position	**1**	**2**	**3**	**4**	**…….**	**61**	**62**	**63**	**64**
DDRAM Address (hexadecimal)	00	01	02	03	…….	3C	3D	3E	3F
	40	41	42	43	…….	7C	7D	7E	7F

To illustrate, for 2-line x 20 characters display, the relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position	**1**	**2**	**3**	**4**	**…….**	18	19	20
DDRAM address (hexadecimal)	00	01	02	03	**…….**	11	12	13
	40	41	42	43	**…….**	51	52	53
Shift left	01	02	03	04	**…….**	12	13	14
	41	42	43	44	**…….**	52	53	54
Shift right	3F	00	01	02	**…….**	10	11	12
	7F	40	41	42	**…….**	50	51	52

Case 2: 40-Character x 2 Lines Display
IC(Master) can be extended to display 40 characters x 2 lines by cascade the other IC(Slave). When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**….**	**37**	**38**	**39**	**40**
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	**….**	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	4A	**….**	64	65	66	67
	IC display (Master)								Cascade 2nd IC(Slave)							
Shift left	01	02	03	04	05	06	07	08	09	0A	0B	**….**	25	26	27	28
	41	42	43	44	45	46	47	48	49	4A	4B	**….**	65	66	67	68
Shift right	3F	00	01	02	03	04	05	06	07	08	09	**….**	23	24	25	26
	7F	40	41	42	43	44	45	46	47	48	49	**….**	63	64	65	66

SLAVE MODE DATA INPUT

When IC is under slave mode, display data is send from the other IC(master).The input data “D” is shifted at the falling edge of CL

M/S	Mode	D	CL	LAT
H	Master	Output	Output	Output
L	Slave	Input	Input	Input